VISIT…

Analog Electronic Circuits

A Simplified Approach

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A Simplified Approach

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Sanguine Technical Publishers
Bangalore - 560016
2014

Price: Rs. 375.00
USD $ 24.99

ISBN 978 81 88849 51 0

Title: Analog Electronic Circuit: A Simplified Approach
Dr.U. B. Mahadevaswamy

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Visit our website at www.sanguineindia.com

© 2008 by Sanguine Technical Publishers, Bangalore – 560 016.

Published by *Lal M Prasad* for *SANGUINE*
Production Editor: *R.Subramanian*
Typeset in *Times New Roman* by *Sigma Publishing Solutions*, *Chennai – 600 033*.

Submitted at the Lotus Feet of
His Holiness
Parama Poojya Lingaikya Jagadguru
Shree Shree Shree Shivaratri Rajendra Mahaswamigalavaru,
Founder President
J. S. S. Mahavidyapeeta
Mysore.

In Fond Memory of My Grand Mother
Late Smt. M. S. Basamma
and
My Father
Late Shree T. N. Basavaraju
who are responsible for what I am today.

Foreword

I am extremely happy to note that Mr. U. B. Mahadevaswamy from Sri Jayachamarajendra College of Engineering, Mysore has authored a book on ANALOG ELECTRONIC CIRCUITS which is helpful to the students of all Electrical Science branches of Engineering.

He is one among the most admired teacher of the Electronics & Communication department of SJCE, Mysore.

With his immense popularity as an excellent teacher among the student community for his dedicated teaching, I am sure the book will be of great asset to the students.

With his rich teaching experience of nearly two decades, this book being brought out, is a boon to the student community.

I would definitely recommend this book to not only the student community but to anyone who wants to advance their knowledge in Analog Electronics.

Dr. M. Shanthakumar

PRINCIPAL

Date: August 13, 2008

JSS ACADEMY OF TECHNICAL EDUCATION,
MAURITIUS

Preface

This book is the fruit of my rich experience of teaching the subject 'Analog Electronics' nearly for a span of 18 years. The various concepts of the subject are arranged logically and explained in a simple reader friendly language for proper understanding of the subject. A large number of problems with their step by step solution are provided for every concept. Illustrative examples are discussed to emphasize on conceptual clarity thereby presenting typical applications.

This book takes you from simple diode circuits through the analysis and design of a variety of transistor amplifiers. Analysis and design of practical feedback amplifiers and various oscillator circuits have also been covered. This book concludes with FET amplifiers wherein various FET configurations, their analysis and design have been discussed.

This book provides a simplified and systematic approach to difficult theoretical concepts in Analog Electronics. It can serve as an excellent reference material for design engineers. Those of you who enjoyed reading our previous book entitled 'Electronic Circuits' would certainly enjoy this book too.

Despite the delight taken by many reviewers in finding mistakes a few typo errors have managed to slip through the sieve. This suggests that more await discovery by you. I suppose that is what second editions are for.

U. B. MAHADEVASWAMY

Acknowledgments

My sincere Pranamas at the Lotus Feet of His Holiness Parama Poojya Jagadguru Shree Shree Shree Shivaratri Deshikendra Mahaswamigalavaru, President, J.S.S Mahavidyapeeta, Mysore, whose divine blessings inspired me to take up and successfully complete this project.

A special word of thanks to Prof. M.H.Dhananjaya, Director (Technical), who continues to be an infinite source of encouragement in all my endeavours.

I gratefully acknowledge all the encouragement from Dr. B.G.Sangameshwara, Principal, SJCE, Mysore in providing all the facilities and resources in drafting this book.

My special thanks to my teacher and my well wisher Dr.M.Shantakumar, Principal, JSS Academy of Technical Education, Mauritius, who motivated me to take up this venture and encouraged me throughout this project.

I must acknowledge the support and encouragement rendered by Prof. Dr. B. S. Basavarajiah, Special Officer, SJCE, Mysore during this project.

I sincerely thank my beloved H.O.D, Dr. R. D. Sudhaker Samuel, who encouraged me to take up this project. His support and invaluable suggestions at each and every stage of drafting this book are unforgettable. I hope without his support and encouragement, this book would hardly be in its present form.

My sincere thanks to my colleague Mr. V. Natttarasu and Mr. R. Subramanian of Sanguine Technical Publishers, who have meticulously reviewed this book and gave invaluable inputs to bring this book to its present form.

I gratefully acknowledge the support rendered during this project, by my teacher and well wisher Mr. C.Chamaraju, Assistant professor, Mathematics department, SJCE, Mysore.

Thanks to Dr.Ganesh Rao, Professor, Department of Telecommunication, MSRIT, Bangalore, for coming to my rescue at various stages in the preparation of this book.

I must thank my colleagues in the department of Electronics and Communication, SJCE, Mysore for all their suggestion towards improving the material presented.

I must thank Ms. Sheethal M. J and Ms. Swetha M. J, software Engineers, for their timely technical inputs, support and encouragement throughout this project.

I appreciate the relentless efforts of my sister's children Mr. G. Shashidharamurthy, software Engineer and Ms. Indumathi, in finding mistakes and typo errors through several readings. I also appreciate the help rendered by Ms. K. S. Sindhu, who patiently checked the solutions of all numerical examples.

I must acknowledge all the encouragement and support from my wife K. S. Umadevi in making this project a success. The timely support of my brother B.Chandra Shekara Murthy, Quality Control Engineer, Muscat and my mother K.P.Leelavthi and all my family members needs a very special mention.

Finally, my sincere gratitude for Sanguine Publishers for continuing to make my dreams a reality.

Please feel free to contact the publisher at info@sanguineindia.com for further assistance. I am sincerely grateful to all the persons mentioned above for their generous support at the right time to make this work truly marvelous.

U. B. MAHADEVASWAMY

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Chapter 1

Diode Circuits

Diodes are semiconductor devices which conduct only in one direction. Their behaviour depends on the value and polarity of the applied voltage. This chapter begins with the volt-amper characteristics of diode and takes the reader through several diode applications. Analysis of each diode circuit is presented, backed by numerous illustrative examples.

◆ 1.1 VOLT-AMPERE CHARACTERISTICS OF SEMICONDUCTOR DIODE

A semiconductor diode results when a junction is formed between a *p*-type and a *n*-type semiconductor. Such a *p-n* junction permits easy flow of charge carriers in one direction but restrains the flow in the opposite direction.

Figure 1.1 shows the biasing arrangement for a *p-n* junction under both forward and reverse biased conditions.

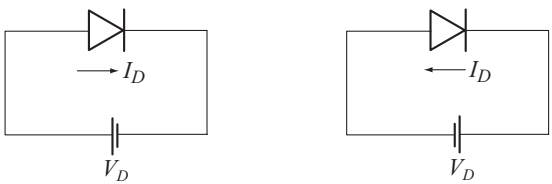


Fig. 1.1 (a) Forward biased p-n junction
(b) Reverse biased p-n junction

The *p-n* junction is forward biased for $V_D > 0$ and is reverse biased for $V_D < 0$. Under forward bias, *p-n* junction conducts heavily from anode to cathode while under reverse bias it conducts a small current from cathode to anode.

Diode Current Equation

Through the use of solid-state physics the general characteristics of a semiconductor diode can be defined by the Shockley's equation, for the forward and reverse bias regions given in Equation (1.1).

$$I_D = I_S\left[e^{\frac{V_D}{nV_T}} - 1\right] \tag{1.1}$$

where I_D = Diode current
V_D = Voltage applied across the diode
I_S = reverse saturation current

n is an ideality factor which depends on the operating conditions and physical construction. It lies between 1 and 2. Unless otherwise stated we assume $n = 1$ throughout the analysis.

V_T = Thermal voltage, given by

$$V_T = \frac{KT}{q}$$

where K = Boltzmann constant $= 1.38 \times 10^{-23}$ J / K
T = Absolute temperature in kelvin
= 273 + the temperature in ºC
q = Magnitude of electronic charge
$= 1.6 \times 10^{-19}$ Coulomb

For example, at a temperature of 27º C

$$T = 273 + 27° \text{ C} = 300 \text{ K}$$

$$V_T = \frac{KT}{q}$$

$$= \frac{\left(1.38 \times 10^{-23}\right)(300)}{1.6 \times 10^{-19}}$$

$$\approx 26 \text{ mV}$$

Forward Biased Condition

From Equation (1.1), we have

$$I_D = I_S\, e^{\frac{V_D}{nV_T}} - I_S \tag{1.2}$$

For positive values of V_D, the exponential term grows very quickly and totally dominates the effect of second term. As a result

$$I_D \approx I_S\, e^{\frac{V_D}{nV_T}} \tag{1.3}$$

Observe from Equation (1.3) that, under forward biased condition, the diode current varies exponentially with the applied forward voltage V_D.

Reverse Biased Condition

For negative values of V_D, the exponential term in Equation (1.2) drops very quickly below the level of I_S. As a result, the diode current is now given by

$$I_D \approx -I_S \tag{1.4}$$

Note from Equation (1.4) that, for negative values of V_D, the diode current is essentially constant at the level of $-I_S$.

Avalanche Breakdown

Equation (1.4) holds good for small reverse voltages. As the reverse voltage across the diode increases, the velocity of minority carriers responsible for the reverse saturation current I_S will also increase. Eventually, their velocity and the associated kinetic energy will be sufficient to release additional carriers through collisions with otherwise stable atomic structures. An ionisation process will result thereby valence electrons absorb sufficient energy to leave the parent atom. These additional electrons can then aid the ionisation process to the point where a high avalanche current is established and the avalanche breakdown is occurred. The reverse voltage at which the avalanche breakdown occurs is called the reverse breakdown voltage, denoted by V_{BV} or V_{BR} or V_{BD}. In the breakdown region, the diode current increases sharply with diode voltage remaining constant at V_{BD}.

It should be noted that, Avalanche breakdown is a destructive phenomenon. Therefore the diode should not be operated in the avalanche breakdown region. The manufacturer specifies peak reverse voltage (PRV) for the safe operation of diode under reverse bias.

The maximum reverse-bias voltage which can be applied before entering the breakdown region is called peak inverse voltage (PIV rating) or the peak reverse voltage (PRV rating).

For the diode BAY 73, the manufacturer specifies PIV rating of 100 V and break down voltage of 125 V. For this diode if the applied reverse voltage exceeds 100 V, it is likely to enter into break down region.

Volt-ampere Characteristics

Figure 1.2 shows the volt-ampere characteristics of Ge, Si and GaAs diodes. V_K is the knee voltage or the threshold voltage at which the forward current of diode begins to increase exponentially with the applied forward voltage.

Table 1.1 compares the values of V_K, I_S and reverse break down voltages for Ge, Si and GaAs diodes.

Table 1.1 V_K, I_s and V_{BD} for Ge, Si and GaAs diodes

Semi conductor	*Parameter*		
	V_K	I_S	V_{BD}
Ge	0.3 V	1 μA	upto 400 V
Si	0.7 V	10 pA	50 V – 20 kV
GaAs	1.2 V	1 pA	50 V – 20 kV

Observe that Ge has large level of I_S and low level of V_{BD} which are highly undesirable. For this reason Ge diodes finds limited application even though V_K is smaller than those of Si and GaAs diodes. Also note that level of V_K for Si is almost one half that of GaAs and the level of V_{BD} is almost same. Hence silicon diodes are more popular.

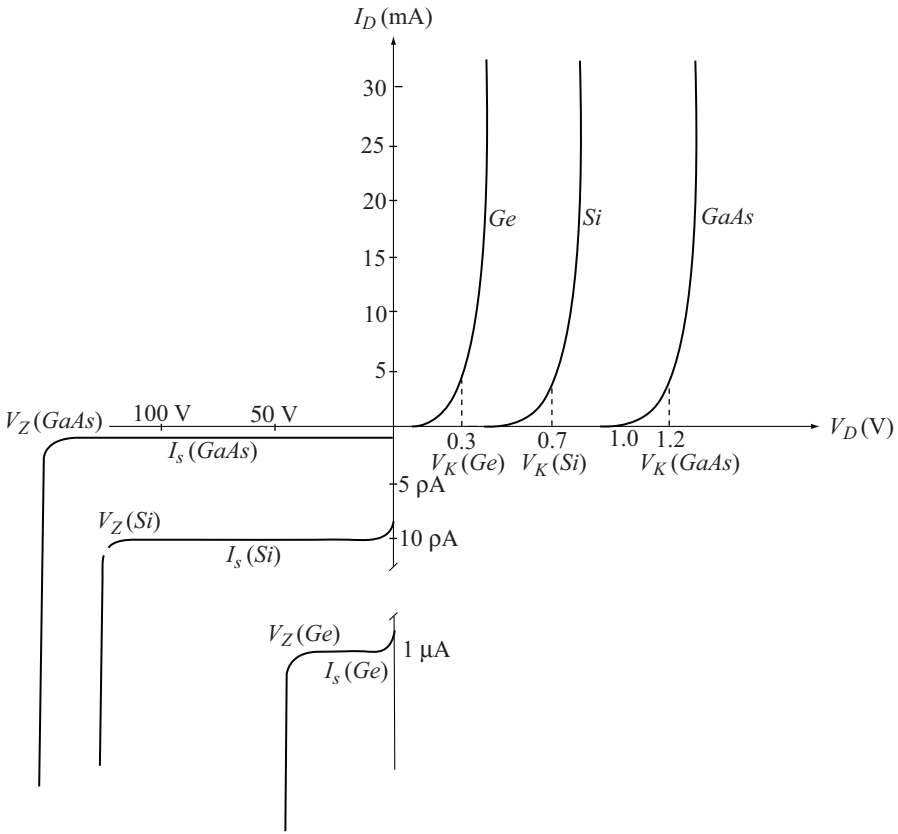


Fig. 1.2 Comparison of Ge, Si, and GaAs diodes

◆ 1.2 TEMPERATURE EFFECTS

The effect of temperature on the characteristics of a silicon diode is illustrated in Fig. 1.3.

In the forward region the characteristics of a silicon diode shift to the left at the rate of 2.5 mV per degree centigrade increase in temperature.

As shown in Fig. 1.3, when the temperature increases from 20°C to 100° C (the boiling point of water), the forward characteristics curve shifts to the left by

$$(100° \text{ C} - 80° \text{ C})\ (2.5 \text{ mV}) = 200 \text{ mV}$$

This shift is significant since the level of V_K for Si is about 0.7 V. A decrease in temperature has the reverse effect as also shown in Fig. 1.3.

In the reverse – bias region the reverse saturation current of a silicon diode doubles for every 10° C rise in temperature.

The doubling effect of I_S with temperature is given by the relation

$$I_S(T_2) = I_S(T_1)\ 2^{\frac{\Delta T}{10}} \tag{1.5}$$

where ΔT = Change in temperature

$= T_2 - T_1$

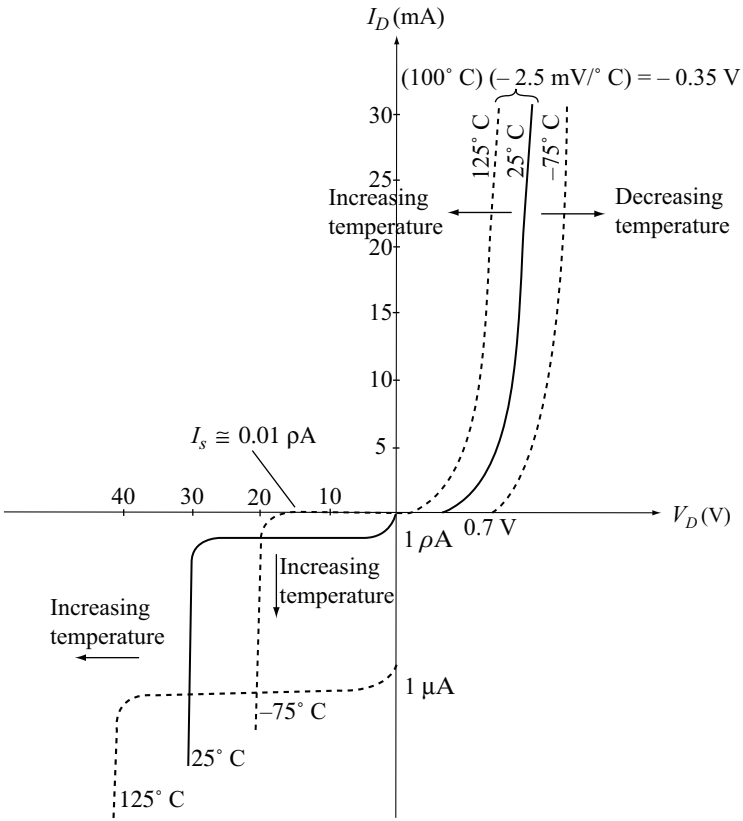


Fig. 1.3 Variation in Si diode characteristics with temperature change

Table 1.2 compares the levels of I_S for Ge, Si and GaAs at an operating temperature of 200° C.

Table 1.2 Level of I_S for Ge, Si and GaAs at 200°C

Operating temperature	*Semi conductor*		
	Ge	*Si*	*GaAs*
20°C	1 μA	10 pA	1 pA
200°C	262.14 mA	2.62 μA	0.262 μA

Observe from table that, an increase in temperature from 20°C to 200°C would result in a monstrous reverse current of 262.14 mA in Ge where as it is only limited to 2.62 μA in Si and 0.262 μA in GaAs, due to their excellent temperature characteristics.

Si diodes can work well upto maximum temperature of 200° C and GaAs diodes upto 400° C. Ge diodes are limited to low temperature applications.

The reverse breakdown voltage of a semiconductor diode will increase or decrease with temperature depending on the break down potential.

If the break down voltage is less than 5 V as in the case of zener diodes, the break down voltage decreases with temperature in the same way as shown in Fig. 1.3.

◆ 1.3 COMPARATIVE STUDY OF Ge, Si AND GaAs DEVICES

The comparative study of Ge, Si and GaAs devices with respect to their characteristics and applications is given in Table 1.3.

Table 1.3 Comparative study of Ge, Si and GaAs devices

Semiconductor	*Characteristics*	*Applications*
Ge	• High temperature sensitivity • High reverse saturation current • Low break down voltage	• Photo detectors • Security systems
Si	• Good temperature characteristics • Low reverse saturation current • Excellent break down voltage level • Low cost	• Full range of electronic devices • Enormously used in very large scale integrated circuits
GaAs	• Good temperature characteristics • Very low reverse saturation current • Excellent break down voltage levels • High speed of operation • Perhaps the semiconductor material of the future	Major applications in opto electronics • LED • Solar cells • photo detectors • If the manufacturing cost drops, it may be used in integrated circuits, in future.

Example 1.1

Calculate the factor by which the current will increase in a silicon diode operating at a forward voltage of 0.4 V when the temperature is raised from 25°C to 150°C. Take $n = 1$.

Solution

$T_1 = 25°C \quad T_2 = 150°C \quad V_D = 0.4\ V \quad n = 1$

$$I_S(T_2) = I_S(T_1)\ 2^{\frac{\Delta T}{10}}$$

$$\Delta T = T_2 - T_1$$

$$= 150°C - 25°C = 125°C$$

$$I_S(T_2) = I_S(T_1)\, 2^{\frac{125}{10}}$$

$$\frac{I_S(T_2)}{I_S(T_1)} = 5793 \tag{A}$$

$$I_D = I_S\left[e^{\frac{V_D}{nV_T}} - 1\right]$$

Since $n = 1$

$$I_D = I_S\left[e^{\frac{V_D}{V_T}} - 1\right]$$

$$I_D(T_1) = I_S(T_1)\left[e^{\frac{V_D}{V_{T_1}}} - 1\right] \tag{B}$$

$$I_D(T_2) = I_S(T_2)\left[e^{\frac{V_D}{V_{T_2}}} - 1\right] \tag{C}$$

Dividing Equation (C) by Equation (B) we have

$$\frac{I_D(T_2)}{I_D(T_1)} = \frac{I_S(T_2)}{I_S(T_1)}\left[\frac{e^{\frac{V_D}{VT_2}} - 1}{e^{\frac{V_D}{VT_1}} - 1}\right] \tag{D}$$

$$V_T = \frac{273 + T}{[q/K]} = \frac{273 + T}{11{,}600}$$

$$V_{T_1} = \frac{273 + 25}{11600} = 0.0257 \text{ V}$$

$$V_{T_2} = \frac{273 + 150}{11600} = 0.0364 \text{ V}$$

$$e^{\frac{V_D}{V_{T_2}}} - 1 = e^{\frac{0.4}{0.0364}} - 1 = 59218.78$$

$$e^{\frac{V_D}{V_{T_1}}} - 1 = e^{\frac{0.4}{0.0257}} - 1 = 5747078.29$$

Now from Equation (D)

$$\frac{I_D(T_2)}{I_D(T_1)} = 5793\left[\frac{59218.78}{5747078.29}\right] = 59.69$$

$$\Rightarrow \quad I_D(T_2) = 59.69\, I_D(T_1)$$

1.4 DIODE RESISTANCE LEVELS

The forward characteristics of the diode is non linear since the diode current changes exponentially with the applied forward voltage. As a result the resistance of the diode will change when the operating point moves from one region to another. Depending upon the type of the applied signal we can define the following three resistance levels of the diode.

(a) DC or static resistance
(b) AC or dynamic resistance
(c) Average ac resistance

Now let us study the definition of each of these resistance levels and the procedure to find them from the diode characteristics.

1.4.1 DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor results in a dc current. The resistance of diode to the flow of dc current is called DC or static resistance.

Let the applied dc voltage V_D, results in a dc current I_D as shown in Fig. 1.4. The dc resistance of the diode at the operating point is given by

$$R_D = \frac{V_D}{I_D} \tag{1.6}$$

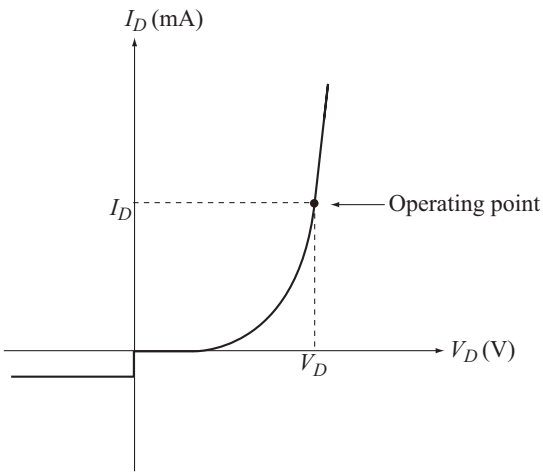


Fig. 1.4 Determination of R_D of a diode

We can make the following observations from Fig. 1.4.

- Under reverse bias, the diode current is almost zero. Hence the dc resistance level in the reverse-bias region is quite high.
- The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics.
- Higher the current through the diode, lower is the dc resistance level.

1.4.2 AC or Dynamic Resistance

The resistance of the diode to the flow of ac current is called the ac or dynamic resistance.

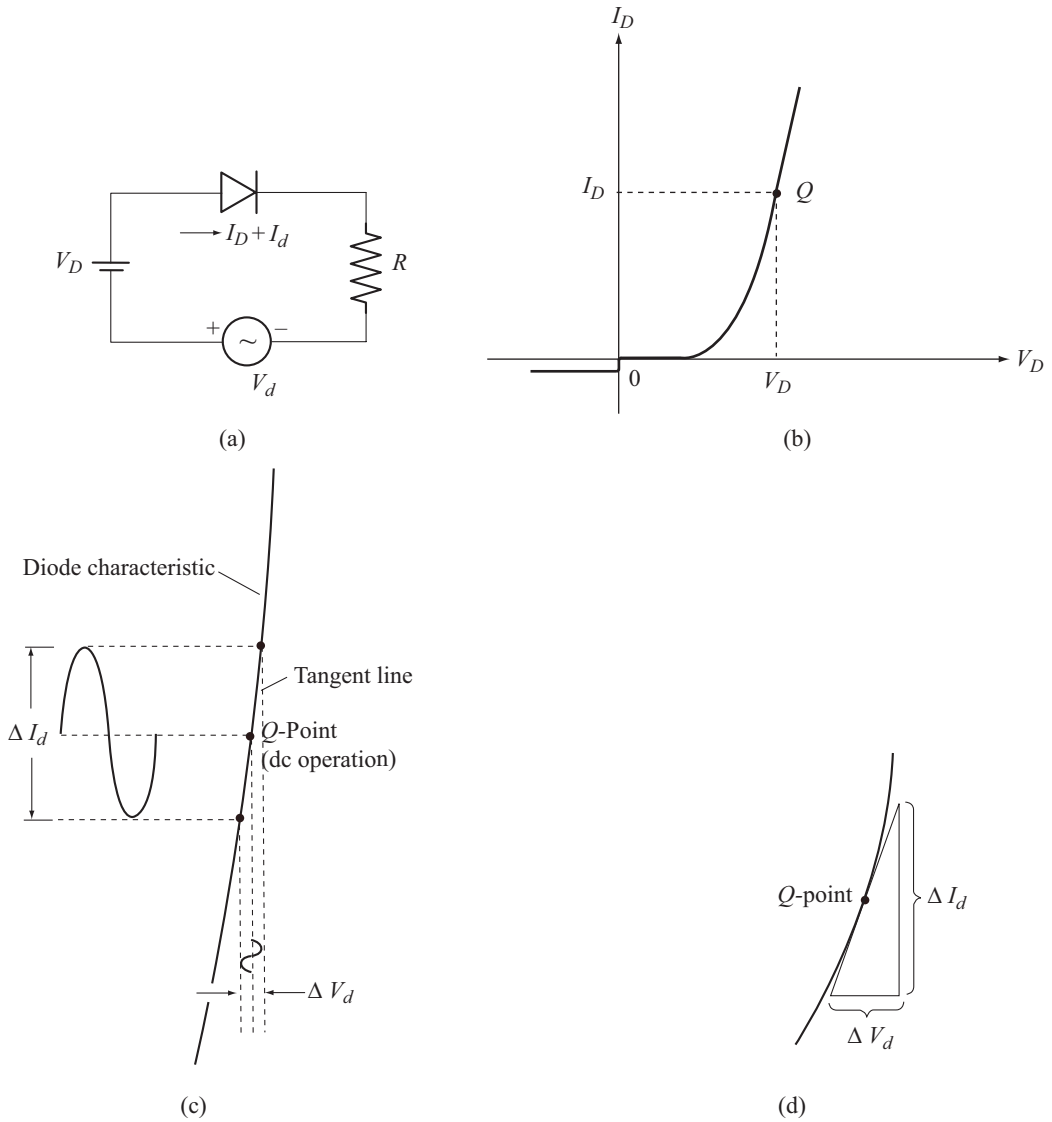


Fig. 1.5 (a) Biased diode with ac input
(b) Q point current and voltage
(c) Variation of diode current and voltage about Q point
(d) Graphical determination of ac resistance

The application of dc voltage V_D in the circuit of Fig. 1.5(a) sets up a dc current I_D resulting in an operating point Q as shown in Fig. 1.5(b). Since V_D and I_D are not changing with time, the operating point is designated as quiescent operating point or Q-point.

If a sinusoidal voltage is also applied then the diode current and voltage will also vary sinusoidally about the Q point as shown in Fig. 1.5(c).

If ΔV_d is the change in ac diode voltage and ΔI_d is the corresponding change in ac diode current, then the ac or dynamic resistance of diode is defined by

$$r_d = \frac{\Delta V_d}{\Delta I_d} \tag{1.7}$$

The level of r_d can be measured by drawing a tangent to the characteristics at the Q point and taking equal increments of diode voltage and diode current about the Q point, as shown in Fig. 1.5(d). The definition of r_d in Equation (1.7) assumes that ΔV_d and ΔI_d are small in amplitude. For this reason r_d is also called the small signal resistance.

It should be noted that, r_d is given by the reciprocal of the slope of the characteristics at the desired Q point. If the Q point is located higher up the curve, the slope becomes steeper [large] resulting in a small value of r_d. Therefore, *the higher the Q point of operation (higher current or higher voltage)*, *the smaller is the ac resistance.*

1.4.3 Average AC Resistance

The ac or dynamic resistance is measured under small signal operation. If the ac input signal amplitude is large it produces a broad swing about the Q point as shown in Fig. 1.6. The resistance associated with the device under large signal operation is called the average ac resistance.

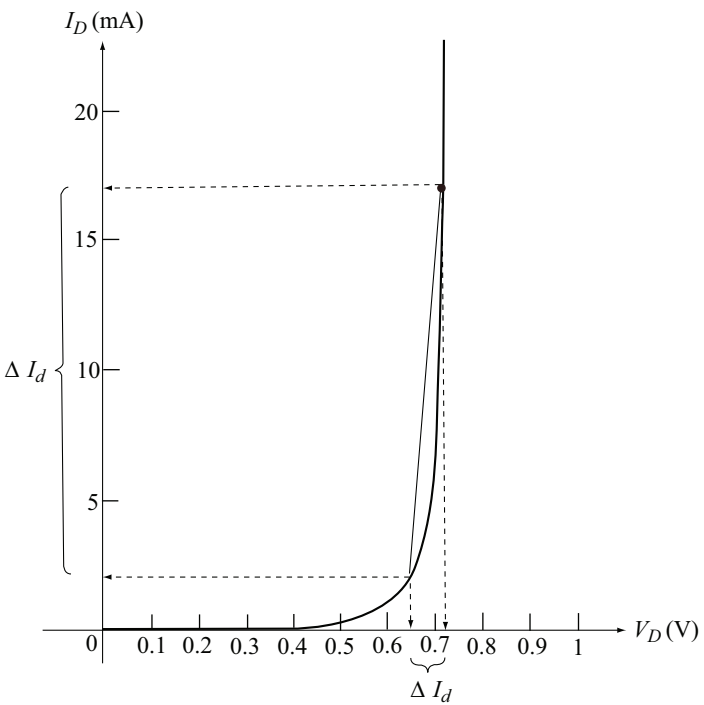


Fig. 1.6 Determining the average ac resistance between indicated limits

The average ac resistance is the resistance determined by a straight line drawn between the two intersections established by the maximum and minimum values of input voltage as shown in Fig. 1.6.

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}} \tag{1.8}$$

Average ac resistance gives one resistance level for a broad swing of current and voltage levels in the diode. r_{av} is used in the diode equivalent circuits, which are useful in the analysis of diode circuits. *As with the dc and ac resistance levels, the lower the levels of currents used to determine r_{av}, the higher is the resistance levels.*

Example 1.2

Following data are available for a silicon diode.

V_D	–12 V	0.6 V	0.8 V
I_D	1 μA	2.5 mA	30 mA

Calculate the dc resistance levels at
(a) $I_D = 2.5$ mA
(b) $I_D = 30$ mA
(c) $V_D = -12$ V

Solution

dc resistance, $R_D = \dfrac{V_D}{I_D}$

(a) At $I_D = 2.5$ mA, $V_D = 0.6$ V

$$R_D = \frac{0.6 \text{ V}}{2.5 \text{ mA}}$$
$$= 240\ \Omega$$

(b) At $I_D = 30$ mA, $V_D = 0.8$ V

$$R_D = \frac{0.8 \text{ V}}{30 \text{ mA}}$$
$$= 26.67\ \Omega$$

(c) At $V_D = -12$ V, $I_D = 1$ μA

$$R_D = \frac{12 \text{ V}}{1\ \mu\text{A}}$$
$$= 12\ \text{M}\Omega$$

Observe that the reverse resistance is very high and forward dc resistance decreases with increase in current level.

Example 1.3

Following data are available for a silicon diode.

V_D (Vo1ts)	0.65	0.71	0.76	0.77	0.78	0.79	0.8
I_D (mA)	0	2	4	15	20	25	30

(a) Determine the ac resistance at $I_D = 2$ mA.
(b) Determine the ac resistance at $I_D = 25$ mA.
(c) Calculate the dc resistances at $I_D = 2$ mA and $I_D = 25$ mA and compare with ac resistance levels.

Solution

AC or dynamic resistance is

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

To find r_d, we have to take symmetrical swing about the specified operating point.

(a) $\boldsymbol{I_D = 2}$ **mA**

It is convenient to take equal swing of 2 mA about $I_D = 2$ mA since V_D values are provided at $I_D = 0$ mA and 4 mA.

at $I_D = 0$ mA $V_D = 0.65$ V and

at $I_D = 4$ mA $V_D = 0.76$ V

$$\therefore \quad \Delta V_d = 0.76 \text{ V} - 0.65 \text{ V} = 0.11 \text{ V}$$

$$\Delta I_d = 4 \text{ mA} - 0 \text{ mA} = 4 \text{ mA}$$

$$r_d = \frac{0.11 \text{ V}}{4 \text{ mA}} = 27.5 \ \Omega$$

(b) $\boldsymbol{I_D = 25}$ **mA**

In this case it is convenient to take equal swing of 5 mA about $I_D = 25$ mA

$V_D = 0.78$ V at $I_D = 20$ mA

$V_D = 0.8$ V at $I_D = 30$ mA

$$\Delta V_d = 0.8 \text{ V} - 0.78 \text{ V} = 0.02 \text{ V}$$

$$\Delta I_d = 30 \text{ mA} - 20 \text{ mA} = 10 \text{ mA}$$

$$r_d = \frac{0.02 \text{ V}}{10 \text{ mA}} = 2 \ \Omega$$

(c) ***DC Resistance***

at $I_D = 2$ mA $\quad R_D = \dfrac{0.71 \text{ V}}{2 \text{ mA}} = 355 \ \Omega$

at $I_D = 25$ mA $\quad R_D = \dfrac{0.79 \text{ V}}{25 \text{ mA}} = 31.6 \ \Omega$

The results are compared in the following table.

Diode current	Diode resistance	
	r_d	R_D
2 mA	27.5 Ω	355 Ω
25 mA	2 Ω	31.6 Ω

Note that $r_d \ll R_D$.

Example 1.4

Using the data given in example 1.3, find the average ac resistance when I_D swings from 2 mA to 30 mA.

Solution

$V_D = 0.71$ V at $I_D = 2$ mA
$V_D = 0.8$ V at $I_D = 30$ mA

$$\Delta V_d = 0.8 \text{ V} - 0.71 \text{ V} = 0.09 \text{ V}$$
$$\Delta I_d = 30 \text{ mA} - 2 \text{ mA} = 28 \text{ mA}$$

Average ac resistance is

$$r_{av} = \frac{\Delta V_d}{\Delta I_d} = \frac{0.09 \text{ V}}{28 \text{ mA}} = 3.2 \ \Omega$$

◆ 1.5 ANALYTICAL EXPRESSION FOR DYNAMIC RESISTANCE OF DIODE

In Section 1.4.2 we have illustrated the graphical determination of dynamic resistance of diode. Graphically the dynamic resistance is equal to the reciprocal of the slope of the curve at the Q point. We can also obtain the analytical expression for dynamic resistance using the basic definition in differential calculus.

i.e., $$r_d = \left.\frac{dV_D}{dI_D}\right|_{Q\text{point}} \tag{1.9}$$

Let us start with the diode current equation

$$I_D = I_S \left[e^{\frac{V_D}{nV_T}} - 1 \right]$$
$$I_D \approx I_S \, e^{\frac{V_D}{nV_T}} \tag{1.10}$$

Differentiating with respect to V_D, we obtain

$$\frac{dI_D}{dV_D} = \left[I_S \, e^{\frac{V_D}{nV_T}} \right] \cdot \frac{1}{nV_T}$$

$$\frac{dI_D}{dV_D} = I_D \left[\frac{1}{nV_T} \right]$$

But $$\frac{dV_D}{dI_D} = \frac{1}{\left[\frac{dI_D}{dV_D} \right]}$$

$$\therefore \quad r_d = \frac{1}{I_D \left[\frac{1}{nV_T} \right]}$$

or $$r_d = \frac{nV_T}{I_D} \tag{1.11}$$

Taking $n = 1$ and $V_T = 26$ mV (at room temperature) we have

$$r_d = \frac{26 \text{ mV}}{I_D} \tag{1.12}$$

Note that, the dynamic resistance can be obtained by simply dividing 26 mV by the diode current I_D at Q point.

The following important remarks can be made with reference to Equation (1.12).

- Equation (1.12) gives accurate results only for values of I_D in the vertical-rise section of the curve.
- For lower values of I_D, we have to take $n = 2$ for Si and as a result the value of r_d obtained in Equation (1.12) must be multiplied by 2.
- For small values of I_D below the knee of the curve, Equation (1.12) becomes inappropriate.

1.5.1 Bulk Resistance r_B

The dynamic resistance r_d is the ac resistance of the *pn* junction. We have not yet considered the following two resistances.

- The resistance of the semiconductor material itself, called the body resistance.
- The resistance introduced by the connection between the semiconductor material and external metallic conductor, called the contact resistance.

The sum of body resistance and contact resistance is called the bulk resistance denoted by r_B.

1.5.2 Dynamic Resistance taking r_B into Account

The dynamic resistance without taking r_B into account is given in Equation (1.12) as

$$r_d = \frac{26 \text{ mV}}{I_D}$$

Now including the effect of r_B, the dynamic resistance is given by

$$r'_d = r_d + r_B$$

$$r'_d = \frac{26 \text{ mV}}{I_D} + r_B \tag{1.13}$$

r_B can range from typically 0.1 Ω for high power devices to 2 Ω for some low power, general purpose diodes.

At low levels of current, the value of r_B is smaller compared to that of r_d and therefore the effect of r_B can be ignored.

At high levels of current, the value of r_B may approach that of r_d. But the external resistors in the diode circuits will be much larger than r_B and hence effect of r_B is swamped out by these external resistors.

Therefore unless otherwise specified, we ignore r_B in the foregoing analysis.

Hence $$r'_d \approx r_d = \frac{26 \text{ mV}}{I_D} \tag{1.14}$$

Example 1.5

For the diode considered in example 1.3, calculate the dynamic resistance at $I_D = 2$ mA and 25 mA using Equation (1.12). Compare the results with those obtained in example 1.3 and comment.

Solution

$I_D = 2$ mA [Low current level]

From example 1.3

$$r_d = 27.5 \ \Omega$$

Using Equation (1.12)

$$r_d = \frac{26 \text{ mV}}{I_D} = 13 \ \Omega$$

For low current levels, $n = 2$

$\therefore$ The value of r_d calculated using Equation (1.12) has to be multiplied by 2.

$$r_d = 2\,[13\ \Omega] = 26\ \Omega$$

The difference, 27.5 Ω – 26 Ω = 1.5 Ω, could be treated as contribution due to r_B.

$I_D = 25$ mA [High current level]

From example 1.3

$$r_d = 2 \ \Omega$$

Using Equation (1.12)

$$r_d = \frac{26 \text{ mV}}{25 \text{ mA}} = 1.04 \ \Omega$$

For high current levels, $n = 1$

The difference, 2 Ω – 1.04 Ω = 0.96 Ω, could be treated as contribution due to r_B.

1.6 EQUIVALENT CIRCUITS OF DIODE

The equivalent circuit of a diode is a circuit that closely approximates the diode behaviour under forward and reverse biased conditions. The diode equivalent circuit is also called the diode model. The analysis of diode circuits can be easily performed using Kirchoff's voltage law (KVL) and Kirchoff's current law (KCL), after replacing the diodes with their equivalent circuits.

1.6.1 Piecewise-linear Equivalent Circuit

Piecewise-linear equivalent circuit of a diode can be obtained by approximating the characteristics of the diode by straight line segments as shown in Fig. 1.7.

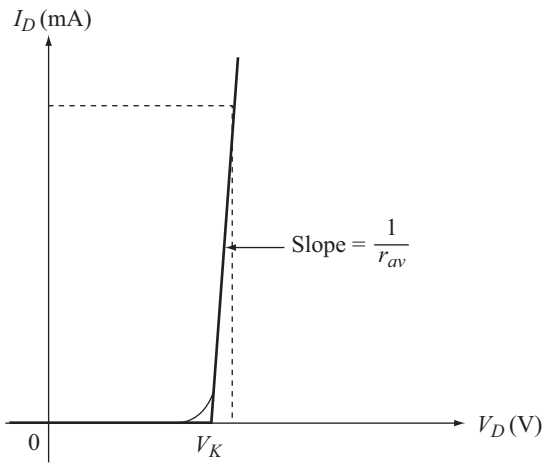


Fig. 1.7 Piece-wise linear characteristics of a diode

We observe the following facts from the piece-wise linear characteristics of Fig. 1.7.

- For $V_D < V_K$, the diode current is zero.
- For $V_D \geq V_K$, the diode current increases linearly with diode voltage. The diode current is related linearly with the diode voltage by the average ac resistance r_{av}.
- The diode acts as an open circuit under reverse bias since, the reverse current through the diode is zero.

Figure 1.8 shows the piecewise linear equivalent circuit of a diode.

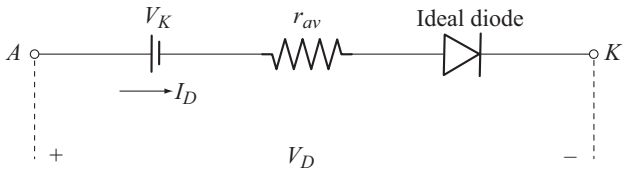


Fig. 1.8 Piecewise linear equivalent circuit of a diode

The polarity of V_K is such that, it opposes the flow of I_D from anode to cathode as long as $V_D < V_K$. Once V_D exceeds V_K, r_{av} limits the diode current.

When conducting, ideal diode acts as a short circuit (0 Ω) and behaves as an open circuit (∞ Ω) when it is reverse biased.

1.6.2 Simplified Equivalent Circuit

In most of the diode circuits external resistors will come in series with diodes during conduction. The resistance levels of these elements will be in the order of few hundred ohms to few tens of kilo-ohms. Under this condition r_{av} can be ignored owing to its sufficiently small value. If we apply the approximation, $r_{av} = 0\ \Omega$ in the piecewise linear equivalent circuit of Fig. 1.8, we obtain the simplified equivalent circuit of diode shown in Fig. 1.9(b). Since $r_{av} = 0$, slope becomes infinite in the piecewise linear characteristics as shown in Fig. 1.9(a).

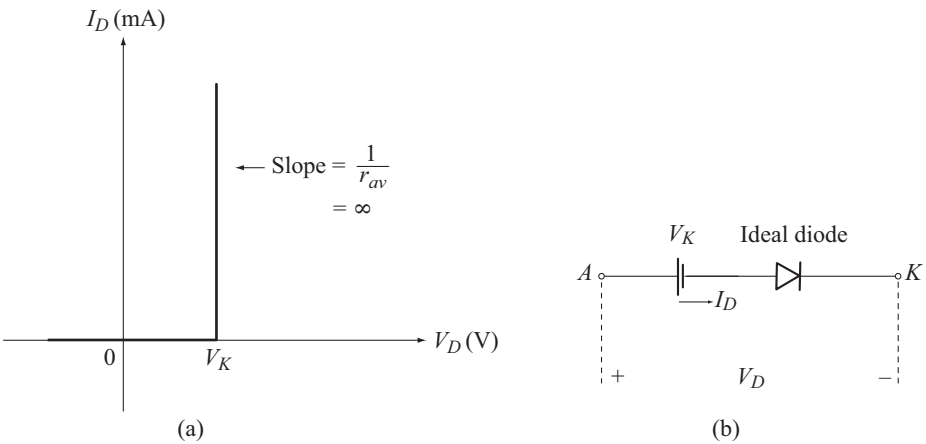


Fig. 1.9 (a) Piece wise linear characteristics with $r_{av} = 0\ \Omega$
(b) Simplified equivalent circuit of a diode

1.6.3 Ideal Equivalent Circuit

For Si diode, the level of V_K is 0.7 V. If the external voltage applied to the diode circuit is much greater than V_K, which is true in most of the cases, the effect of V_K can be ignored. If we apply the approximation $V_K = 0$ V to the piecewise linear characteristics and the simplified equivalent circuit of Fig. 1.9 we obtain the piecewise characteristics and the equivalent circuit of ideal diode shown in Fig. 1.10.

Ideal diode is characterised by

- Zero knee voltage ($V_K = 0$ V)
- Zero average ac resistance ($r_{av} = 0\ \Omega \Rightarrow$ short circuit between anode and cathode)
- Infinite reverse resistance ($R_r = \infty\ \Omega \Rightarrow$ open circuit between anode and cathode)

Ideal diode can be regarded as an electronic switch in the sense that, it acts as a short circuit for $V_D \geq 0$ V and open circuit for $V_D < 0$ V.

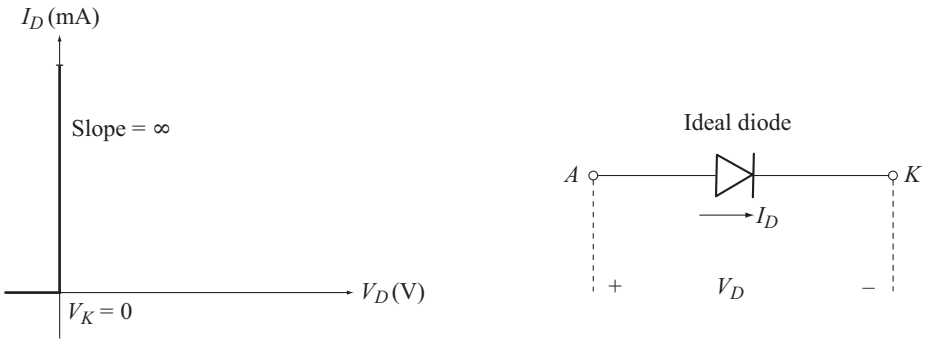


Fig. 1.10 Characteristics and equivalent circuit of ideal diode

1.6.4 Summary of Diode Equivalent Circuits

The summary of diode equivalent circuits is given in Table 1.4.

Table 1.4 Diode equivalent circuits (models)

Type	*Conditions*	*Model*	*Characteristics*
Piecewise-linear model	r_{av} and V_K are considered	+ V_K – r_{av} Ideal diode	I_D, r_{av}, 0, V_K, V_D
Simplified model	$R_{\text{network}} \gg r_{av}$	+ V_K – Ideal diode	I_D, 0, V_K, V_D
Ideal diode	$R_{\text{network}} \gg r_{av}$ $E_{\text{network}} \gg V_K$	Ideal diode	I_D, 0, V_D

◆ 1.7 TRANSITION AND DIFFUSION CAPACITANCE

The basic equation for the capacitance of a capacitor is given by

$$C = \frac{Q}{V} \tag{1.15}$$

where Q = Charge on capacitor plate
V = Applied voltage

In a diode the number of charge carriers crossing the Junction directly depends on the applied voltage, giving rise to a capacitive effect. Two capacitances exists in the diode one in the forward biased region and the other in the reverse biased region. They are

1. Transition or depletion capacitance (C_T)
2. Diffusion or storage capacitance (C_D)

***Transition or Depletion Capacitance* [C_T]**

The basic equation for the capacitance of a parallel plate capacitor is given by

$$C = \frac{A\,\varepsilon}{d} \tag{1.16}$$

A = Plate area
d = Distance between plates
ε = Permittivity of the dielectric (insulator) between the plates

In the reverse bias region there exists a depletion region which is free of carriers, that behaves essentially like an insulator between the p and n layers of opposite charge. This gives rise to a capacitance which is called the depletion capacitance or transition capacitance, C_T. With increase in reverse voltage, the depletion width d increases and hence the depletion capacitance decreases as shown in Fig. 1.11(a).

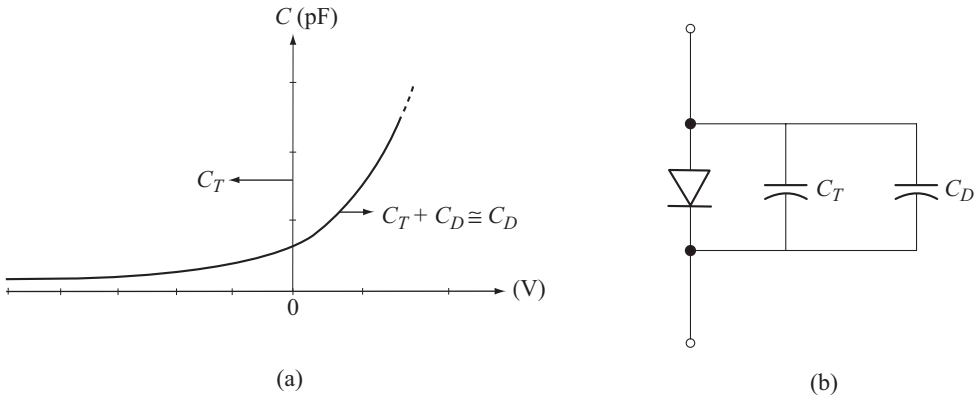


Fig. 1.11 (a) Transition and diffusion capacitance versus applied bias for a Si diode
(b) Diode with its capacitances

***Diffusion Capacitance or Storage Capacitance* [C_D]**

Under forward bias, the holes move from p side to n side and electrons from n side to p side. The electrons in p side and the holes on n side are called minority carriers. The number of excess minority carriers change with the applied bias and constitutes a voltage dependent charge storage or capacitance. Because this extra charge is caused by the diffusion of majority carriers across the junction, the capacitance is called the diffusion capacitance denoted by C_D. With increase in forward voltage, the diffusion of majority carriers will also increase giving rise to an increase in diffusion capacitance as shown in Fig. 1.11(a).

It is important to note that, depletion capacitance is dominant under reverse bias. Since the depletion width is very small under forward bias, diffusion capacitance is predominant. The effect of C_T and C_D are considered by placing them in parallel across the diode as shown in Fig. 1.11(b).

Special diodes optimised for use as voltage-dependent capacitors, operating under reverse bias are called varactor diodes. Varactor diodes finds application in communication systems.

1.8 CHARGE STORAGE AND REVERSE RECOVERY TIME

Consider a rectifier diode which is forward biased and carrying a constant forward current I_F as shown in Fig. 1.12.

Due to the application of forward bias, holes move from *p* region to *n* region and electrons move from *n* region to *p* region (it may be noted that holes in *n* region and electrons in *p* region are minority carriers). Therefore when the diode is conducting, *p* region has plenty (excess) of electrons and *n* region has plenty (excess) of holes which are taking part in conduction. The excess electrons in *p* region and excess holes in *n* region are called stored charges and this phenomenon is called charge storage.

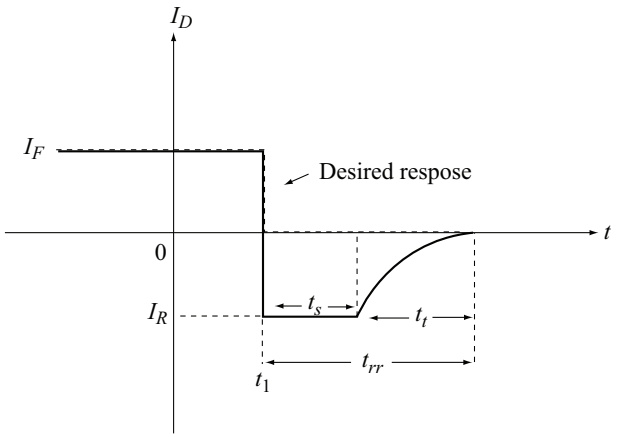


Fig. 1.12 Reverse recovery in rectifier diode

If the conducting diode is suddenly reverse biased at $t = t_1$, the diode current does not fall immediately from I_F to zero but it becomes zero after a time, t_{rr}, called reverse recovery time as explained below.

1. A large number of stored charge, (minority carriers) are present in each region. A certain amount of time, t_s, called the storage time is required for the minority carriers to return to their majority carrier state. Since excess holes in *n* region are moving towards *p* region and excess electrons in *p* region are moving towards n region, the current direction reverses in the diode. As a result the diode conducts a reverse current I_R during the interval t_s.
2. Once the excess or stored charges returned to their original regions, the reverse current gradually decreases from I_R to zero in the internal t_t, which is called the transition interval.

The reverse recovery time t_{rr} is the sum of storage time t_s and the transition time t_t.

i.e., $$t_{rr} = t_s + t_t \tag{1.17}$$

As a guide, t_{rr} is usually defined as the time taken by the reverse current to drop to 10 percent of the forward current.

For example IN4148 has a t_{rr} of 4 ns. If this diode has a forward current of 20 mA, and it is suddenly reverse biased, it takes approximately 4 ns for the reverse current to decrease to 2 mA.

◆ 1.9 DIODE SPECIFICATION SHEETS

Specification sheets or data sheets for semiconductor devices are provided by the manufacturer, which give certain data or characteristics that are very helpful to the designer while selecting the devices for a specific applications. The commonly provided data for a diode on specification sheets are:

1. The forward voltage V_F (at a specified current and temperature)
2. The maximum forward current I_F (at a specified temperature)
3. The reverse saturation current I_R (at a specified voltage and temperature)
4. The reverse-voltage rating PIV or PRV (at a specified temperature)
5. The maximum power dissipation level (at a particular temperature)

$$P_{D\max} = V_D I_D$$
$$\approx (0.7 \text{ V}) I_D \qquad [\text{For Si diode}]$$

6. Capacitance levels
7. Reverse recovery time (t_{rr})
8. Operating temperature range.

For the silicon diode BAY73 we find the following data on specification sheets.

1. Maximum forward current I_F : 500 mA
2. Reverse saturation current I_R : 500 nA
3. Peak inverse voltage PIV : 100 V
4. Break down voltage : 125 V
5. Maximum power dissipation $P_{D\max}$: 500 mW
6. Capacitance : 8 pF
7. Reverse recovery time t_{rr} : 3 μS
8. Operating temperature range : 175 °C (maximum)

For instance, if in a given application the expected maximum reverse voltage is 50 V, BAY 73 diode can be safely used since its PIV rating is 100 V. If the expected maximum reverse voltage is more than 100 V, then the diode with higher PIV rating must se selected. Similarly the other ratings must be considered while selecting a diode for a specified application.

1.10 CLASSIFICATION OF JUNCTION DIODES

Based on currents, diodes may be classified as

(i) Low-current diodes
(ii) Medium-current diodes
(iii) High-current diodes

Typically low-current diodes have a body 3 mm long with a coloured band close to the cathode for identification as shown in Fig. 1.13. These diodes can withstand forward currents of the order of 100 mA and reverse voltage of about 75 V. The reverse current at room temperature is typically less than 1 μA.

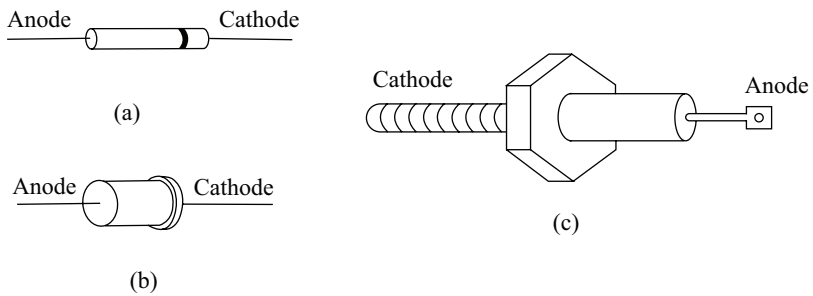


Fig. 1.13 (a) Low current diode
(b) Medium current diode
(c) High current diode

Medium current diodes are packaged in a metal can-like casing of typical diameter 8.9 mm and length 7.6 mm as shown in Fig. 1.13(b). They can carry a forward current in the range of about 400 – 500 mA and withstand reverse voltage of about 200 – 300 V.

The appearance of a high current diode in a solid metal package is shown in Fig. 1.13(c). The diode is screwed into a metal heat sink for quick dissipation of the heat generated when high current is conducted through the device. Typical body diameter is 7.8 mm and the total length is 31.2 mm. These diodes can carry several amperes of current and can withstand reverse voltage of several hundreds of volts.

1.11 LOAD-LINE ANALYSIS OF DIODE CIRCUIT

The load line analysis is the graphical method of analysing diode circuits. In this method the current and voltage levels in the diode circuit to the applied load are obtained by drawing the load line on the actual diode characteristics. The procedure for constructing the load-line is explained below.

Figure 1.14(a) shows a series diode circuit and characteristics of diode is shown in Fig. 1.14(b).

Applying KVL to the circuit of Fig. 1.14(a) we have

$$V - V_D - I_D R = 0$$

or

$$V = V_D + I_D R \tag{1.18}$$

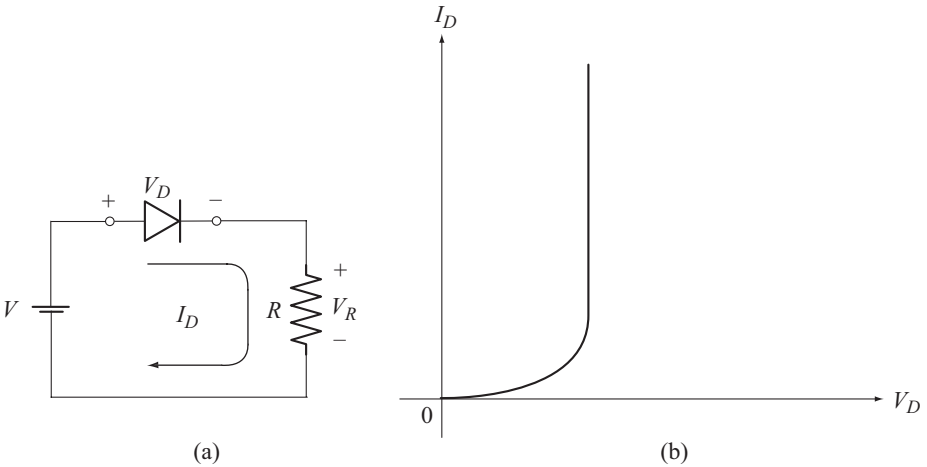


Fig. 1.14 (a) Series diode configuration
(b) Diode characteristics

For any point say A on I_D axis, $V_D = 0$.
Using $V_D = 0$ in Equation (1.18) we have

$$I_D = \frac{V}{R} \tag{1.19}$$

Now the coordinates of point A are

$$A\,(V_D, I_D) = A\left(0, \frac{V}{R}\right)$$

Similarly for any point B on V_D axis, $I_D = 0$.
Using $I_D = 0$ in Equation (1.18), we obtain

$$V_D = V \tag{1.20}$$

Now the coordinates of point B are

$$B\,(V_D, I_D) = B\,(V, 0)$$

Let us draw the load line on the diode characteristics by connecting the points A and B as shown in Fig. 1.15. The intersection of load line with characteristics curve gives the Q point.

The co-ordinates of the Q point, gives the diode voltage V_{DQ} and the diode current I_{DQ} for the applied load R.

The straight line AB is also called the dc load line since it is drawn for the dc conditions. Once I_{DQ} is known we can find the voltage across the load resistance R using

$$V_R = I_{DQ}\,R \tag{1.21}$$

or

$$V_R = V - V_{DQ} \tag{1.22}$$

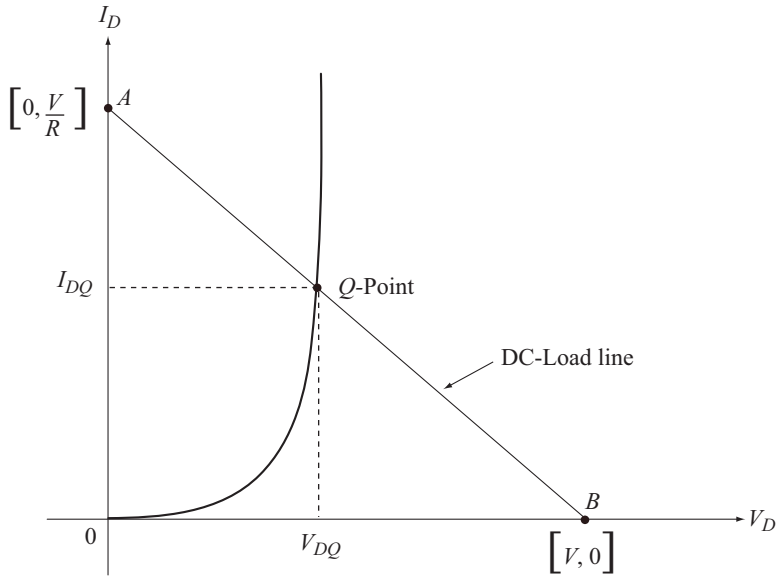


Fig. 1.15 DC load-line drawn on diode characteristics

Equation (1.18) can also be put in the form

$$I_D = \left[-\frac{1}{R} \right] V_D + \frac{V}{R} \tag{1.23}$$

Equation (1.23) represents the dc load line with a slope $-\frac{1}{R}$ and intercept $\frac{V}{R}$ on I_D axis.

Load line analysis described above uses the diode characteristics which is available on specification sheets. The characteristics of the device in actual use may be different from that available on data sheet. Hence the results obtained may be slightly different from the actual results. Also the graphical analysis become tedious for a complex circuit which uses diodes in many branches. The best method to analyse the diode circuits is to use the diode equivalent circuit which is described in the next section.

◆ 1.12 ANALYSIS OF DIODE CIRCUITS USING THE DIODE EQUIVALENT CIRCUIT

In this technique each diode in the circuit is replaced by its appropriate equivalent circuit depending upon whether the diode is forward biased or reverse biased. The diode equivalent circuits were developed in section 1.6.1 using the piece - wise linear characteristics.

In majority of the circuits, the external circuit resistance levels are much greater than the average diode resistance. Hence we can use approximate equivalent circuit which is reproduced in Fig. 1.16(a), neglecting the effect of r_{av}.

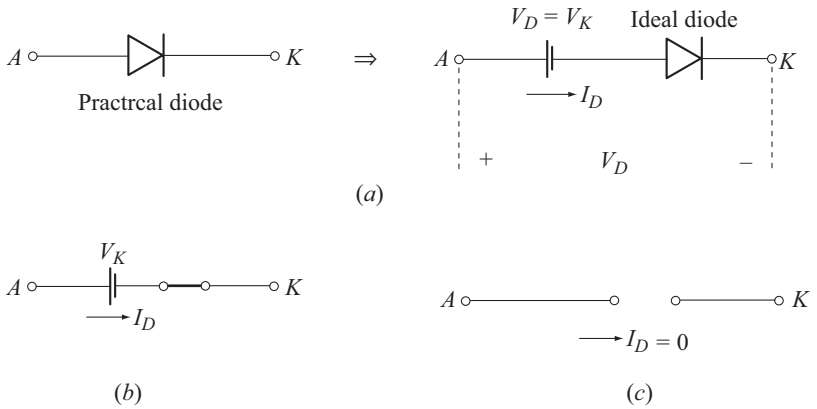


Fig. 1.16 (a) Approximate equivalent circuit of diode
(b) Equivalent circuit when diode conducts
(c) Equivalent circuit when diode is reverse biased

Note that ideal diode represents short circuit when it conducts and an open circuit under reverse bias as shown in Fig. 1.16(b) and Fig. 1.16(c) respectively.

If V_K is neglected compared with external applied voltages the equivalent circuit reduces to that of ideal diode which represents a short circuit under forward bias and open circuit under reverse bias as shown in Fig. 1.17.

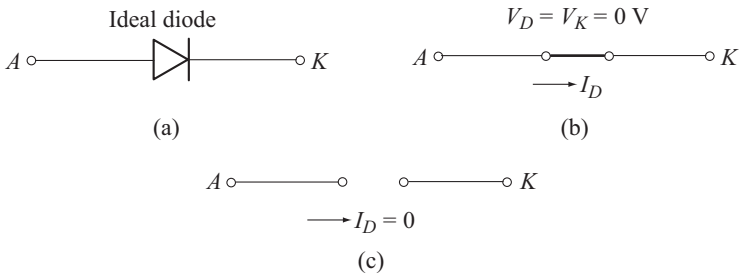


Fig. 1.17 (a) Ideal diode
(b) Equivalent circuit under forward bias
(c) Equivalent circuit under reverse bias

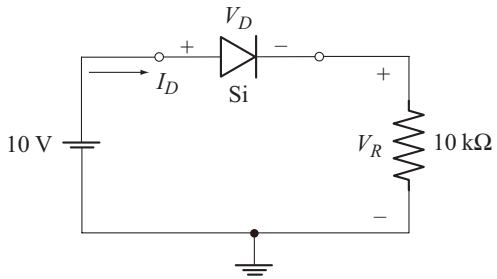
The analysis of series, parallel and series-parallel diode circuits are considered in the following examples.

Example 1.6

For the diode circuit shown

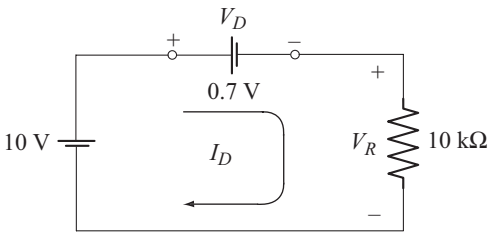
(a) Calculate I_D, V_D and V_R

(b) Repeat part (a) if the battery polarity is reversed



Solution

(a) The diode conducts since the battery voltage forward biases the diode (10 V > V_K). Let us replace the diode by its approximate equivalent circuit.



$$V_D = V_K = 0.7 \text{ V}$$

Applying KVL we have

$$10 \text{ V} - 0.7 \text{ V} - I_D\,[10 \text{ k}\Omega] = 0$$

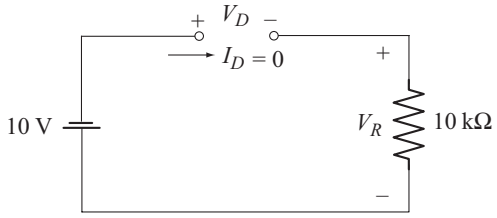
$$I_D = \frac{9.3 \text{ V}}{10 \text{ k}\Omega} = 0.93 \text{ mA}$$

$$V_R = I_D\,(10 \text{ k}\Omega)$$

$$= (0.93 \text{ mA})\,(10 \text{ k}\Omega)$$

$$= 9.3 \text{ V}$$

(b) If the battery polarity is reversed, the diode gets reverse biased and hence it acts as an open circuit as shown below.



$$I_D = 0 \text{ mA}$$

$$V_R = I_D\,(10 \text{ k}\Omega) = 0 \text{ V}$$

Writing KVL equation we get

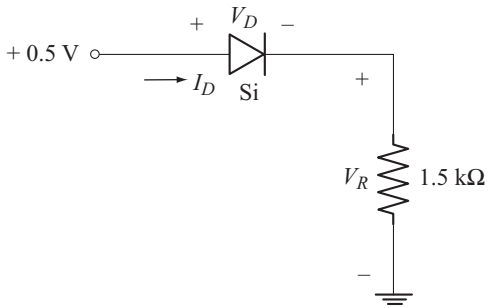
$$-10\text{ V} - V_D - I_D\,(10\text{ k}\Omega) = 0$$

$$\Rightarrow \qquad V_D = -10\text{ V}$$

Note that the diode is reverse biased to the level of – 10 V.

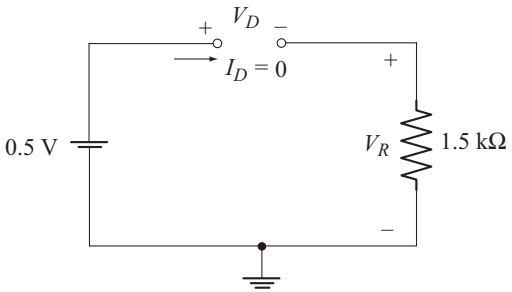
Example 1.7

For the circuit shown find I_D, V_D and V_R.



Solution

The applied forward voltage is only 0.5 V which is less than $V_K = 0.7$ V. Hence the diode does not conduct and it acts as an open circuit as shown below.



$$I_D = 0\text{ mA}$$

$$V_R = I_D\,(1.5\text{ k}\Omega) = 0\text{ V}$$

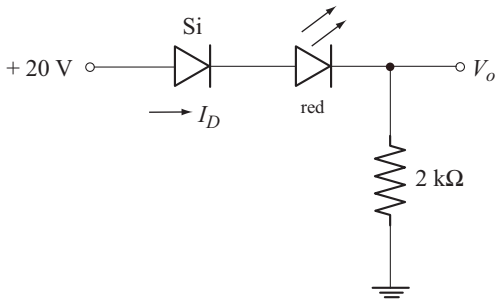
Applying KVL we get

$$0.5\text{ V} - V_D - I_D\,(1.5\text{ k}\Omega) = 0$$

$$\Rightarrow \qquad V_D = 0.5\text{ V}.$$

Example 1.8

For the circuit shown below determine V_o and I_D. Assume $V_K = 1.6$ V for the red LED.

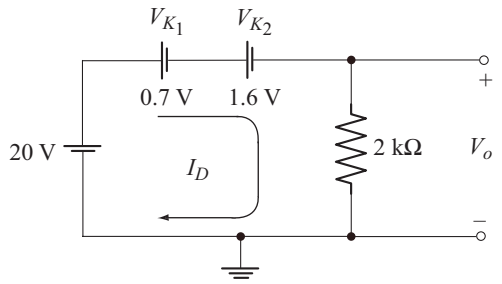


Solution

Both diodes conduct in the same direction. Since both are in series, the total knee voltage is

$$\begin{aligned} V_K &= V_{K_1} + V_{K_2} \\ &= 0.7 \text{ V} + 1.6 \text{ V} \\ &= 2.3 \text{ V}. \end{aligned}$$

Both diodes are turned on since the applied voltage is more than 2.3 V. The equivalent circuit is shown below.



Applying KVL we have

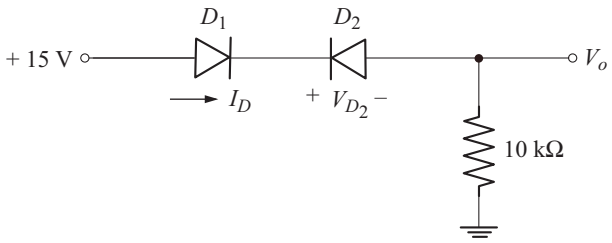
$$20 \text{ V} - 0.7 \text{ V} - 1.6 \text{ V} - I_D\,(2 \text{ k}\Omega) = 0$$

$$I_D = \frac{17.7 \text{ V}}{2 \text{ k}\Omega} = 8.85 \text{ mA}$$

$$\begin{aligned} V_D &= I_D\,(2 \text{ k}\Omega) \\ &= (8.85 \text{ mA})\,(2 \text{ k}\Omega) \\ &= 17.7 \text{ V} \end{aligned}$$

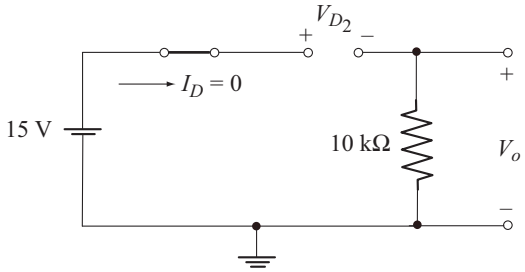
Example 1.9

For the circuit shown below determine I_D, V_{D_2} and V_o. D_1 and D_2 are both silicon diodes.



Solution

The applied voltage forward biases D_1 but reverse biases D_2. The current in the circuit is zero since D_2 acts as an open circuit. Though D_1 is forward biased, its current is zero. Hence we have to replace D_1 by short circuit instead of V_K. The equivalent circuit is shown below.



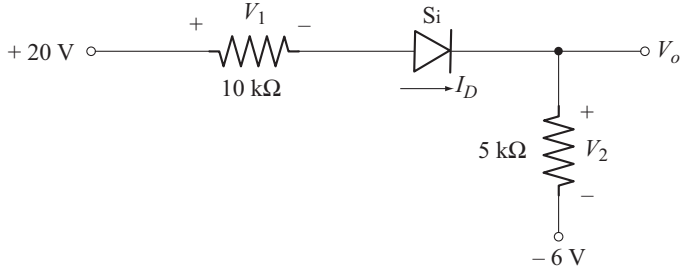
$$I_D = 0 \text{ mA}$$
$$V_0 = I_D\,(10\ \text{k}\Omega) = 0 \text{ V}$$

Applying KVL we have

$$15 \text{ V} - V_{D_2} - V_o = 0$$
$$V_{D_2} = 15 \text{ V}$$

Example 1.10

For the circuit shown below determine I_D, V_1, V_2 and V_o.



Solution

The diode is in the on state since the anode has positive potential and the cathode negative potential. The equivalent circuit is shown below.

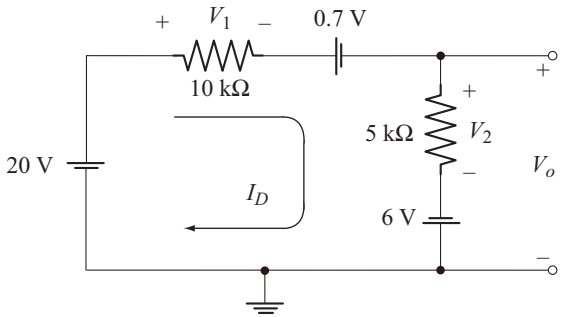


Fig. A

Applying KVL to the circuit of Fig. A, we get

$$20\text{ V} - 10\text{ k}\Omega\,(I_D) - 0.7\text{ V} - 5\text{ k}\Omega\,(I_D) + 6\text{ V} = 0$$

$$I_D = \frac{26\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega + 5\text{ k}\Omega} = 1.68\text{ mA}$$

$$V_1 = I_D\,(10\text{ k}\Omega) = (1.68\text{ mA})\,(10\text{ k}\Omega) = 16.8\text{ V}$$

$$V_2 = I_D\,(5\text{ k}\Omega) = (1.68\text{ mA})\,(5\text{ k}\Omega) = 8.4\text{ V}$$

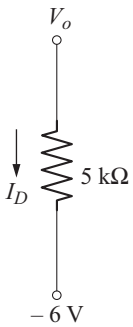


Fig. B

From the circuit of Fig. B

$$I_D = \frac{V_o - (-6\text{ V})}{5\text{ k}\Omega}$$

$$\Rightarrow \quad V_o = I_D\,(5\text{ k}\Omega) - 6\text{ V} = (1.68\text{ mA})\,(5\text{ k}\Omega) - 6\text{ V} = 2.4\text{ V}$$

Alternatively, applying KVL to the path consisting of V_o, V_2 and 6 V battery we have

$$V_o - V_2 + 6\text{ V} = 0$$
$$V_o = V_2 - 6\text{ V} = 8.4\text{ V} - 6\text{ V} = 2.4\text{ V}$$

Example 1.11

For each of the following circuits determine the current *I*. Assume silicon diodes.

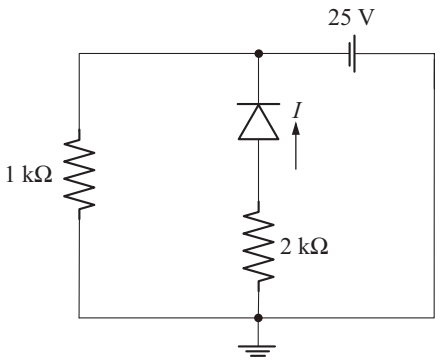


Fig. A

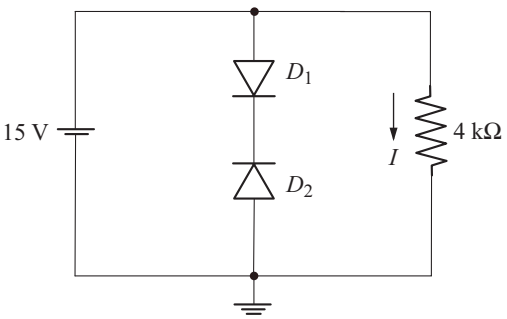
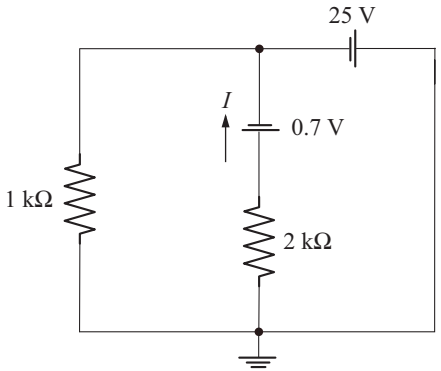


Fig. B

Solution

To find I in the circuit of Fig. A

The diode is in the on state. The equivalent circuit is shown below.

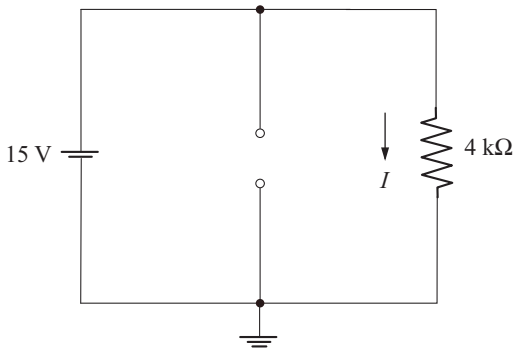


Applying KVL to the second loop we have

$$-I\,(2\text{ k}\Omega) - 0.7\text{ V} + 25\text{ V} = 0$$
$$I = \frac{25\text{ V} - 0.7\text{ V}}{2\text{ k}\Omega} = 12.15\text{ mA}$$

To find I in the circuit of Fig. B

Since D_2 is reverse biased, the diode branch can be treated as an open circuit. The equivalent circuit is shown below.



$$I = \frac{15\text{ V}}{4\text{ k}\Omega} = 3.75\text{ mA}$$

Example 1.12

Determine V_o and I_D for the circuits shown below.

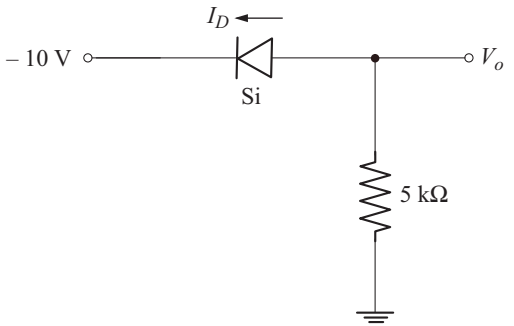


Fig. A

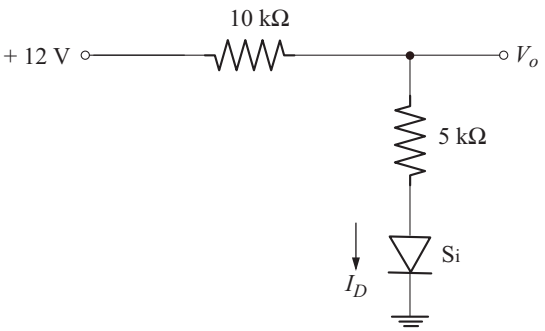
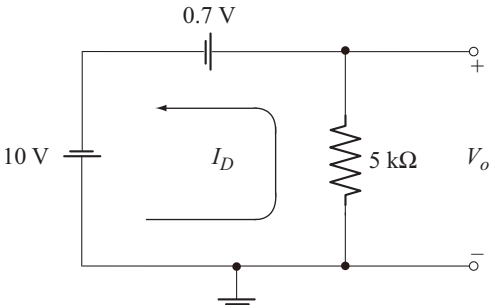


Fig. B

Solution

To find I_D and V_o for the circuit of Fig. A

The diode is in the on state. The equivalent circuit is shown below.



Writing KVL equation we have

$$-10\text{ V} + 0.7\text{ V} + I_D\,(5\text{ k}\Omega) = 0$$

$$I_D = \frac{9.3\text{ V}}{5\text{ k}\Omega} = 1.86\text{ mA}$$

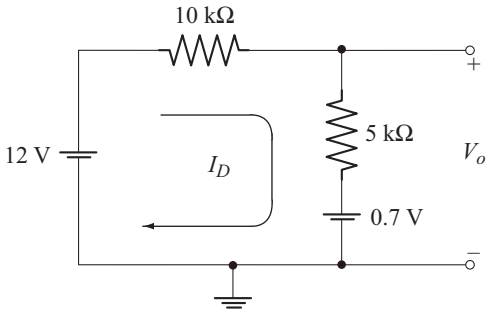
Rewriting KVL equation using V_o we have

$$-10\text{ V} + 0.7\text{ V} - V_o = 0$$

$$V_o = -9.3\text{ V}$$

To find I_D and V_o for the circuit of Fig. B

The diode is in the on state. The equivalent circuit is given below.



Writing KVL equation we have

$$12\text{ V} - I_D\,[10\text{ k}\Omega + 5\text{ k}\Omega] - 0.7\text{ V} = 0$$

$$I_D = \frac{11.3\text{ V}}{15\text{ k}\Omega} = 0.753\text{ mA}$$

Rewriting KVL equation using V_o we have

$$12\text{ V} - I_D\,(10\text{ k}\Omega) - V_o = 0$$

$$V_o = 12\text{ V} - I_D\,(10\text{ k}\Omega) = 4.47\text{ V}$$

Alternate method

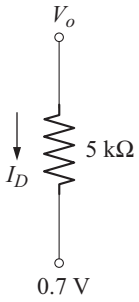


Fig. C

From Fig. C

$$I_D = \frac{V_o - 0.7\ \text{V}}{5\ \text{k}\Omega}$$

$$\Rightarrow \quad V_o = I_D\,(5\ \text{k}\Omega) + 0.7\ \text{V}$$

$$= 4.47\ \text{V}$$

Example 1.13

For the circuits shown determine V_o and I_D.

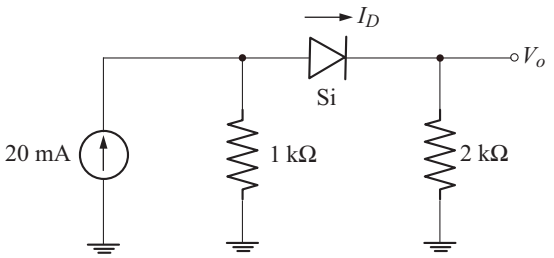


Fig. A

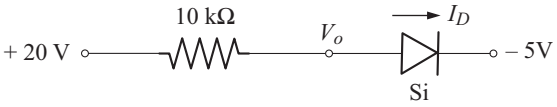
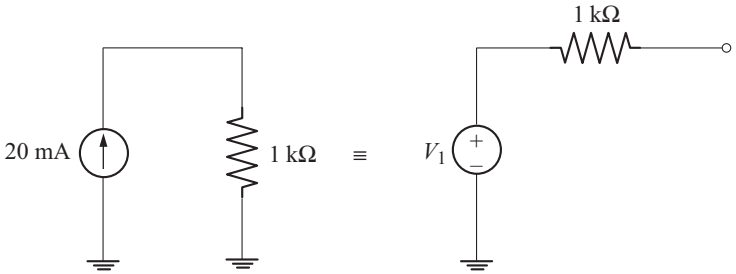


Fig. B

Solution

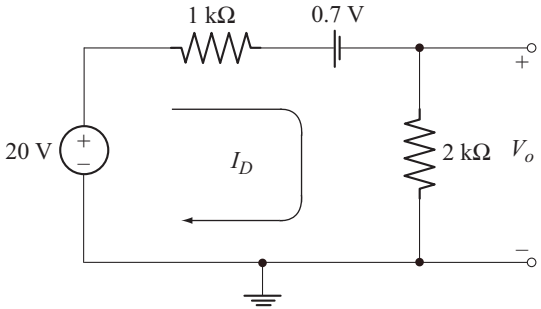
To find I_D and V_o for the circuit of Fig. A

Let us convert the current source into its equivalent voltage source.



$$V_1 = (20\ \text{mA})\,(1\ \text{k}\Omega) = 20\ \text{V}$$

The resulting circuit is shown below



Applying KVL we get

$$20\text{ V} - I_D\,(1\text{ k}\Omega) - 0.7\text{ V} - I_D\,(2\text{ k}\Omega) = 0$$

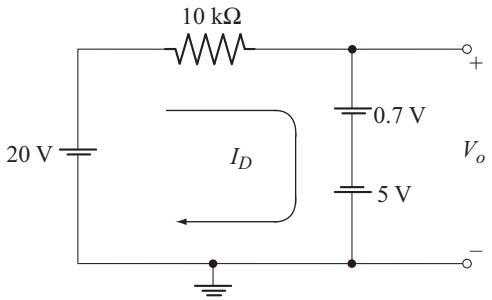
$$I_D = \frac{19.3\text{ V}}{3\text{ k}\Omega} = 6.43\text{ mA}$$

$$V_o = I_D\,(2\text{ k}\Omega)$$

$$= (6.43\text{ mA})\,(2\text{ k}\Omega) = 12.86\text{ V}$$

To find V_o and I_D for the circuit of Fig. B

The diode is in the conducting state. The equivalent circuit is shown below.



Writing KVL equation, we have

$$20\text{ V} - I_D\,(10\text{ k}\Omega) - 0.7\text{ V} + 5\text{ V} = 0$$

$$I_D = \frac{24.3\text{ V}}{10\text{ k}\Omega} = 2.43\text{ mA}$$

Again writing KVL equation using V_o, we have

$$20\text{ V} - I_D\,(10\text{ k}\Omega) - V_o = 0$$

$$V_o = 20\text{ V} - (2.43\text{ mA})\,(10\text{ k}\Omega) = -4.3\text{ V}$$

Example 1.14

For the circuits shown below determine I_D, V_{o_1} and V_{o_2}.

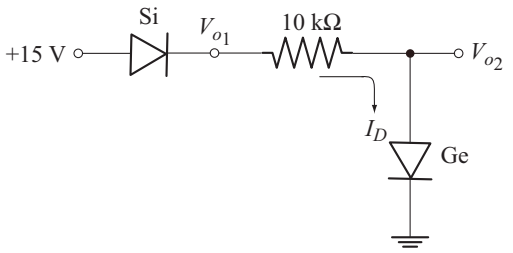


Fig. A

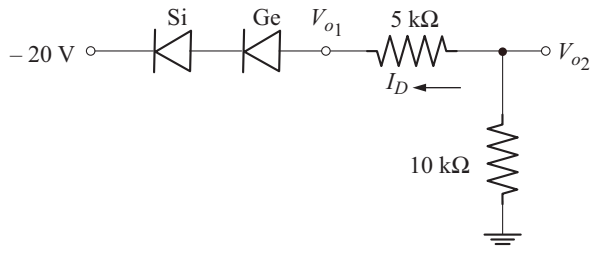
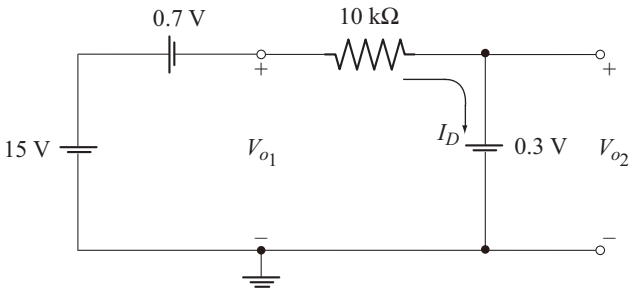


Fig. B

Solution

I_D, V_{o_1} and V_{o_2} for the circuit of Fig. A

Both diodes are in the conducting state. The equivalent circuit is shown below.



Applying KVL we have

$$15\text{ V} - 0.7\text{ V} - I_D\,(10\text{ k}\Omega) - 0.3\text{ V} = 0$$

$$I_D = \frac{14\text{ V}}{10\text{ k}\Omega} = 1.4\text{ mA}$$

$$V_{o_2} = 0.3\text{ V}$$

Writing KVL equation to the left part of the circuit we get

$$15\text{ V} - 0.7\text{ V} - V_{o_1} = 0$$

$$V_{o_1} = 14.3\text{ V}$$

Alternatively,

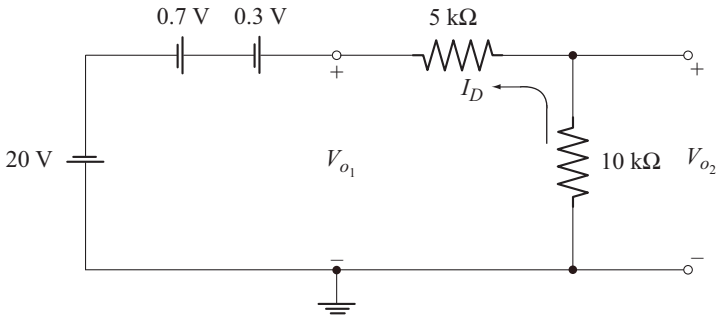
$$I_D = \frac{V_{o_1} - V_{o_2}}{10\text{ k}\Omega}$$

$$\Rightarrow \quad V_{o_1} = I_D\,(10\text{ k}\Omega) + V_{o_2}$$

$$= (1.4\text{ mA})\,(10\text{ k}\Omega) + 0.3\text{ V} = 14.3\text{ V}$$

I_D, V_{o_1} and V_{o_2} for the circuit of Fig. B

Both diodes are in the conducting state. The equivalent circuit is shown below.



KVL equation to the circuit is

$$-20\text{ V} + 0.7\text{ V} + 0.3\text{ V} + I_D\,[5\text{ k}\Omega + 10\text{ k}\Omega] = 0$$

$$I_D = \frac{19\text{ V}}{15\text{ k}\Omega} = 1.26\text{ mA}$$

KVL equation to the left part of the circuit is

$$-20\text{ V} + 0.7\text{ V} + 0.3\text{ V} - V_{o_1} = 0$$

$$V_{o_1} = -19\text{ V}$$

$$V_{o_2} = -I_D\,(10\text{ k}\Omega) = -(1.26\text{ mA})\,(10\text{ k}\Omega) = -12.6\text{ V}$$

Example 1.15

Determine I_D, I_o, and V_o for the circuits shown below.

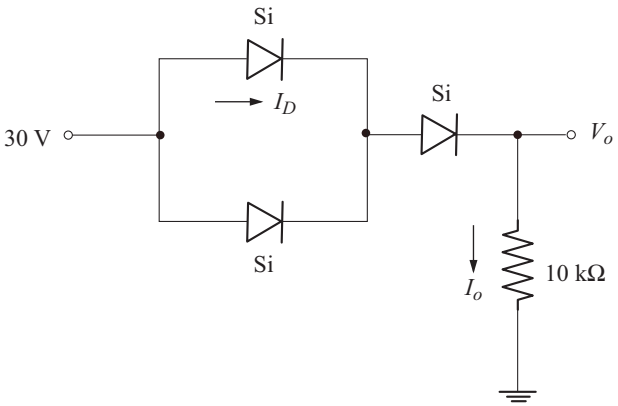


Fig. A

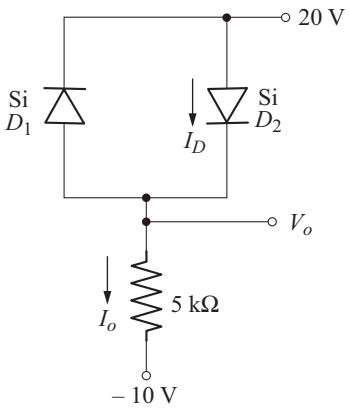
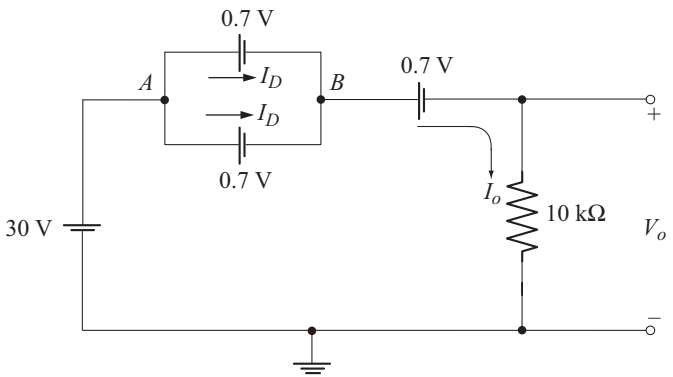


Fig. B

Solution

I_D, I_o and V_o for the circuit of Fig. A

All diodes are in the conducting state. The equivalent circuit is shown below.



Voltage between points A and B is 0.7 V.

Also $$I_o = 2I_D$$

KVL equation to the circuit is

$$30 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V} - I_o (10 \text{ k}\Omega) = 0$$

$$I_o = \frac{28.6 \text{ V}}{10 \text{ k}\Omega} = 2.86 \text{ mA}$$

$$I_D = \frac{I_o}{2} = 1.43 \text{ mA}$$

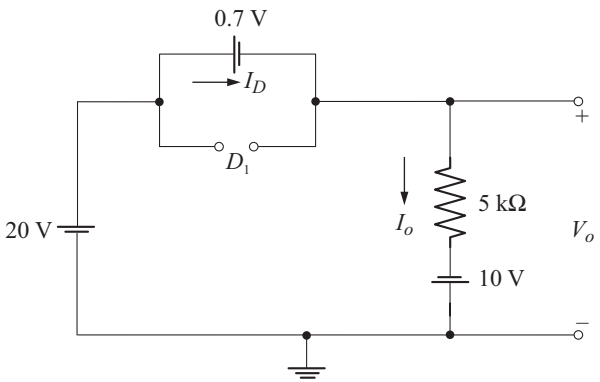
$$V_o = I_o (10 \text{ k}\Omega)$$

$$= (2.86 \text{ mA}) (10 \text{ k}\Omega)$$

$$= 28.6 \text{ V}$$

I_D, I_o and V_D for the circuit of Fig. B

D_1 is off and D_2 is in the conducting state. The equivalent circuit is shown below.



Note that, $I_o = I_D$

KVL equation to the circuit is

$$20 \text{ V} - 0.7 \text{ V} - I_o (5 \text{ k}\Omega) + 10 \text{ V} = 0$$

$$I_o = \frac{29.3 \text{ V}}{5 \text{ k}\Omega} = 5.86 \text{ mA}$$

Rewriting KVL equation using V_o,

$$20 \text{ V} - 0.7 \text{ V} - V_o = 0$$

$$V_o = 19.3 \text{ V}$$

Alternatively: [Refer Fig. C]

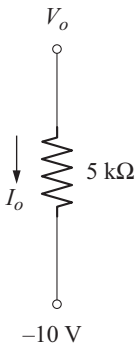


Fig. C

$$I_o = \frac{V_o - (-10\text{ V})}{5\text{ k}\Omega}$$

$$\Rightarrow \quad V_o = I_o\,(5\text{ k}\Omega) - 10\text{ V}$$

$$= 5.86\text{ mA}\,(5\text{ k}\Omega) - 10\text{ V} = 19.3\text{ V}$$

Example 1.16

For the circuits shown below calculate V_o and I.

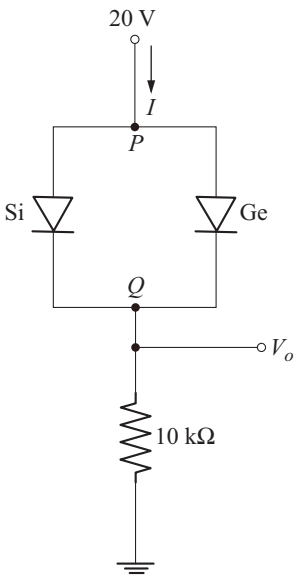


Fig. A

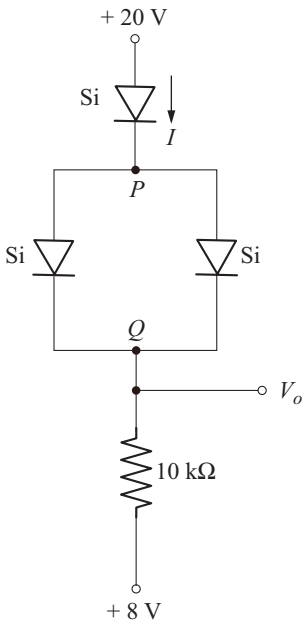
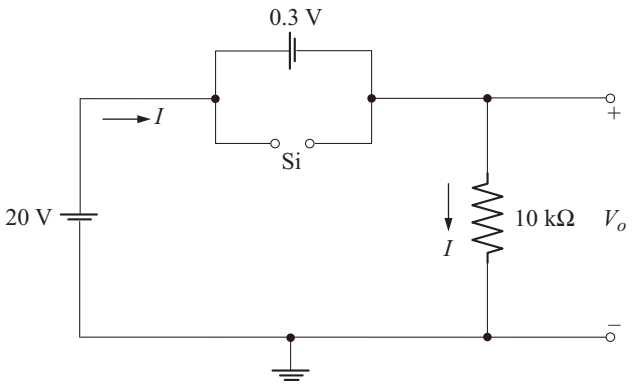


Fig. B

Solution

I and V_o for the Circuit of Fig. A

Ge diode conducts and as a result the voltage between points *P* and *Q* is 0.3 V. This voltage is not adequate to turn on Si diode. Hence Si diode is permanently off and the Ge diode is permanently on. The equivalent circuit is shown below.



KVL equation to the circuit is

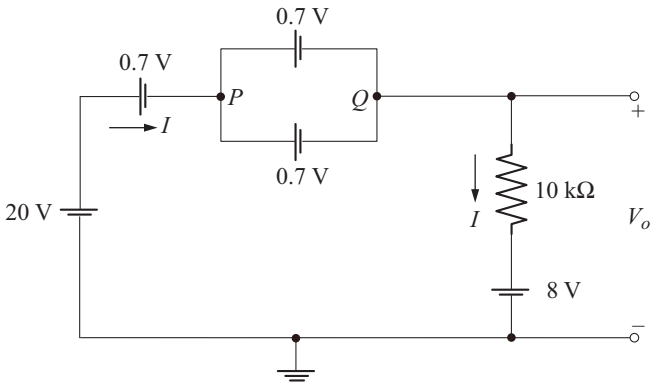
$$20\text{ V} - 0.3\text{ V} - I\,(10\text{ k}\Omega) = 0$$

$$I = \frac{19.7\text{ V}}{10\text{ k}\Omega} = 1.97\text{ mA}$$

$$V_o = I\,(10\text{ k}\Omega) = (1.97\text{ mA})\,(10\text{ k}\Omega) = 19.7\text{ V}$$

I and V_o for the Circuit of Fig. B

All diodes are in the conducting state. The equivalent circuit is shown below.



KVL equation to the circuit is

$$20\text{ V} - 0.7\text{ V} - 0.7\text{ V} - I\,(10\text{ k}\Omega) - 8\text{ V} = 0$$

$$I = \frac{10.6\text{ V}}{10\text{ k}\Omega} = 1.06\text{ mA}$$

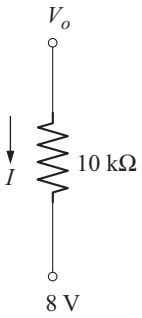


Fig. C

From Fig. C

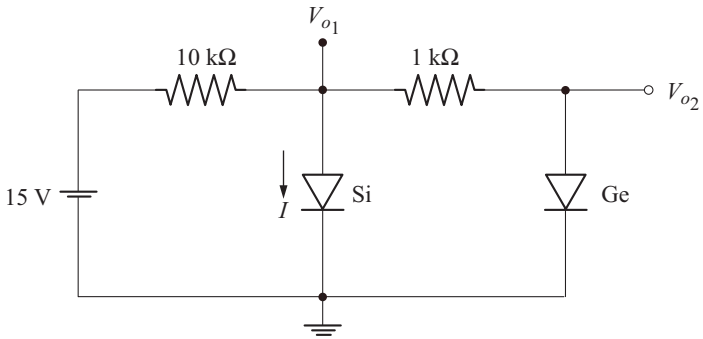
$$I = \frac{V_o - 8\text{ V}}{10\text{ k}\Omega}$$

$$\Rightarrow \quad V_o = I\,(10\text{ k}\Omega) + 8\text{ V}$$

$$= (1.06\text{ mA})\,(10\text{ k}\Omega) + 8\text{ V} = 18.6\text{ V}$$

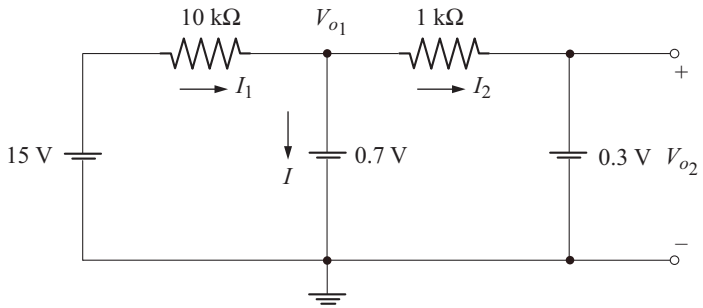
Example 1.17

For the circuit shown below determine V_{o_1}, V_{o_2} and I.



Solution

Both diodes are in the conducting state. The equivalent circuit is shown below.



From the equivalent circuit

$$V_{o_1} = 0.7 \text{ V} \quad \text{and} \quad V_{o_2} = 0.3 \text{ V}$$

KCL equation at the node V_{o_1} is

$$I_1 - I - I_2 = 0 \tag{A}$$

$$I_1 = \frac{15 \text{ V} - V_{o_1}}{10 \text{ k}\Omega} = \frac{15 \text{ V} - 0.7 \text{ V}}{10 \text{ k}\Omega} = 1.43 \text{ mA}$$

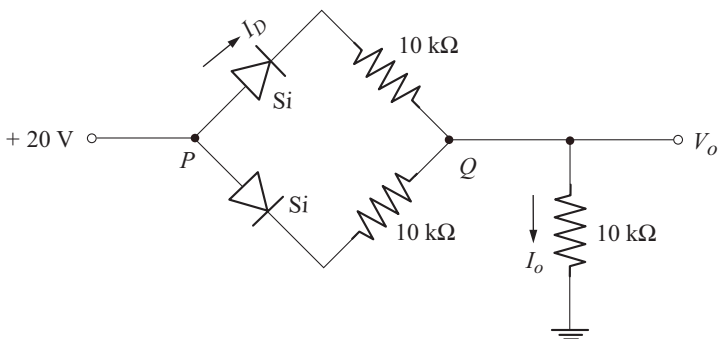
$$I_2 = \frac{V_{o_1} - V_{o_2}}{1 \text{ k}\Omega} = \frac{0.7 \text{ V} - 0.3 \text{ V}}{1 \text{ k}\Omega} = 0.4 \text{ mA}$$

Now from Equation (A),

$$I = 1.43 \text{ mA} - 0.4 \text{ mA} = 1.03 \text{ mA}$$

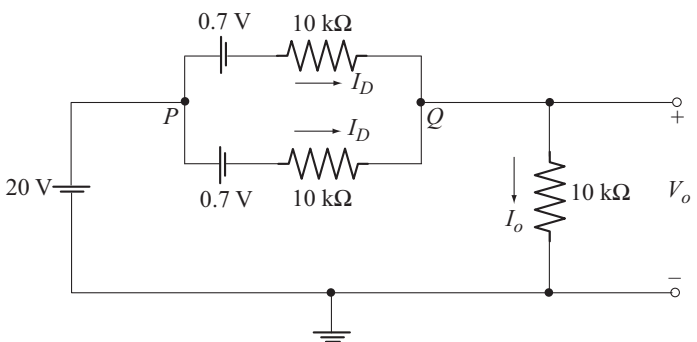
Example 1.18

For the circuit shown below calculate I_D, I_o and V_o.



Solution

Both diodes are in the conducting state. The equivalent circuit is shown below.



$$I_o = 2 I_D$$

KVL equation to the circuit is

$$20\text{ V} - 0.7\text{ V} - I_D(10\text{ k}\Omega) - I_o(10\text{ k}\Omega) = 0$$

$$I_D[10\text{ k}\Omega + 2(10\text{ k}\Omega)] = 19.3\text{ V}$$

$$I_D = 0.643\text{ mA}$$

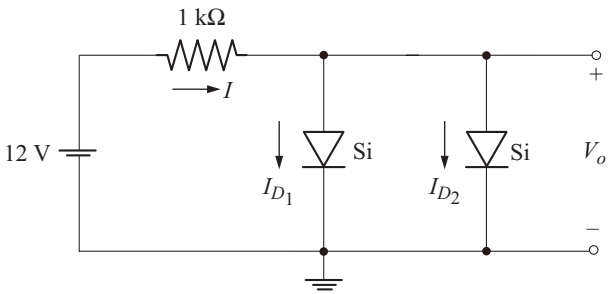
$$I_o = 2(0.643\text{ mA}) = 1.286\text{ mA}$$

$$V_o = I_o(10\text{ k}\Omega)$$

$$= (1.286\text{ mA})(10\text{ k}\Omega) = 12.86\text{ V}$$

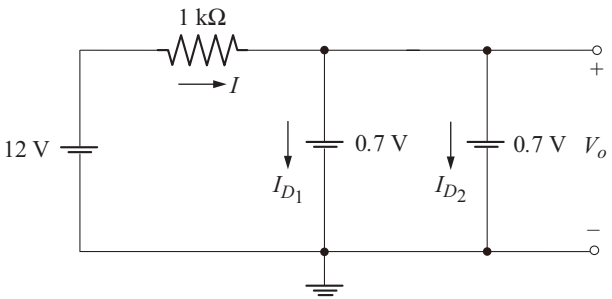
Example 1.19

For the circuit shown calculate V_o, I_{D_1}, I_{D_2} and I.



Solution

Both diodes are in the conducting state. The equivalent circuit is shown below.



From the equivalent circuit

$$V_o = 0.7\text{ V}$$

Also $$I_{D_1} = I_{D_2}$$

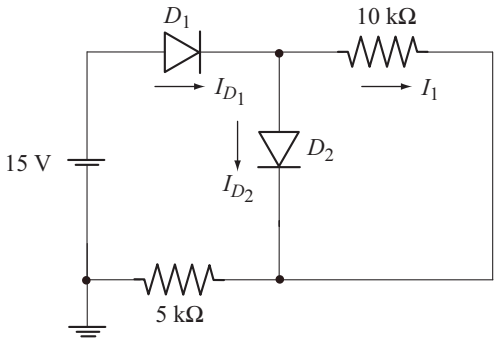
$\therefore$ $$I = 2I_{D_1} = 2I_{D_2}$$

$$I = \frac{12\text{ V} - V_o}{1\text{ k}\Omega} = \frac{12\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = 11.3\text{ mA}$$

$$I_{D_1} = I_{D_2} = \frac{I}{2}$$
$$= 5.65 \text{ mA}$$

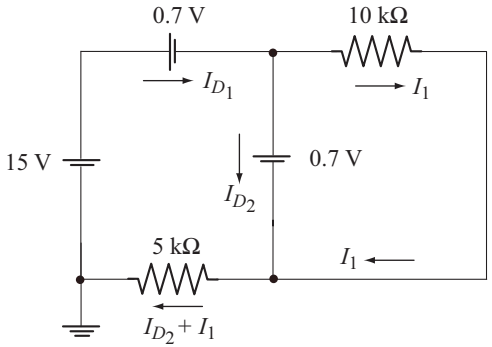
Example 1.20

For the circuit shown below calculate I_{D_1}, I_{D_2} and I_1. Both are Si diodes.



Solution

Both diodes are in the conducting state. The equivalent circuit is shown below.



$$I_{D_1} = I_1 + I_{D_2} \quad \text{(A)}$$

KVL equation to the second loop is

$$0.7 \text{ V} - I_1 (10 \text{ k}\Omega) = 0$$
$$I_1 = \frac{0.7 \text{ V}}{10 \text{ k}\Omega} = 0.07 \text{ mA}$$

KVL equation to the first loop is

$$15 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V} - 5 \text{ k}\Omega \, [I_{D_2} + I_1] = 0$$
$$I_{D_2} + I_1 = \frac{13.6 \text{ V}}{5 \text{ k}\Omega} = 2.72 \text{ mA}$$

$$I_{D_2} = 2.72 \text{ mA} - I_1$$
$$= 2.72 \text{ mA} - 0.07 \text{ mA} = 2.65 \text{ mA}$$

From Equation (A)

$$I_{D_1} = 0.07 \text{ mA} + 2.65 \text{ mA} = 2.72 \text{ mA}$$

1.13 RECTIFIERS

Rectifiers convert alternating current in to direct current. Since semiconductor diodes conduct current in the forward direction and blocks current in the reverse direction they can be employed for rectification. Most of the electronic systems require a dc voltage in the range of 5 V to 30 V for the proper operation of their internal circuits. Hence it is essential to convert ac to dc.

1.14 HALF-WAVE RECTIFIER

Half-wave rectifier converters only one half cycle of ac signal in to dc. Figure 1.18 shows the circuit of half wave rectifier supplying the load *R*.

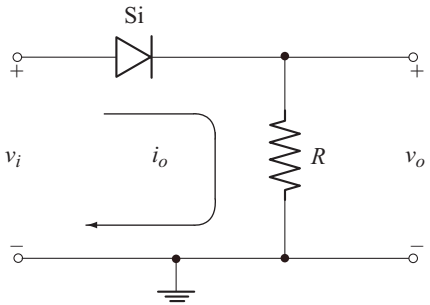


Fig. 1.18 Half-wave rectifier

v_i is the ac input voltage given by

$$v_i = V_m \sin \omega t \tag{1.24}$$

During the positive half cycle of ac input, the diode conducts when $v_i \geq V_K$. The equivalent circuit when the diode is conducting is shown in Fig. 1.19.

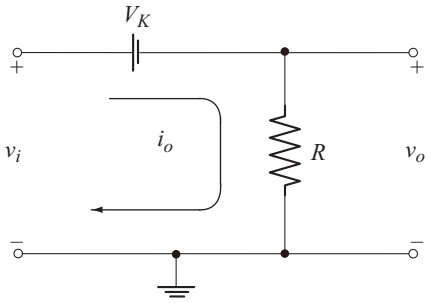


Fig. 1.19 Equivalent Circuit when the diode conducts

The KVL equation to the circuit of Fig. 1.19 is

$$v_i - V_K - v_o = 0$$

$$v_o = v_i - V_K \tag{1.25}$$

When the input signal is at its peak level V_m, the peak level of the output from Equation (1.25) is

$$V_{om} = V_m - V_K$$

Neglecting the time taken for the input signal to reach the level V_K, the output voltage when the diode is conducting can be described by the equation.

$$v_o = (V_m - V_K) \sin \omega t, \quad 0 \le \omega t \le \pi \tag{1.26}$$

The output current is given by

$$i_o = \frac{V_m - V_K}{R} \sin \omega t, \quad 0 \le \omega t \le \pi \tag{1.27}$$

When the input signal level falls below V_K, the diode stops conducting.

The equivalent circuit is shown in Fig 1.20. v_d represents the instantaneous reverse voltage across the non conducting diode.

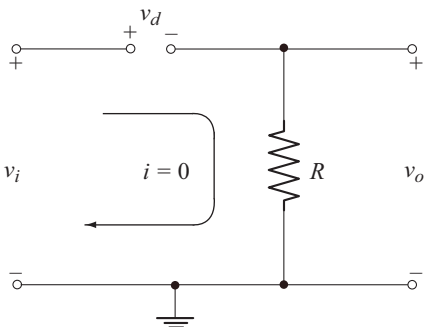


Fig. 1.20 Equivalent circuit during the negative half cycle of v_i

From the circuit of Fig 1.20, we find that

$$i_o = 0 \qquad \pi \le \omega t \le 2\pi \tag{1.28}$$

$$\therefore \quad v_o = i_o R = 0 \qquad \pi \le \omega t \le 2\pi \tag{1.29}$$

The waveforms of v_o and i_o are shown in Fig. 1.21.

Observe that both v_o and i_o are zero for $v_i \le V_K$. Since this interval is much smaller than the diode conduction time, it can be neglected.

Average (dc) Output Voltage [V_{dc}]

From Fig. 1.21 we note that the period of v_o is 2π. Hence its average or dc value is given by

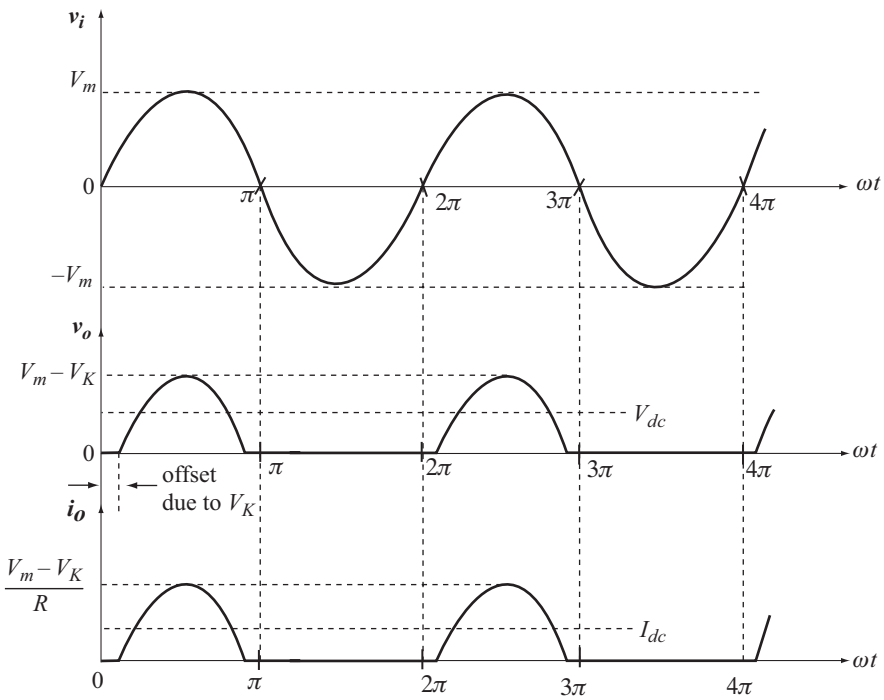


Fig. 1.21 Wave forms of v_i, v_o and i_o

$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} v_o \, d\omega t$$

$$= \frac{1}{2\pi}\int_0^{\pi} (V_m - V_K)\sin\omega t \, d\omega t$$

$$= \frac{V_m - V_K}{2\pi}\left[-\cos\omega t\right]_0^{\pi}$$

$$V_{dc} = \frac{1}{\pi}\left[V_m - V_K\right] \tag{1.30}$$

or $$V_{dc} = 0.318\,[V_m - V_K] \tag{1.31}$$

If $V_m \gg V_K$ or if the diode is ideal, $V_K = 0$

$$\therefore \quad V_{dc} = 0.318\,V_m \tag{1.32}$$

Average (dc) Output Current [I_{dc}]

Average or dc output current is given by

$$I_{dc} = \frac{V_{dc}}{R}$$

$$I_{dc} = 0.318 \frac{[V_m - V_K]}{R} \quad (1.33)$$

Average and Peak Diode Current

The diode current is same as the load current. Hence the average diode current equals the average load current.

i.e., $$I_{dc\ (diode)} = 0.318 \frac{[V_m - V_K]}{R} \quad (1.34)$$

From Equation (1.27), the peak diode current is

$$I_{dm} = \frac{V_m - V_K}{R} \quad (1.35)$$

Note that peak diode current is same as peak load current, I_{om}.

Peak Inverse Voltage [PIV]

Diode is subjected to reverse bias during the negative half cycle of v_i. Applying KVL to the circuit of Fig 1.20 we have

$$v_i - v_d - v_o = 0$$

Since $v_o = 0$ when the diode is not conducting, we have

$$v_d = v_i$$

v_d is the instantaneous reverse voltage on the diode. Reverse voltage is maximum when $v_i = V_m$. Hence the peak inverse voltage across the diode is

$$\text{PIV} = V_m \quad (1.36)$$

For safe operation, the PIV rating of the diode must be greater than V_m.

Power Dissipation in the Diode

The power dissipated in the diode is

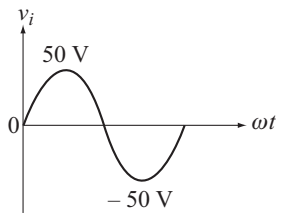
$$P_{diode} = V_K I_{dc\ (diode)} \quad (1.37)$$

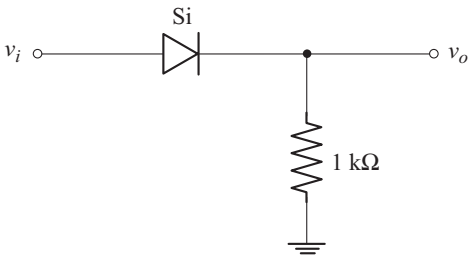
Example 1.21

For the circuit shown below calculate

(a) Average output voltage
(b) Average load current
(c) Average diode current
(d) Peak load current

(e) Peak diode current
(f) PIV of diode
(g) Power dissipation in diode





Solution

From the input voltage waveform.

$$V_m = 50 \text{ V}$$

(a) Average output voltage is

$$V_{dc} = 0.318 [V_m - V_K]$$
$$= 0.318 [50 \text{ V} - 0.7 \text{ V}] = 15.67 \text{ V}$$

(b) Average load current is

$$I_{dc} = \frac{V_{dc}}{R}$$
$$= \frac{15.67 \text{ V}}{1 \text{ k}\Omega} = 15.67 \text{ mA}$$

(c) Average diode current is

$$I_{dc\ (diode)} = I_{dc} = 15.67 \text{ mA}$$

(d) Peak load current is

$$I_{om} = \frac{V_m - V_K}{R}$$
$$= \frac{50 \text{ V} - 0.7 \text{ V}}{1 \text{ k}\Omega} = 49.3 \text{ mA}$$

(e) Peak diode current is

$$I_{dm} = I_{om} = 49.3 \text{ mA}$$

(g) Peak inverse voltage is

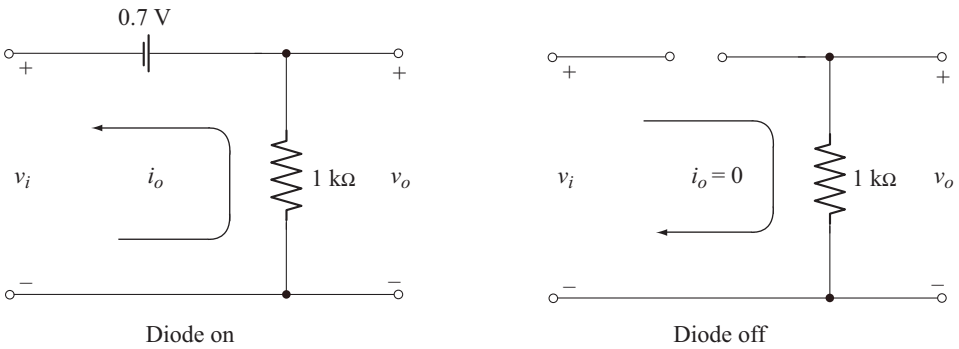
$$\text{PIV} = V_m = 50 \text{ V}$$

Example 1.22

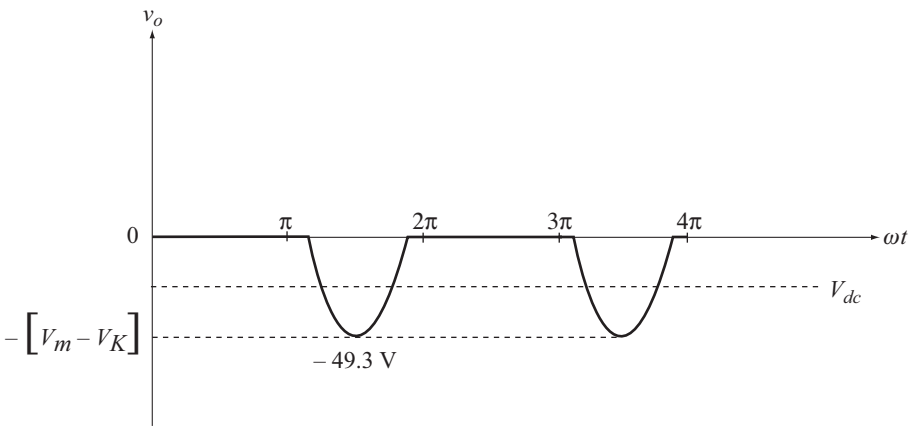
Repeat example 1.21 if the diode is reversed. Sketch the output voltage waveform.

Solution

When the diode connection is reversed, it conducts during the negative half cycle and is off during the positive half cycle. The equivalent circuits are shown below.



The output voltage waveform is shown below.



Note that the load current direction is reversed but the diode current flows from anode to cathode only. Therefore we have the following results.

$$V_{dc} = -15.67 \text{ V}$$

$$I_{dc} = -15.67 \text{ mA}$$

$$I_m = -49.3 \text{ mA}$$

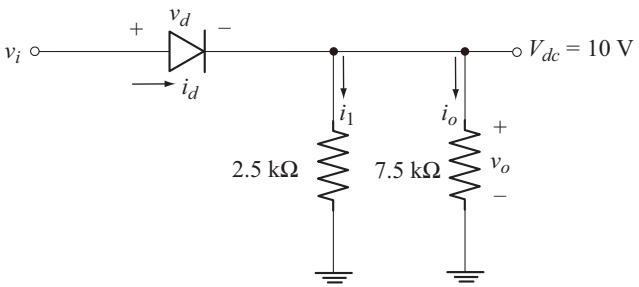
For the diode

$$I_{dc\,(\text{diode})} = 15.67 \text{ mA}$$

$$I_{dm} = 49.3 \text{ mA}$$
$$\text{PIV} = 50 \text{ V}$$

Example 1.23

For the circuit shown sketch the waveforms of i_d, v_d, v_o and i_o. Assume Si diode.



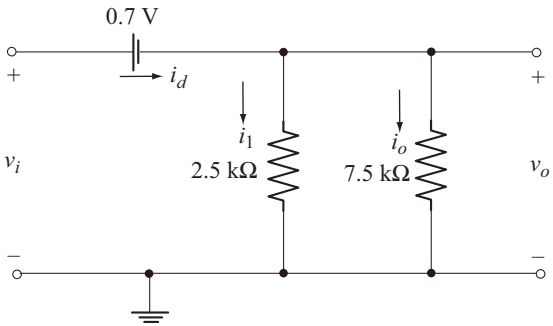
Solution

$$V_{dc} = 0.318 [V_m - V_K]$$
$$10 \text{ V} = 0.318 [V_m - 0.7 \text{ V}]$$

Solving we get

$$V_m = 32.15 \text{ V}$$
$$\therefore \quad v_i = V_m \sin \omega t$$
$$= 32.15 \sin \omega t \text{ Volts}$$

The equivalent circuit when the diode is conducting is shown below.



Peak value of output voltage is

$$V_{om} = V_m - V_K$$
$$= 32.15 \text{ V} - 0.7 \text{ V}$$
$$= 31.45 \text{ V}$$
$$\therefore \quad v_o = 31.45 \sin \omega t \text{ V} \qquad \text{(A)}$$

$$i_o = \frac{v_o}{7.5\ \text{k}\Omega}$$

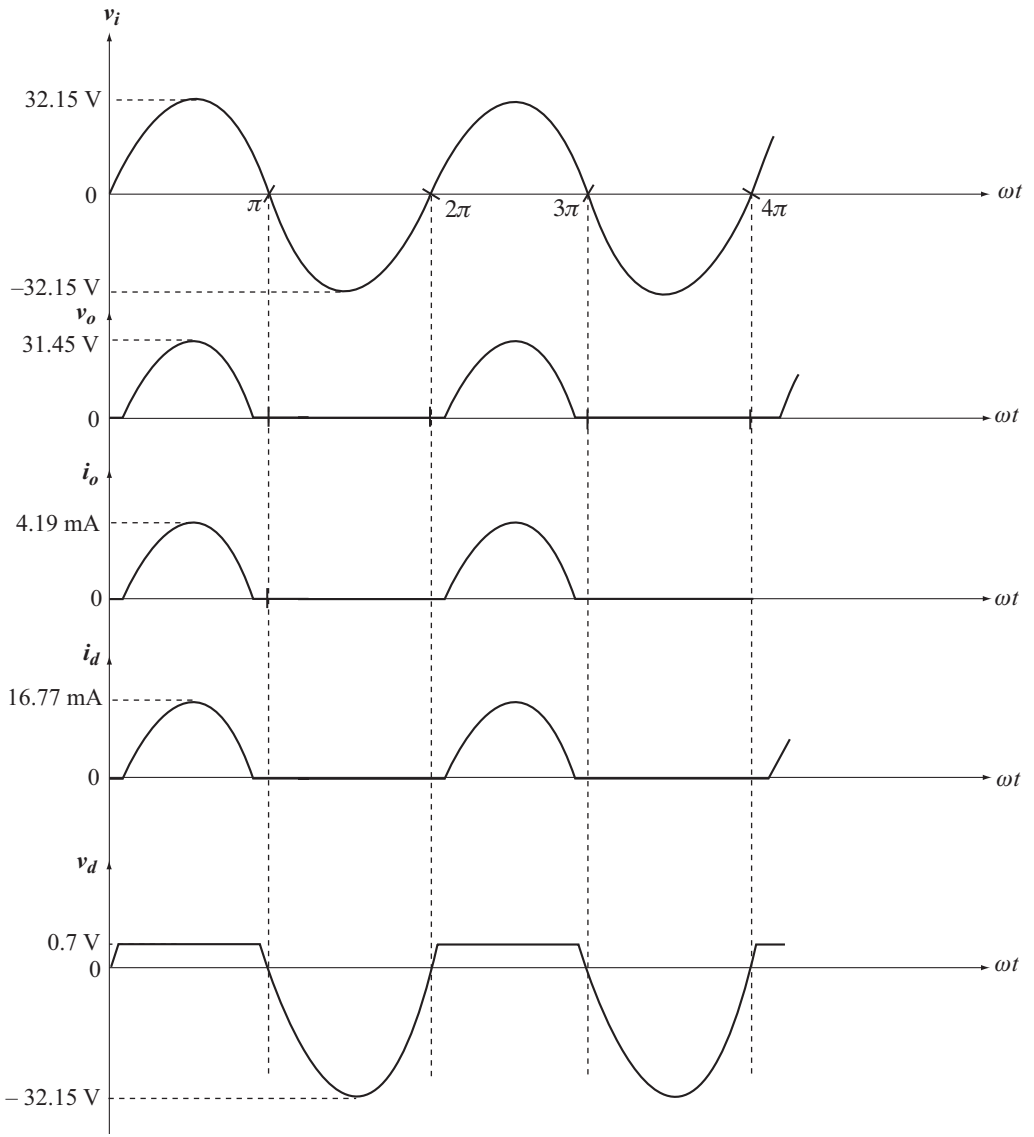
$$\therefore \quad i_o = 4.19 \sin \omega t \text{ mA} \qquad \text{(B)}$$

$$i_l = \frac{v_o}{2.5\ \text{k}\Omega} = 12.58 \sin \omega t \text{ mA}$$

$$i_d = i_l + i_o$$

$$= 16.77 \sin \omega t \text{ mA} \qquad \text{(C)}$$

The waveforms of i_d, v_d, v_o and i_o are shown below.



Note:

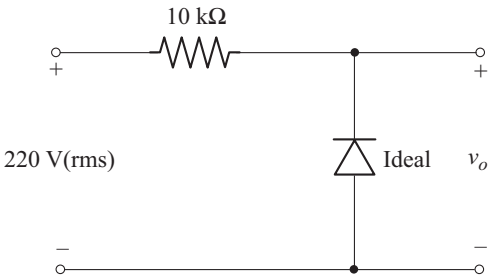
- If the diode is ideal, $V_K = 0$

$$\therefore \qquad V_{om} = V_m = 32.15 \text{ V}$$

- Without 2.5 kΩ resistor, $i_o = i_d$.

Example 1.24

For the circuit shown below sketch v_o and calculate V_{dc}.

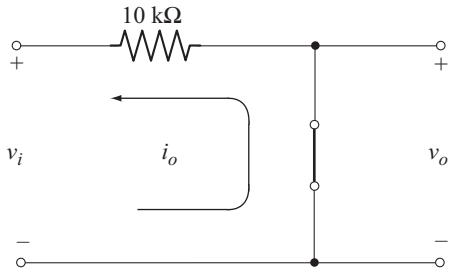


Solution

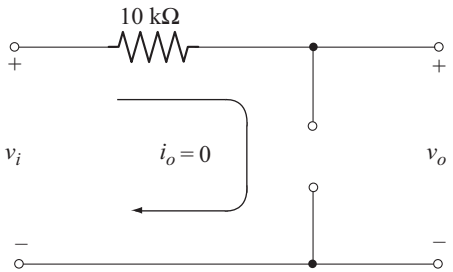
$$V_i = 220 \text{ V (rms)}$$
$$V_m = 220\sqrt{2} = 311.13 \text{ V}$$

Since the diode is ideal $V_K = 0$.

Diode conducts during the negative half cycle of v_i and is off during the positive half cycle. The equivalent circuits are shown below.



(a) Diode on

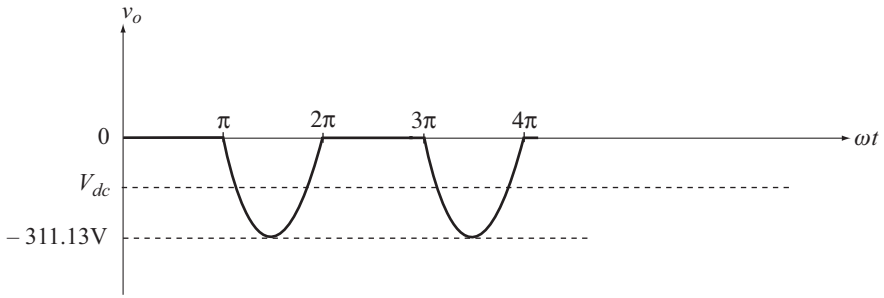


(b) Diode off

From the equivalent circuits we can write

$$v_o = \begin{cases} 0 & 0 \le \omega t \le \pi \\ v_i & \pi \le \omega t \le 2\pi \end{cases}$$

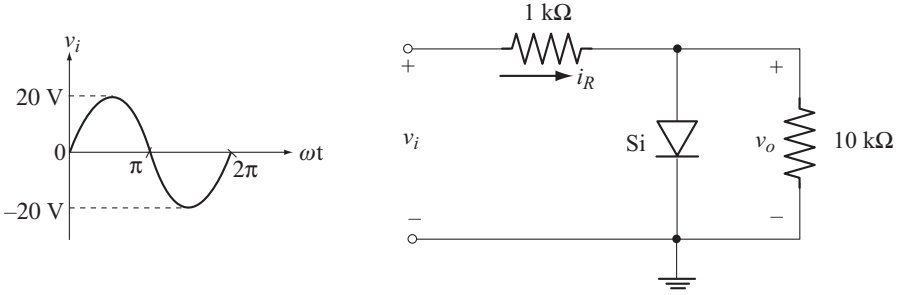
The waveform of v_o is shown below.



$$V_{dc} = -0.318\,[V_m - V_K]$$
$$= -0.318\,[311.13\ \text{V}] \quad [\text{since } V_K = 0]$$
$$= -98.94\ \text{V}$$

Example 1.25

For the circuit shown below sketch v_o and i_R.



Solution

The equivalent circuits are shown below.

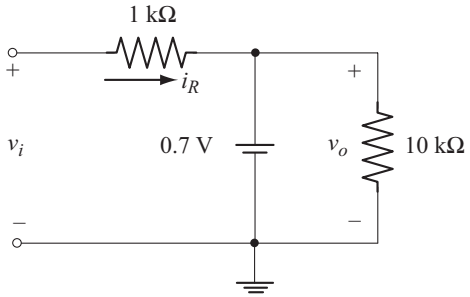


Fig. A Equivalent circuit during diode conduction

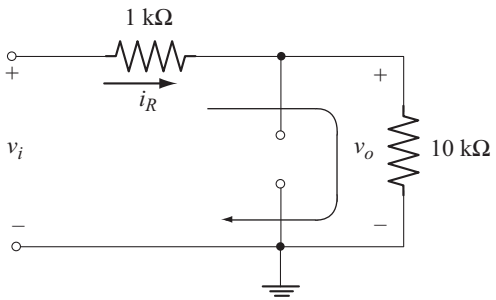


Fig. B Equivalent circuit when diode is off

***For* $0 \le \omega t \le \pi$**

Diode conducts. We refer the circuit of Fig. A

$$v_o = 0.7 \text{ V (constant)}$$

$$i_R = \frac{v_i - 0.7 \text{ V}}{1 \text{ k}\Omega}$$

When $v_i = V_m = 20$ V, the corresponding current is

$$I_{Rm} = \frac{20 \text{ V} - 0.7 \text{ V}}{1 \text{ k}\Omega} = 19.3 \text{ mA}$$

***For* $\pi \le \omega t \le 2\pi$**

Diode is off. We refer the circuit of Fig. B.

$$i_R = \frac{v_i}{1 \text{ k}\Omega + 10 \text{ k}\Omega}$$

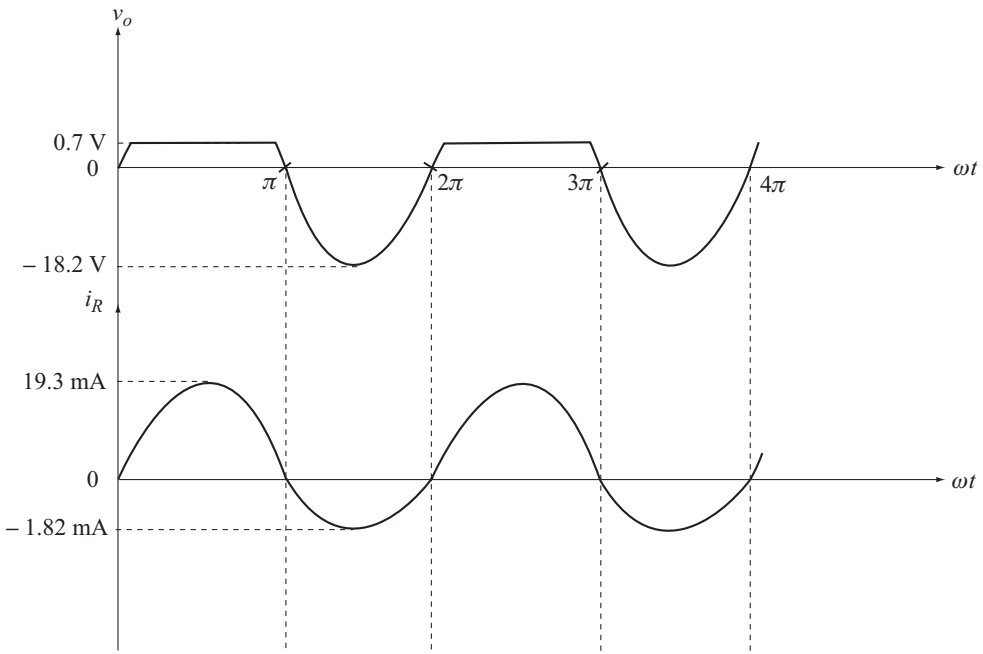
When $v_i = -20$ V

$$I_{Rm} = \frac{-20 \text{ V}}{11 \text{ k}\Omega} = -1.82 \text{ mA}$$

$$v_o = i_R (10 \text{ k}\Omega)$$

$$\Rightarrow \quad V_{om} = I_{Rm} (10 \text{ k}\Omega) = -18.2 \text{ V}$$

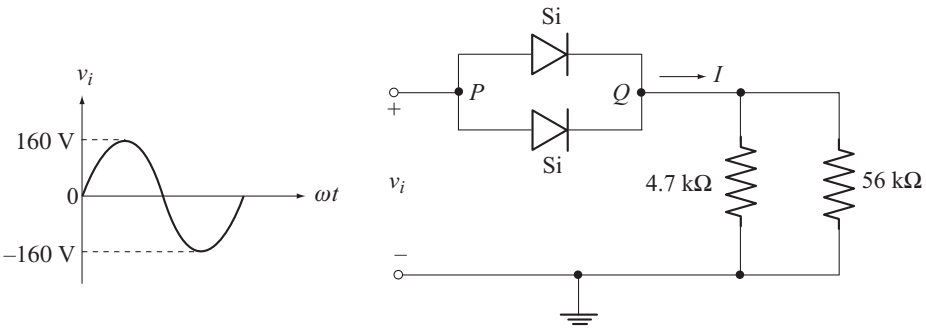
Wave forms of v_o and i_R are shown below.



Example 1.26

For the circuit shown below determine

(a) The maximum current rating of each diode if P_{max} for each diode is 14 mW.
(b) The maximum value of I.
(c) The maximum current through each diode.
(d) Check whether the diode current rating is exceeded.
(e) If one diode is removed, calculate the maximum current through other diode. Will this current be within the maximum current rating of diode?

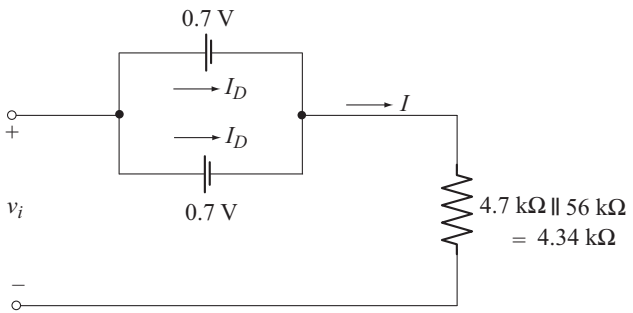


Solution

(a)
$$P_{max} = (0.7\text{ V})\, I_D$$
$$I_D = \frac{P_{max}}{0.7\text{ V}}$$
$$= \frac{14\text{ mW}}{0.7\text{ V}}$$
$$= 20\text{ mA}$$

Maximum forward current rating of each diode is 20 mA.

(b) Both diodes conduct during the positive half cycle of v_i. The equivalent circuit is shown below.



$$I = 2 I_D$$

KVL equation to the circuit is

$$v_i - 0.7 \text{ V} - I\,(4.34 \text{ k}\Omega) = 0$$

$$I = \frac{v_i - 0.7 \text{ V}}{4.34 \text{ k}\Omega}$$

Maximum value of I_m occurs when v_i is maximum.

$$\therefore \quad I_{\max} = \frac{160 \text{ V} - 0.7 \text{ V}}{4.34 \text{ k}\Omega} = 36.7 \text{ mA}$$

$$I_{D\max} = \frac{I_{\max}}{2} = 18.35 \text{ mA} = I_{dm}$$

(c) Note that $I_{D\max} < 20$ mA
$\therefore$ Diode current rating is not exceeded.

(d) With only one diode

$$I = I_D$$

$$\therefore \quad I_{\max} = I_{D\max} = 36.7 \text{ mA}$$

In this case the diode current rating is exceeded. The diode carries almost twice the rated current which is not safe.

◆ 1.15 FULL-WAVE BRIDGE RECTIFIER

Full wave rectifier converts both half cycle of ac signal in to dc. Figure 1.22 shows the circuit of full-wave bridge rectifier.

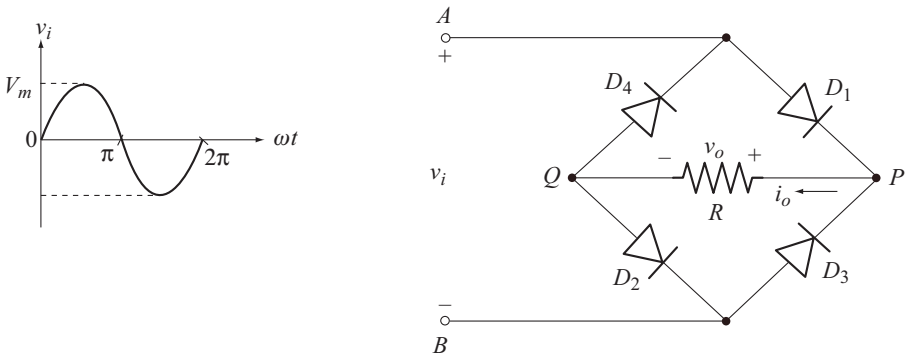


Fig. 1.22 Full-wave bridge rectifier

During the positive half cycle of v_i, diodes D_1 and D_2 are forward biased and D_3 and D_4 are reverse biased. The equivalent circuit is shown in Fig. 1.23(a). The current follows the path $A - D_1 - P - Q - D_2 - B - A$.

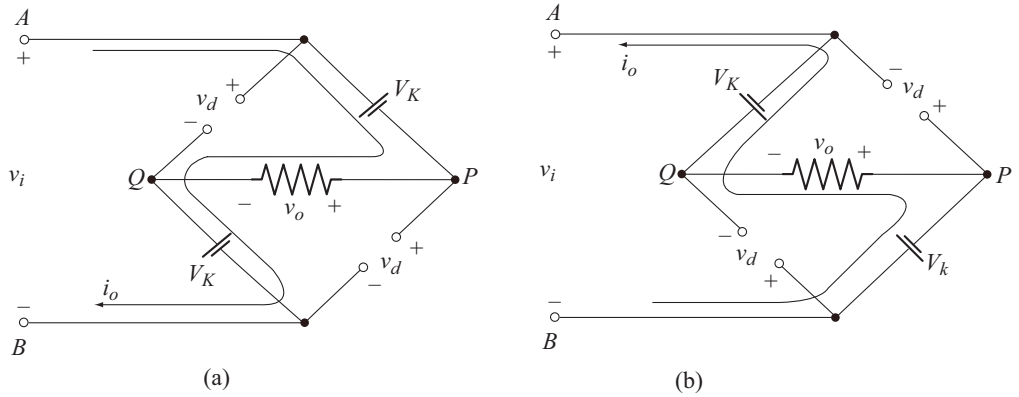


Fig. 1.23 Equivalent circuit during
(a) Positive half cycle of v_i
(b) Negative half cycle of v_i

Applying KVL to the current path indicated in Fig. 1.23 (a) we have

$$v_i - V_K - v_o - V_K = 0$$

$$v_o = v_i - 2V_K \tag{1.38}$$

When v_i is at its peak value V_m, the peak level of v_o is

$$V_{om} = V_m - 2V_K \tag{1.39}$$

Now the output voltage equation is

$$v_o = (V_m - 2V_K)\sin\omega t, \quad 0 \le \omega t \le \pi \tag{1.40}$$

The output current is

$$i_o = \frac{V_m - 2V_K}{R}\sin\omega t$$

or

$$i_o = I_{om}\sin\omega t, \quad 0 \le \omega t \le \pi \tag{1.41}$$

where I_{om} is the peak output / load current , given by

$$I_{om} = \frac{V_m - 2V_K}{R} \tag{1.42}$$

During the negative half cycle of v_i, diodes D_3 and D_4 conduct and D_1 and D_2 are reverse biased. The equivalent circuit is shown in Fig 1.23 (b). The current follows the path $B - D_3 - P - Q - D_4 - A - B$. Note that, during both half cycles of v_i, the load current i_o, flows from P to Q only. Hence i_o is undirectional or dc.

Equations (1.40) and (1.41) are also applicable for the interval $\pi \le \omega t \le 2\pi$. In Fig. 1.23 , v_d represents the instantaneous reverse voltage across the non conducting diodes. The waveforms of v_o and i_o are shown in Fig 1.24.

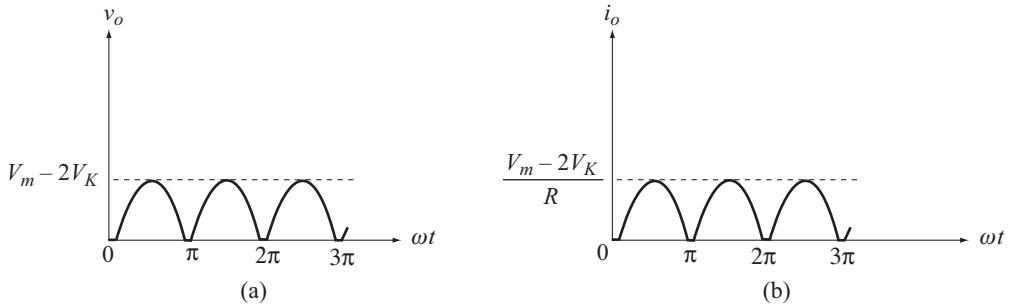


Fig. 1.24 Wave forms of v_o and i_o

Average (dc) Output Voltage [V_{dc}]

From Fig. 1.24 we note that the period of v_o is π. Hence the average or dc value is given by

$$V_{dc} = \frac{1}{\pi}\int_0^{\pi} v_o \, d\omega t$$

$$= \frac{1}{\pi}\int_0^{\pi} [V_m - 2V_K] \sin \omega t \, d\omega t$$

$$= \frac{V_m - 2V_K}{\pi} [-\cos \omega t]_0^{\pi}$$

$$V_{dc} = \frac{2[V_m - 2V_K]}{\pi}$$

or
$$V_{dc} = 0.636 [V_m - 2V_K] \quad (1.43)$$

If $V_m \gg V_K$ or if the diode is ideal, $V_K = 0$

$$\therefore \quad V_{dc} = 0.636 \, V_m \quad (1.44)$$

Note that, the dc output voltage of full-wave rectifier is twice that of half wave rectifier.

Average (dc) Output Current [I_{dc}]

The average or dc output current is given by

$$I_{dc} = \frac{V_{dc}}{R}$$

$$I_{dc} = 0.636 \frac{[V_m - 2V_K]}{R} \quad (1.45)$$

Average and Peak Diode Current

Diodes D_1 and D_2 Conducts during the positive half cycle of v_i and D_3 and D_4 during the negative half cycle. Hence the load current I_{dc} is equally shared by each pair of diode. Also the Conducting diodes are in series. Hence dc current through each diode is

$$I_{dc\ (diode)} = \frac{I_{dc}}{2}$$

$$= 0.318\ \frac{[V_m - 2\,V_K]}{R} \tag{1.46}$$

The peak diode current is same as the peak load current. Hence from equation 1.42,

$$I_{dm} = I_{om} = \frac{V_m - 2\,V_K}{R} \tag{1.47}$$

***Peak Inverse Voltage* [*PIV*]**

Applying KVL to the path $A - Q - B - A$ in the circuit of Fig 1.23 (a), we get

$$v_i - v_d - V_K = 0$$

$$v_d = v_i - V_K$$

v_d is the instaneous reverse voltage on the diode. Maximum reverse voltage occurs when, $v_i = V_m$. Hence peak inverse voltage across the diode is

$$\text{PIV} = V_m - V_K$$

For $V_m \gg V_K$,

$$\text{PIV} = V_m \tag{1.48}$$

It is important to note that, the PIV rating of the diode should be greater then V_m, for safe operation.

Diode Power Dissipation

The power dissipated in each diode is

$$P_{diode} = V_K\, I_{dc\ (diode)} \tag{1.49}$$

Example 1.27

A full-wave bridge rectifier with a 220 V rms sinusoidal input has a load resistor of 10 kΩ. Assuming silicon diodes, calculate

(a) dc output voltage and dc load current
(b) peak output voltage and peak load current
(c) peak and average diode currents
(d) power rating of each diode
(e) PIV across each diode

Solution

$$V_i = 220\ \text{V (rms)}$$

$$V_m = 220\ \text{V} \times \sqrt{2} = 311.13\ \text{V}$$

$$R = 10\ \text{k}\Omega$$

(a) DC output voltage is

$$V_{dc} = 0.636\,[V_m - 2\,V_K]$$
$$= 0.636\,[311.13\text{ V} - 1.4\text{ V}] = 197\text{ V}$$

dc load current is

$$I_{dc} = \frac{V_{\text{dc}}}{R}$$
$$= \frac{197\text{ V}}{10\text{ k}\Omega} = 19.7\text{ mA}$$

(b) Peak output voltage is

$$V_{om} = V_m - 2\,V_K$$
$$= 311.13\text{ V} - 1.4\text{ V} = 309.73\text{ V}$$

Peak load current is

$$I_{om} = \frac{V_{om}}{R}$$
$$= \frac{309.72\text{ V}}{10\text{ k}\Omega} = 30.972\text{ mA}$$

(c) Peak diode current is same as peak load current

$$\therefore \quad I_{dm} = I_{om} = 30.972\text{ mA}$$

Average diode current is

$$I_{dc\ (diode)} = \frac{I_{dc}}{2}$$
$$= \frac{19.7\text{ mA}}{2} = 9.85\text{ mA}$$

(d) Diode power dissipation is

$$P_{diode} = V_K\,I_{dc\ (diode)}$$
$$= (0.7\text{ V})\,(9.85\text{ mA}) = 6.895\text{ mW}$$

If the peak diode current is considered

$$P_{D\max} = V_K\,I_{dm}$$
$$= (0.7\text{ V})\,(30.972\text{ mA}) = 21.68\text{ mW}$$

For safe operation, it is wise to consider the maximum power dissipation $P_{D\max}$.

(e) PIV across each diode is

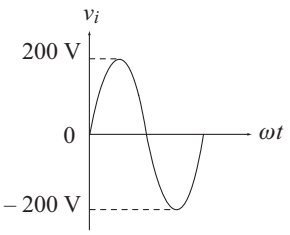
$$\text{PIV} = V_m$$
$$= 311.13\text{ V}$$

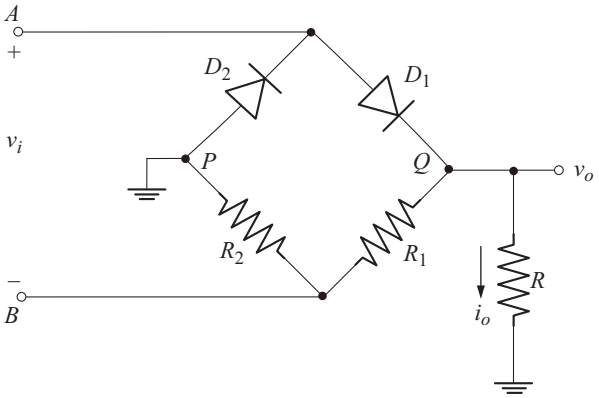
Example 1.28

For the circuit shown below.

(a) Explain the operation of the circuit
(b) Calculate the dc output voltage and current.
(c) Find the average and peak diode currents
(d) Calculate the required PIV rating of each diode.
Assume ideal diodes.

Take $R_1 = R_2 = R = 10\ \text{k}\Omega$.





Solution

Since diodes are ideal, $V_K = 0$.

(a) *Circuit Operation*

During the positive half cycle of v_i, D_1 conducts and D_2 is reverse biased. The equivalent circuit is shown below. R can be connected between P and Q.

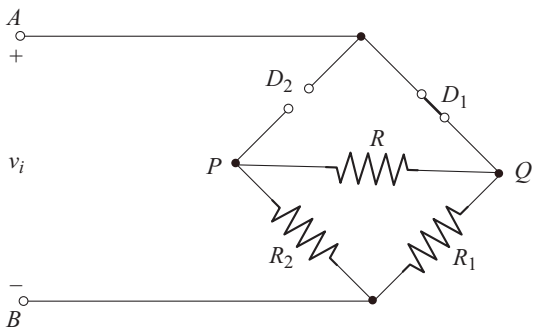


Fig. A

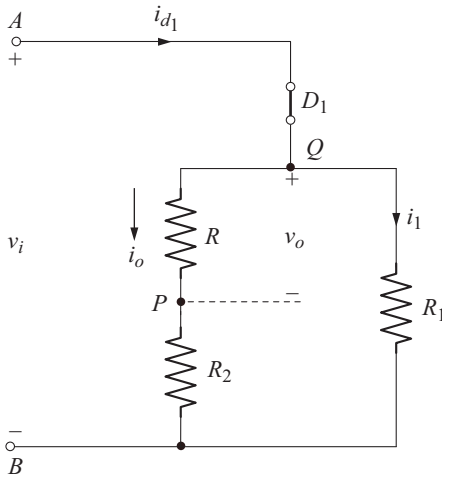


Fig. B

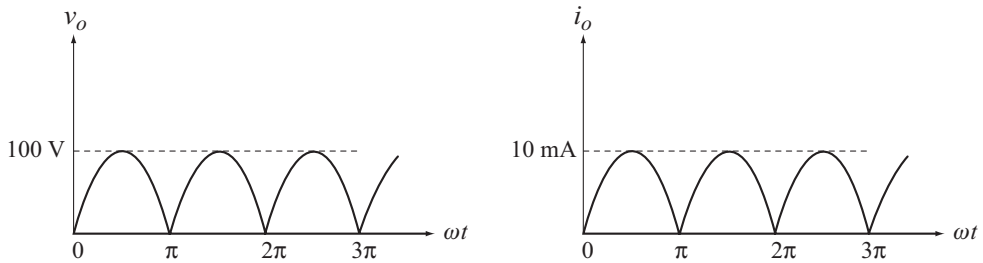
From Fig. B
The output current is

$$\begin{aligned} i_o &= \frac{v_i}{R + R_2} \\ &= \frac{200 \sin \omega t}{20\ \text{k}\Omega} \\ &= 10 \sin \omega t\ \text{mA}, \quad 0 \le \omega t \le \pi \end{aligned} \tag{A}$$

The output voltage is

$$\begin{aligned} v_o &= i_o R \\ &= (10 \sin \omega t\ \text{mA})\ (10\ \text{k}\Omega) \\ &= 100 \sin \omega t\ \text{V}, \quad 0 \le \omega t \le \pi \end{aligned} \tag{B}$$

During negative half cycle of v_i, D_2 conducts and D_1 is off. i_o and v_o are still given by Equations (A) and (B) respectively. The waveforms of i_o and v_o are shown below.



(b) v_o is a full rectified voltage with peak value of 100 V

$$\therefore \quad V_{dc} = 0.636\ [100\ \text{V}]$$

$$= 63.6\ \text{V}$$

$$I_{dc} = \frac{V_{dc}}{R}$$

$$= \frac{63.6\ \text{V}}{10\ \text{k}\Omega} = 6.36\ \text{mA}$$

(c) $$i_{d_1} = i_o + i_1 \qquad \text{[From Fig. B]}$$

$$i_1 = \frac{v_i}{R_1} = \frac{200 \sin \omega t\ V}{10\ \text{k}\Omega} = 20 \sin \omega \text{t mA}$$

$$\therefore \quad i_{d_1} = 10 \sin \omega \text{t} + 20 \sin \omega \text{t}$$

$$= 30 \sin \omega \text{t mA}, \qquad 0 \le \omega \text{t} \le \pi$$

During the negative half cycle of v_i, D_2 is on and D_1 is off. The diode current is a half-rectified sinusoid with a peak value of 30 mA.

$\therefore$ Peak diode current is

$$I_{dm} = 30 \text{ mA}$$

$$I_{dc\ (diode)} = \frac{I_{dm}}{\pi} = \frac{30 \text{ mA}}{\pi} = 9.55 \text{ mA}$$

(d) To find PIV let us consider a part of the circuit of Fig. (A) which is shown in Fig. C.

KVL equation to the circuit of Fig. (C) is

$$\begin{aligned} v_d - v_o &= 0 \\ v_d &= v_o \\ \text{PIV} &= v_{o\max} \\ &= 100 \text{ V} \end{aligned}$$

PIV rating of diode must be greater than 100 V.

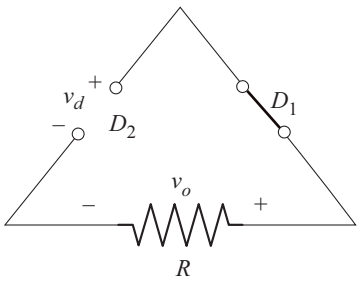


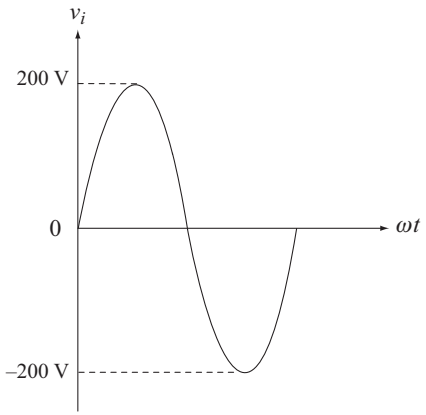
Fig. C

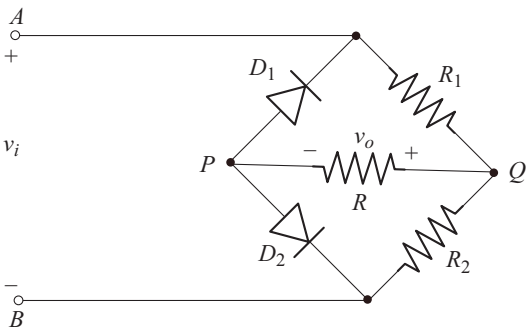
Example 1.29

For the circuit shown below

(a) Explain the operation
(b) Calculate average ouput voltage and current
(c) Calculate average and peak diode current
(d) PIV across each diode.

Assume ideal diodes.
Take $R_1 = R_2 = R = 10$ kΩ

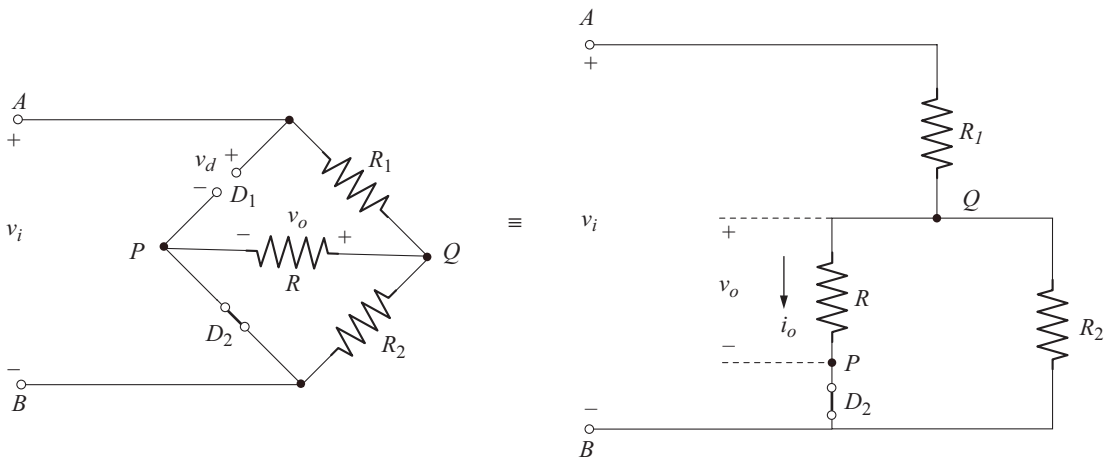




Solution

(a) Circuit Operaton

During the positive half cycle of v_i, potential of point A is positive with respect to point B. D_2 conducts and D_1 is reverse biased. The equivalent circuit is shown below.



(a) (b) (c)

Let $R' = R \parallel R_2$

$R' = 10\ \text{k}\Omega \parallel 10\ \text{k}\Omega = 5\ \text{k}\Omega$

Using voltage division rule in the circuit of Fig. (c), we have

$$v_o = \frac{v_i\, R'}{R' + R_1}$$

$$= 200 \sin \omega t \left[\frac{5\ \text{k}\Omega}{10\ \text{k}\Omega + 5\ \text{k}\Omega}\right]$$

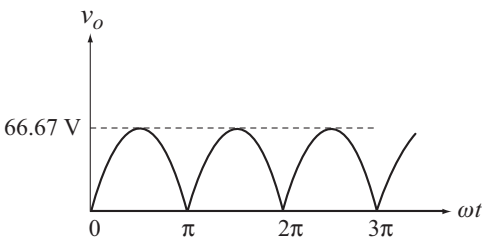
$$v_o = 66.67 \sin \omega t\ \text{V}, \quad 0 \le \omega t \le \pi \qquad \text{(A)}$$

$$i_o = \frac{v_o}{R}$$

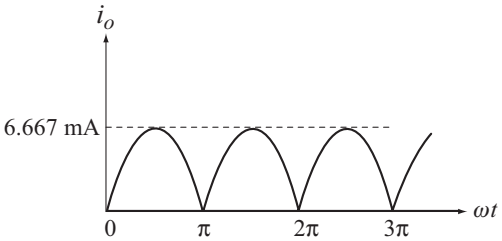
$$= \frac{66.67 \sin \omega t \text{ V}}{10 \text{ k}\Omega}$$

$$i_o = 6.667 \sin \omega t \text{ mA}, \quad 0 \le \omega t \le \pi \qquad \text{(B)}$$

During the negative half cycle of v_i, the roles of D_1 and D_2 are interchanged. v_o and i_o are still given by Equations (A) and (B) respectively. The waveforms of v_o and i_o are shown below.



(d)



(e)

Note that v_o is a full rectified voltage.

From the waveforms shown above, we note that

Peak output voltage = 66.67 V

Peak output current = 6.667 mA

(b) dc output voltage is

$$V_{dc} = 0.636 \, [66.67 \text{ V}]$$

$$= 42.4 \text{ V}$$

dc output current is

$$I_{dc} = \frac{V_{dc}}{R} = \frac{42.4 \text{ V}}{10 \text{ k}\Omega} = 4.24 \text{ mA}$$

(c) Average diode current is

$$I_{dc \ (diode)} = \frac{I_{dc}}{2} = \frac{4.24 \text{ mA}}{2} = 2.12 \text{ mA}$$

Peak diode current is same as peak output current

$$\therefore \qquad I_{dm} = I_{om} = 6.667 \text{ mA}$$

(a) To find PIV let us apply KVL to the path $A - D_1 - P - D_2 - B - A$ in the circuit of Fig. (a).

$$v_i - v_d = 0$$

$$v_d = v_i$$

$$\text{PIV} = v_{i\max} = 200 \text{ V}$$

◆ 1.16 PRACTICAL RECTIFIER CIRCUITS

Most of the electronic systems require dc voltages in the range of 5 V – 30 V for their proper operation. Since the available $1-\phi$ ac supply is 220 V at 50 Hz, the ac voltage is first reduced in amplitude using a step down transformer and then fed to the rectifier. The circuits of half-wave and full wave bridge rectifier using a step down transformer is shown in Fig. 1.25.

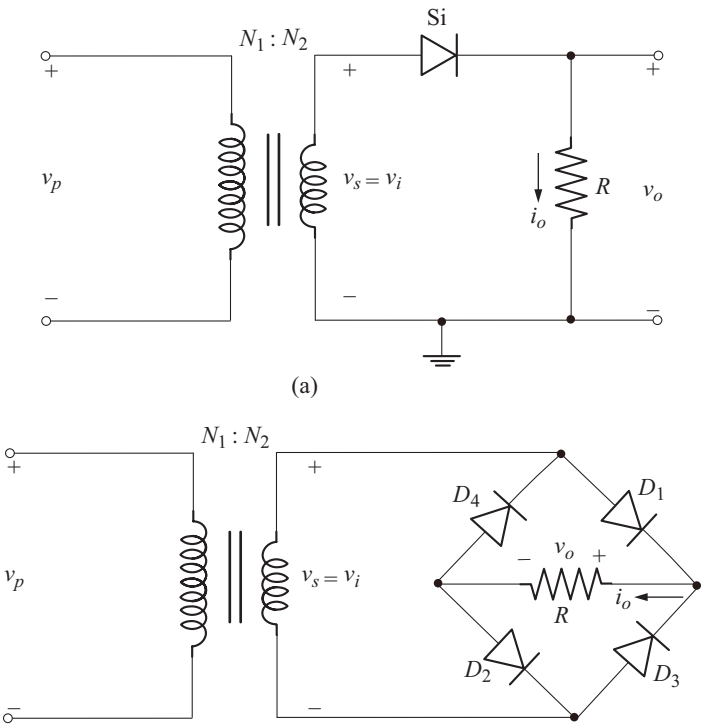


Fig. 1.25 (a) Half wave rectifier
(b) Full wave bridge rectifier

Let v_P = instantaneous primary voltage

v_S = instantaneous secondary voltage

$$\frac{N_1}{N_2} = \text{turns ratio of the transformer}$$

$$\frac{v_P}{v_S} = \frac{N_1}{N_2} \tag{1.50}$$

It should be noted that v_S is same as v_i which is the actual voltage applied to the rectifier. The following two examples illustrates how we can proceed to solve for various currents and voltages when the value of v_p is known

Let $v_p = 311 \sin \omega t$ V

and $$\frac{N_1}{N_2} = 10 \text{ or } 10:1$$

Now $$v_S = v_i = \frac{N_2}{N_1} v_p$$

$$= \frac{311}{10} \sin \omega t$$

$$v_i = 31.1 \sin \omega t = V_m \sin \omega t$$

$\Rightarrow$ $$V_m = 31.1 \text{ V}$$

This value of V_m should be used to calculate the required currents and voltages as illustrated in the previous examples. As another example

Let $$V_p = 220 \text{ V (rms)}$$

and $$\frac{N_1}{N_2} = 10 \text{ or } 10:1$$

Now $$V_s = V_i = \frac{N_2}{N_1} V_p$$

$$= \frac{220 \text{ V}}{10}$$

$$= 22 \text{ V (rms)}$$

$$V_m = \sqrt{2} \times \text{RMS value}$$

$$= \left(\sqrt{2}\right) (22 \text{ V})$$

$$= 31.11 \text{ V}$$

◆ 1.17 FULL WAVE RECTIFIER USING TWO DIODES AND A CENTRE-TAPPED TRANSFORMER

A full wave rectifier can also be constructed using only two diodes but it requires a centre–tapped transformer as shown in Fig. 1.26. The centre tapped transformer is used to obtain two equal voltages but of opposite phase at points *A* and *B*.

Note that the secondary has two identical windings and each half of the secondary having N_2 turns along with the primary having N_1 turns works as a transformer with turns ratio

$$\frac{N_1}{N_2} = \frac{v_p}{v_S} = \frac{v_p}{v_i} \tag{1.51}$$

The voltage from one end i.e., *A* (or *B*) to centre-tap i.e., *O* is v_S and the end-to-end (between *A* and *B*) voltage is $2v_S$.

During the positive half cycle of v_p, the voltage at point *A* is positive going and that at *B* is negative going with respect to centre tap. D_1 conducts and D_2 is off. The current follows the path $A - D_1 - \text{P} - O - A$. The equivalent circuit is shown in Fig. 1.27 (a).

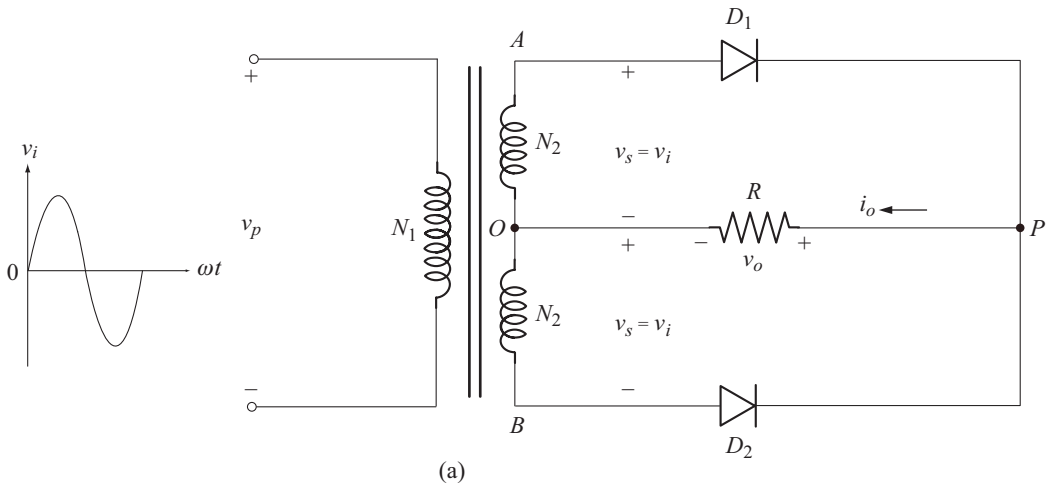


Fig. 1.26 Full wave rectifier with centre-tapped transformer

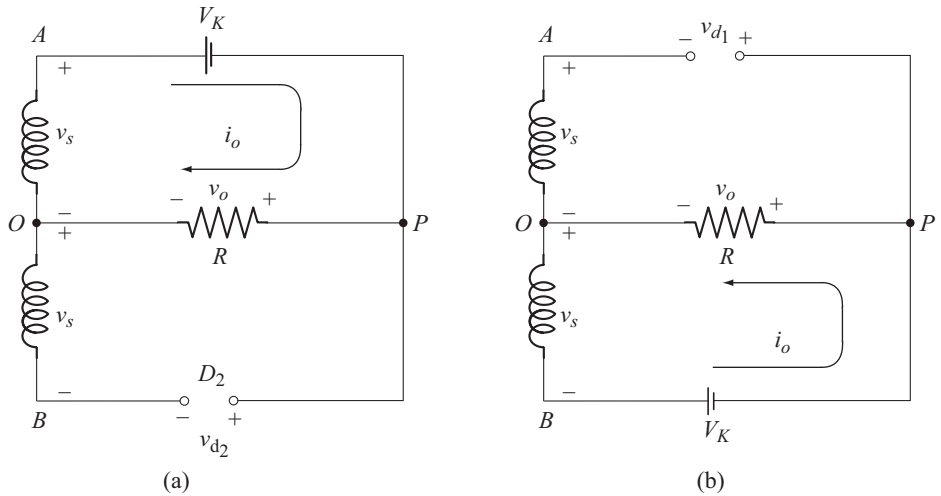


Fig. 1.27 Equivalent circuit
(a) During the positive half cycle of input
(b) During the negative half cycle of input

Applying KVL to the path $A - P - O - A$ in the circuit of Fig. 1.27(a) we have

$$-V_K - v_o + v_s = 0$$

$$v_o = v_s - V_K$$

When $v_s = V_m$, the peak level of the output voltage is

$$V_{om} = V_m - V_K$$

Therefore the equation for output voltage is

$$\begin{aligned} v_o &= V_{om} \sin \omega t \\ &= (V_m - V_K) \sin \omega t, \quad 0 \le \omega t \le \pi \end{aligned} \tag{1.52}$$

The output current is

$$i_o = \frac{v_o}{R}$$

$$i_o = \frac{V_m - V_K}{R} \sin \omega t \quad 0 \le \omega t \le \pi \tag{1.53}$$

During the negative half cycle of v_p, the voltage at point A is negative going and that at B is positive going with respect to the centre tap. D_2 conducts and D_1 is off. The current follows the path $B - D_2 - P - O - B$. The equivalent circuit is shown in Fig. 1.27(b). Note that during both half cycles of ac input, the load current i_o flows from P to O only. Hence i_o is unidirectional or dc. The waveforms of v_o and i_o are shown in Fig. 1.28.

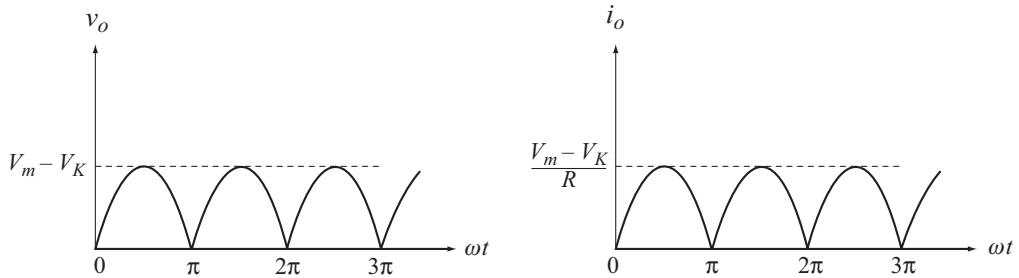


Fig. 1.28 Wave forms of v_o and i_o

The expressions for average output voltage, average output current etc can be derived in a similar way as explained in section 1.15 for full-wave bridge rectifier.

The average output voltage is

$$V_{dc} = 0.636 \, [V_m - V_K] \tag{1.54}$$

Average output current is

$$I_{dc} = 0.636 \, \frac{[V_m - V_K]}{R} \tag{1.55}$$

Average diode current is

$$\begin{aligned} I_{dc\ (diode)} &= \frac{I_{dc}}{2} \\ &= 0.318 \, \frac{[V_m - V_K]}{R} \end{aligned} \tag{1.56}$$

The peak diode current is

$$I_{dm} = I_{om} = \frac{V_m - V_K}{R} \tag{1.57}$$

and the diode power dissipation is

$$P_D = V_K I_{dc\ (diode)} \tag{1.58}$$

***Peak Inverse Voltage* [*PIV*]**

Applying KVL to the path $A - P - B - O - A$ to the circuit of Fig. 1.27 (a) we have

$$-V_K - v_{d_2} + v_s + v_s = 0$$
$$v_{d_2} = 2\,v_s - V_K$$

The reverse voltage v_{d_2} is maximum when $v_s = V_m$

$$\therefore \qquad \text{PIV} = 2\,V_m - V_K$$

Neglecting V_K, we get

$$\text{PIV} \approx 2\,V_m \tag{1.59}$$

Note that the PIV across each diode is twice that of the bridge circuit. For safe operation, the PIV rating of the diode must be greater than $2V_m$.

Example 1.30

A full-wave rectifier using two diodes and a centre-tapped transformer is supplying a resistive load of 2 kΩ. The ac supply voltage is 220 V (rms) and turns ratio of the transformer is 10 : 1. Assuming silicon diodes calculate

(a) dc output voltage
(b) dc load current
(c) dc diode current
(d) Peak diode current
(e) Peak load current
(f) PIV across each diode

Solution

$$V_p = 220\text{ V (rms)} \quad R = 2\text{ k}\Omega$$

$$\frac{N_1}{N_2} = 10$$

$$V_s = \frac{N_2}{N_1} V_p = \frac{1}{10}(220\text{ V}) = 22\text{ V}$$

$$V_m = \sqrt{2}\ V_s = \sqrt{2}\ (22\text{ V}) = 31.11\text{ V}$$

(a) dc output voltage is

$$V_{dc} = 0.636\,[V_m - V_K]$$
$$= 0.636\,[31.11\text{ V} - 0.7\text{ V}] = 19.34\text{ V}$$

(b) dc load current is

$$I_{dc} = \frac{V_{dc}}{R} = \frac{19.34\text{ V}}{2\text{ k}\Omega} = 9.67\text{ mA}$$

(c) dc diode current is

$$I_{dc\ (diode)} = \frac{I_{dc}}{2} = 4.835\text{ mA}$$

(d) peak diode current is

$$I_{dm} = \frac{V_m - V_K}{R} = \frac{31.11\text{ V} - 0.7\text{ V}}{2\text{ k}\Omega} = 15.2\text{ mA}$$

(e) peak load current is same as peak diode current

$$I_{om} = 15.2\text{ mA}$$

(f) PIV across each diode is

$$\text{PIV} = 2V_m = 2\,(31.11\text{ V}) = 62.22\text{ V}$$

◆ 1.18 ANALYSIS OF RECTIFIER CIRCUITS CONSIDERING THE EFFECT OF DIODE RESISTANCE

In the analysis carried out so far, we have not taken into account the average forward resistance r_{av} that appears in the diode equivalent circuit, since we have assumed that, $R \gg r_{av}$. If r_{av} is comparable to R, then it is necessary to consider the effect of r_{av}. The average forward resistance r_{av}, is some times also denoted by r_f. In the following example we have considered the effect of r_{av}.

Example 1.31

Repeat example 1.30 with $R = 100\ \Omega$ and $r_{av} = 20\ \Omega$.

Solution

Here we first find the peak diode / load current

$$I_{dm} = I_{om} = \frac{V_m - V_K}{R + r_{av}}$$

$$= \frac{31.11\text{ V} - 0.7\text{ V}}{100\ \Omega + 20\ \Omega} = 253.42\text{ mA}$$

Average load current is

$$I_{dc} = \frac{2}{\pi} I_{om} = 0.636\,[253.42\text{ mA}] = 161.17\text{ mA}$$

Average diode current is

$$I_{dc\ (diode)} = \frac{I_{dc}}{2} = 80.58 \text{ mA}$$

PIV across each diode is

$$\text{PIV} = 2V_m = 2\,[31.11 \text{ V}] = 62.22 \text{ V}$$

Average load voltage is

$$V_{dc} = I_{dc} R = (161.17 \text{ mA})\,(100\ \Omega) = 16.11 \text{ V}$$

Note:

- For full wave bridge rectifier

$$I_{om} = I_{dm} = \frac{V_m - 2\,V_K}{R + 2\,r_{av}}$$

- For half wave rectifier

$$I_{om} = I_{dm} = \frac{V_m - V_K}{R + r_{av}}$$

◆ 1.19 CLIPPING CIRCUITS OR LIMITING CIRCUITS

Clipping circuits (clippers) are used to remove a portion of a time varying input signal without distorting the remaining part of the applied waveform. One simple example of a clipper is a half–wave rectifier which transfers only one half cycle of the input to the output, while clipping-off the other half cycle. Therefore diodes can be used to perform clipping.

◆ 1.20 SHUNT OR PARALLEL CLIPPER

In parallel clipper the diode appears in the parallel branch or shunt with the applied input signal. Figure 1.29 shows a shunt clipper with a bias or reference voltage V_R.

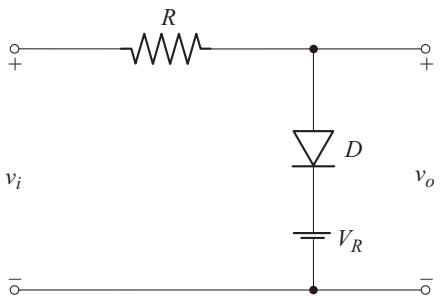


Fig. 1.29 Shunt clipper

The input signal v_i can be any periodic signal such as sine, square, triangle etc with peak value V_m greater than V_R. If $V_m < V_R$, clipping does not take place. In the analysis of clipping circuits we use the approximate equivalent circuit of diode, unless otherwise specifically mentioned.

Just before the diode conducts, the current through R is zero and hence the input signal v_i is directly available at the anode of diode, as shown in Fig. 1.30.

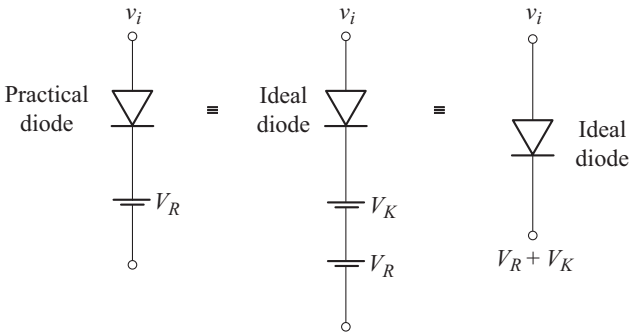


Fig. 1.30 Voltage at diode terminals

For the ideal diode to conduct, it is enough that the anode voltage just equals the cathode voltage. From Fig. 1.30 we find that the diode conducts for

$$v_i \geq V_R + V_K$$

The equivalent circuit during diode conduction is shown in Fig. 1.31 (a).

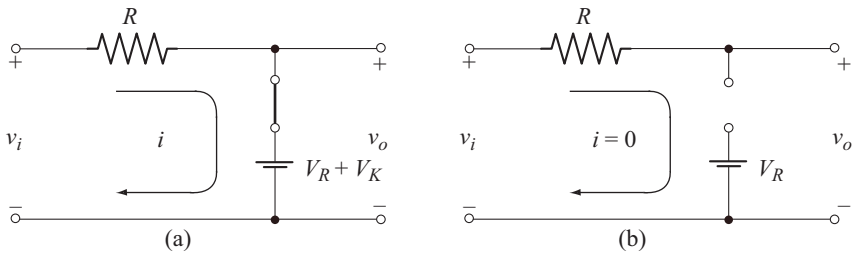


Fig. 1.31 Equivalent circuit during
(a) Diode conduction
(b) Diode off

From the equivalent circuit of Fig. 1.31 (a), we find that

$$v_o = V_R + V_K \quad \text{for} \quad v_i \geq V_R + V_K \tag{1.60}$$

For $v_i < V_R + V_K$, the diode is off and the equivalent circuit is shown in Fig. 1.31 (b). Writing KVL equation to the equivalent circuit we have

$$v_i - i R - v_o = 0$$

or

$$v_o = v_i, \quad \text{for} \quad v_i < V_R + V_K \tag{1.61}$$

In Fig. 1.32, the ouput waveforms are sketched for sine, square and triangular input waveforms.

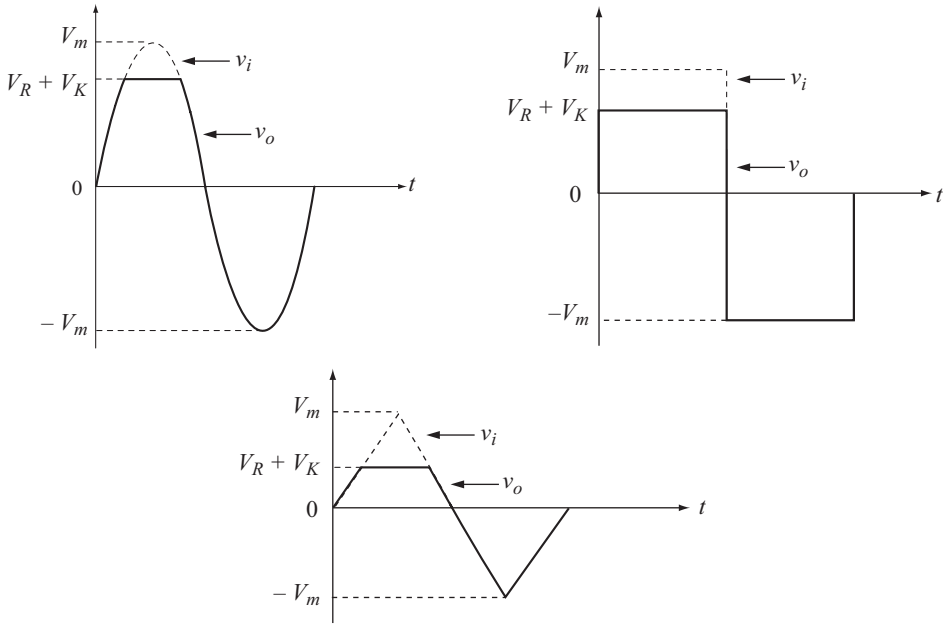


Fig. 1.32 Output waveforms of series clipper of Fig. 1.29 for different inputs

Note that the circuit clips-off a portion of the input signal, which lies above the level $V_R + V_K$ and retains the remaining part as it is.

Transfer Characteristics

The transfer characteristics is obtained by plotting v_o as a function of v_i. Transfer characteristics can be easily constructed by evaluating slope $\frac{\Delta v_o}{\Delta v_i}$

For $v_i \geq V_R + V_K$, from Equation (1.60) we have

$$v_o = V_R + V_K = \text{constant}$$

$$\Rightarrow \quad \Delta v_o = 0$$

$$\text{Hence} \quad \text{slope} = \frac{\Delta v_o}{\Delta v_i} = 0 \tag{1.62}$$

For $v_i < V_R + V_K$, from Equation (1.61) we have

$$v_o = v_i$$

$$\Rightarrow \quad \Delta v_o = \Delta v_i$$

$$\therefore \quad \text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 1 \tag{1.63}$$

Figure 1.33 shows the transfer characteristics of the shunt clipper shown in Fig. 1.29 along with output waveform for sinusoidal input.

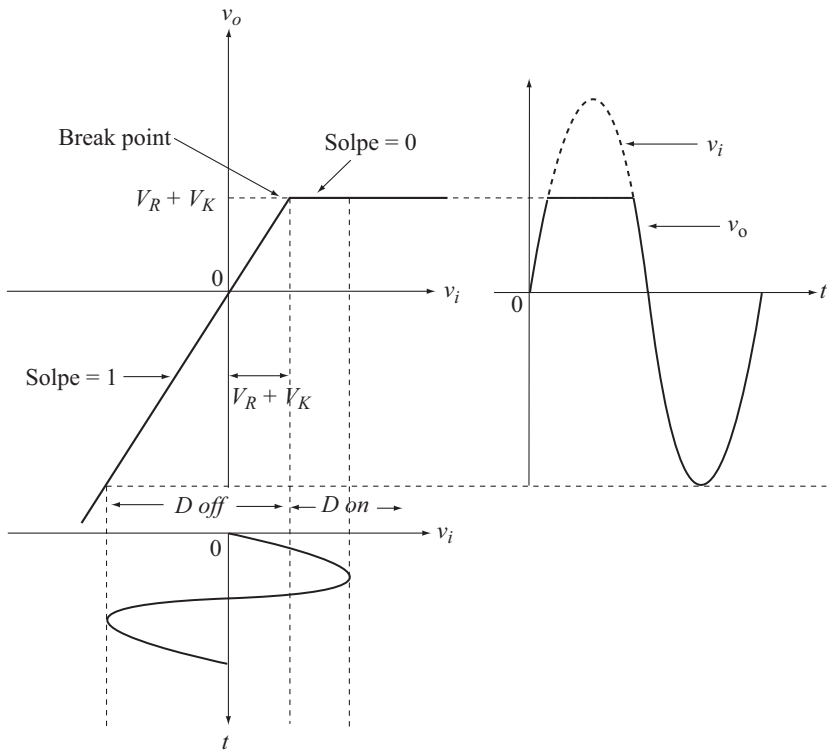


Fig. 1.33 Transfer characteristics and output waveform for the shunt clipper of Fig. 1.29

◆ 1.21 SERIES CLIPPER

In series clipper, the diode appears in series with the input or it appears in the series branch as shown in Fig. 1.34.

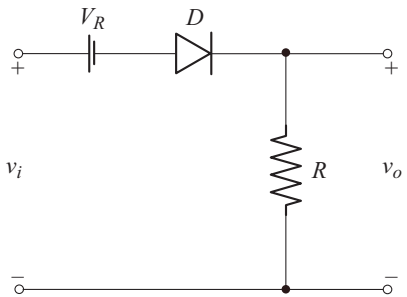


Fig. 1.34 Series clipper

First let us find the voltage on diode terminals as shown in Fig. 1.35.

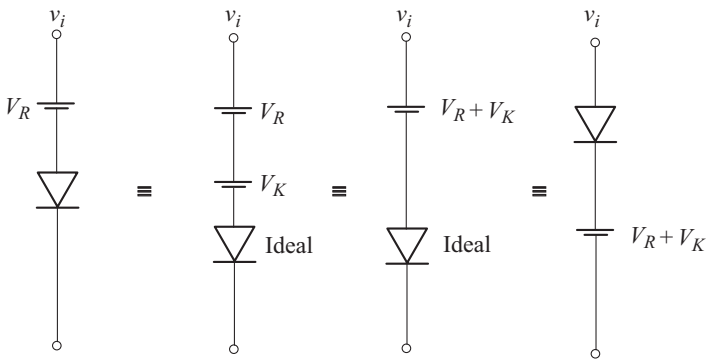


Fig. 1.35 voltage on diode terminals

From Fig. 1.35 we note that, diode conducts for $v_i \geq V_R + V_K$. The equivalent circuit during diode conduction is shown in Fig. 1.36 (a).

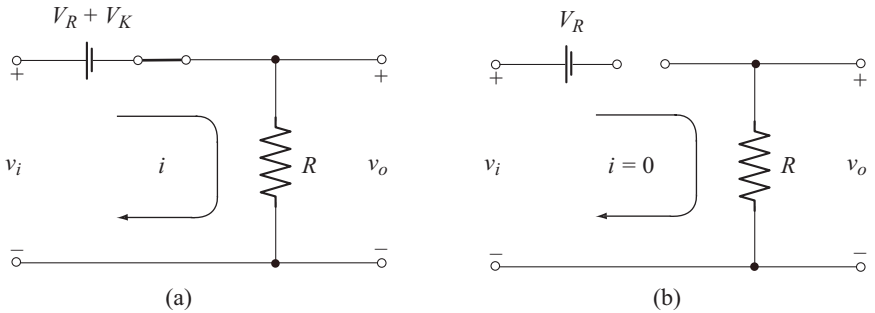


Fig. 1.36 Equivalent circuit
(a) During diode conduction
(b) During diode off

Applying KVL to the circuit of Fig. 1.36(a) we have

$$v_i - [V_R + V_K] - v_o = 0$$

$$v_o = v_i - [V_R + V_K], \quad \text{for } v_i \geq V_R + V_K \tag{1.64}$$

Since $V_R + V_K$ is a constant

$$\Delta v_o = \Delta v_i$$

$$\Rightarrow \quad \text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 1$$

Alo from Equation (1.64), when $v_i = V_m$,

$$v_o = V_m - [V_R + V_K] \tag{1.65}$$

For $v_i < V_R + V_K$, diode is off. The equivalent circuit is shown in Fig. 1.36(b). From the equivalent circuit we have

$$v_o = iR = 0 \tag{1.66}$$

Also
$$\text{slope} = \frac{\Delta v_o}{\Delta v_i} = 0 \tag{1.67}$$

The transfer characteristics and the output voltage waveforms for different inputs are shown in Fig. 1.37.

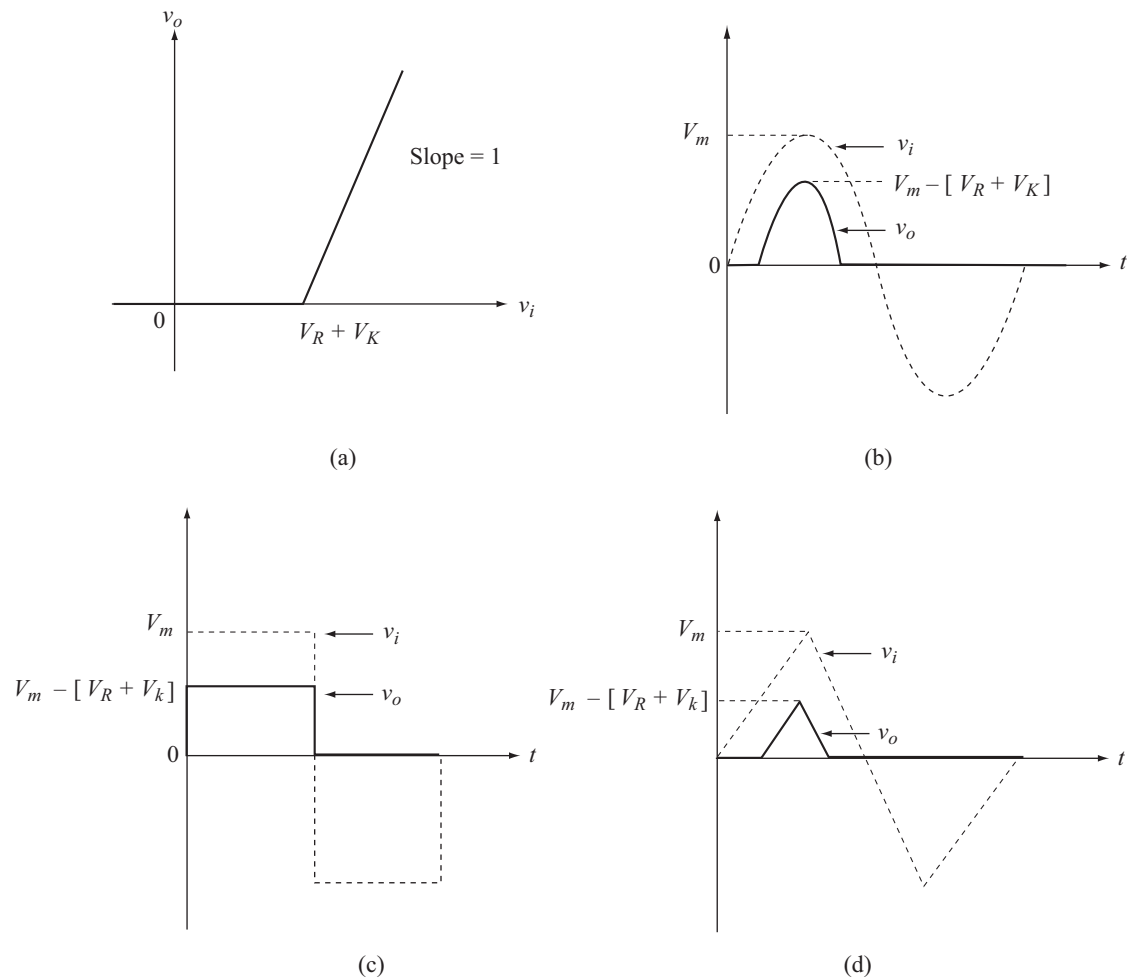


Fig. 1.37 (a) Transfer characteristics
(b) (c) and (d) output waveforms sine, square and triangular inputs

Note: In the clipping circuits, the reference voltage V_R need not be in series with the diode. The location of diode and reference voltage depends on the nature of the required output waveform.

◆ 1.21 CLIPPING AT TWO INDEPENDENT LEVELS [DOUBLE ENDED CLIPPER]

In Section 1.20 we saw clipper which clipped at one reference level. Two such clippers can be combined to obtain clipping at two independent levels. Fig. 1.38 shows clipping circuit which uses two reference voltages.

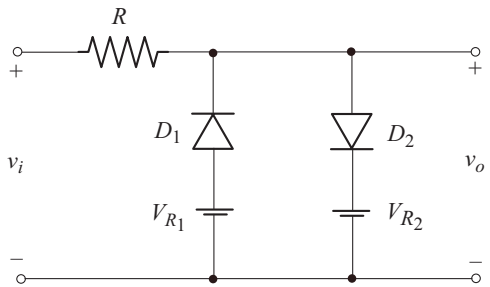


Fig. 1.38 Clipping circuit with two reference voltages

Note that both V_{R_1} and V_{R_2} are positive. V_{R_1} forward biases D_1 and V_{R_2} reverse biases D_2. Also $V_{R_2} > V_{R_1}$.

Now let us find the voltages on the terminals of D_1 as shown in Fig. 1.39.

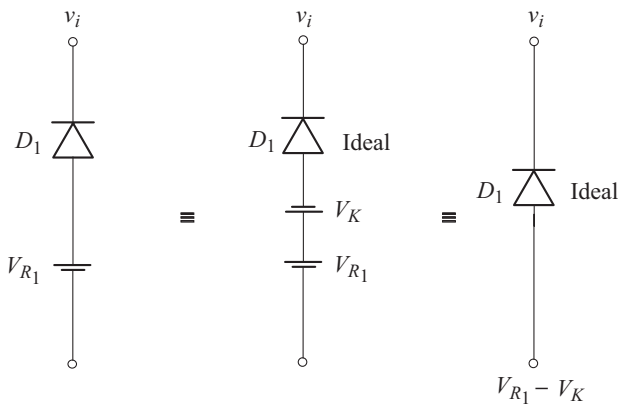


Fig. 1.39 Terminal voltages on D_1

From Fig. 1.39, we note that D_1 conducts for $v_i \leq V_{R_1} - V_K$.

The equivalent circuit is shown in Fig. 1.40 (a). From the equivalent circuit, we find that

$$v_o = V_{R_1} - V_K, \quad \text{for } v_i \leq V_{R_1} - V_K \tag{1.68}$$

$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 0 \tag{1.69}$$

The analysis of the second branch containing D_2 and V_{R_2} has already been considered in section 1.20. We find that D_2 conducts for $v_i \geq V_{R2} + V_K$.

The equivalent circuit is shown in Fig. 1.40(c). From the equivalent circuit we find that

$$v_o = V_{R_2} + V_K, \quad \text{for } v_i \geq V_{R_2} + V_K \tag{1.70}$$

$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 0 \tag{1.71}$$

For $(V_{R_1} - V_K) < v_i < (V_{R_2} + V_K)$, neither D_1 nor D_2 conducts.

The equivalent circuit is shown in Fig. 1.40(b). From the equivalent circuit we get

$$v_o = v_i \tag{1.72}$$

$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 1 \tag{1.73}$$

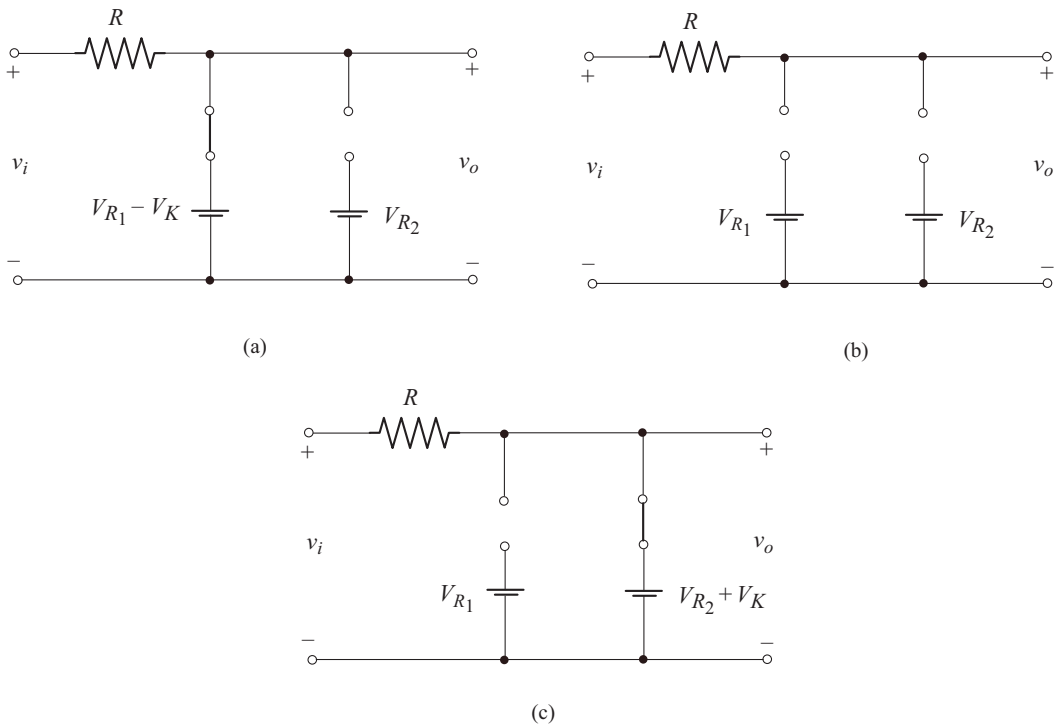


Fig. 1.40 Equivalent circuit for
(a) $v_i \leq V_{R_1} - V_K$
(b) $V_{R_1} - V_K < v_i < V_{R_2} + V_K$
(c) $v_i \geq V_{R_2} + V_K$

The circuit operation is summarized in Table 1.4.

Table 1.4 Summary of operation of double ended clipper of Fig. 1.38

Input voltage	*Diode status*	*Output voltage*	*Slope*
$v_i \leq V_{R_1} - V_K$	D_1 on D_2 off	$v_o = V_{R_1} - V_K$	0
$V_{R_1} - V_K < v_i < V_{R_2} + V_K$	D_1 off D_2 off	$v_o = v_i$	1
$v_i \geq V_{R_2} + V_K$	D_1 off D_2 on	$v_o = V_{R_2} + V_K$	0

The transfer characteristic along with output waveform for sinusoidal input is shown in Fig. 1.41.

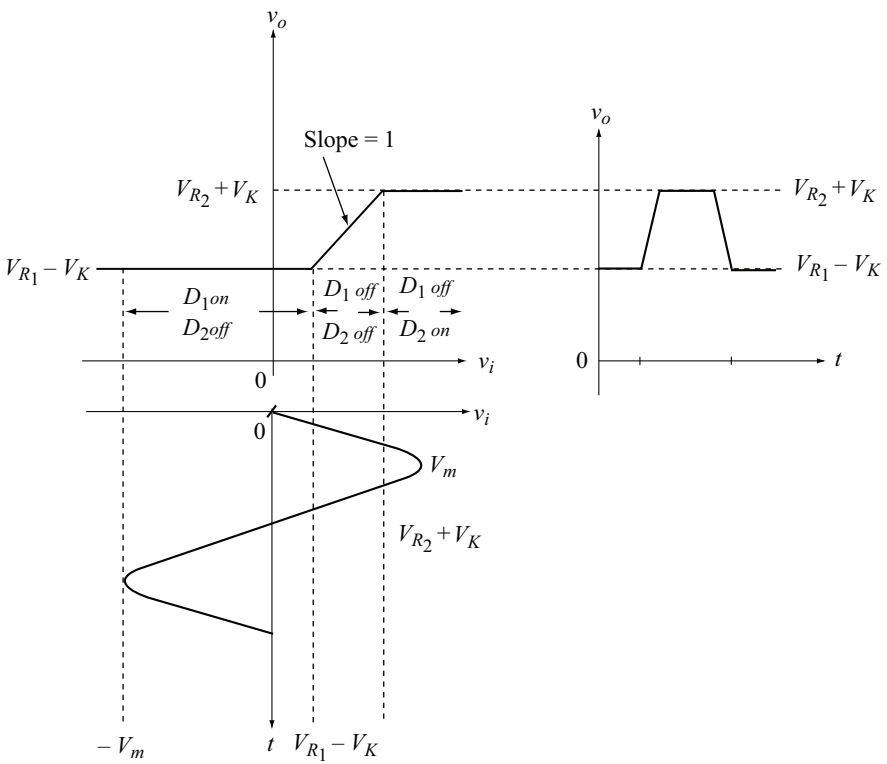


Fig. 1.41 Transfer characteristic and output waveform of the double ended clipper of Fig. 1.38

The output voltage waveforms for other input signals is shown in Fig. 1.42.

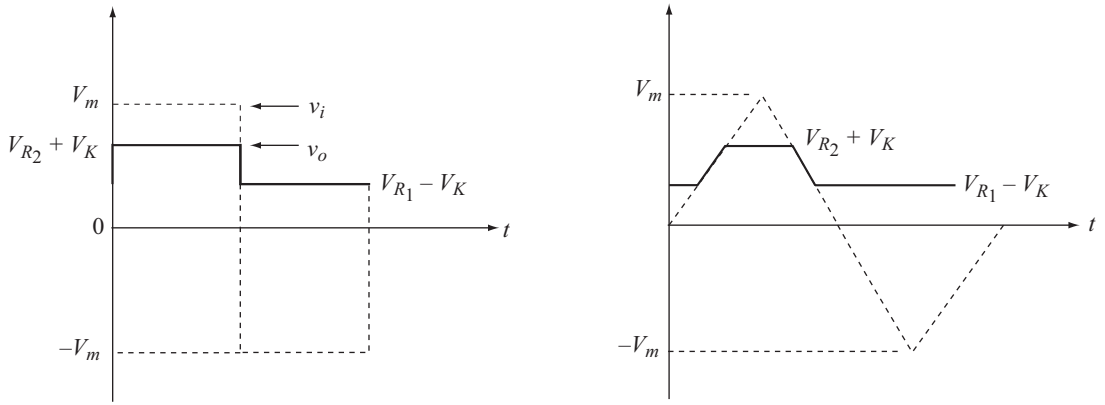


Fig. 1.42 Output waveforms for square and triangular input waveforms

1.22 ANOTHER DOUBLE ENDED CLIPPER

The variation in the double ended clipper results as shown in Fig. 1.43 when the polarity of V_{R_1} is reversed in the circuit of Fig. 1.38.

Since V_{R_1} is negative, the condition for D_1 to conduct becomes

$$v_i \leq -[V_{R_1} + V_K]$$

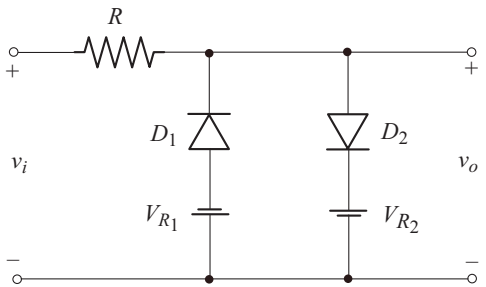


Fig. 1.43 Another double ended clipper

The analysis of this circuit can be carried out in a similar way as explained in the previous section. The circuit operation is summarized in Table 1.5.

Table 1.5 Summary of operation of doubled ended clipper of Fig. 1.43

Input voltage	*Diode status*	*Output voltage*	*Slope*
$v_i \leq -[V_{R_1} + V_K]$	D_1 on D_2 off	$v_o = -[V_{R_1} + V_K]$	0
$-[V_{R_1} + V_K] < v_i < [V_{R_2} + V_K]$	D_1 off D_2 off	$v_o = v_i$	1
$v_i \geq V_{R_2} + V_K$	D_1 off D_2 on	$v_o = [V_{R_2} + V_K]$	0

The transfer characteristic along with output for sinusoidal input is shown in Fig. 1.44.

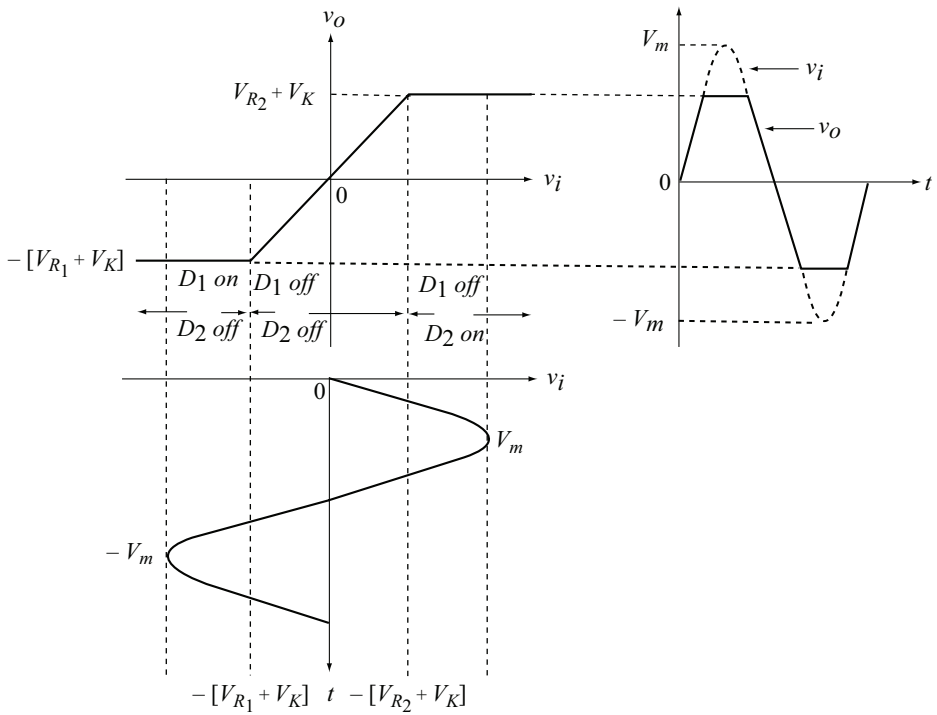


Fig. 1.44 Transfer characteristics and output waveform of the double ended clipper of Fig. 1.43

The output voltage waveforms for other inputs are shown in Fig. 1.45.

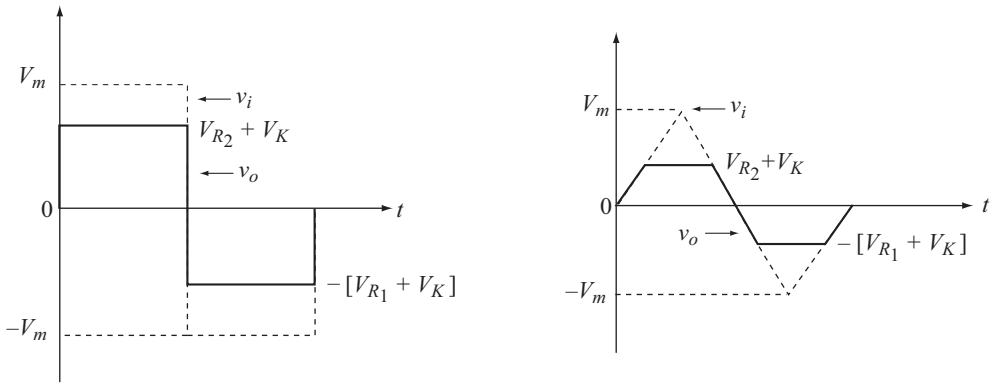
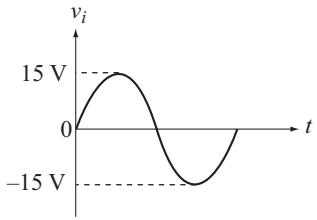


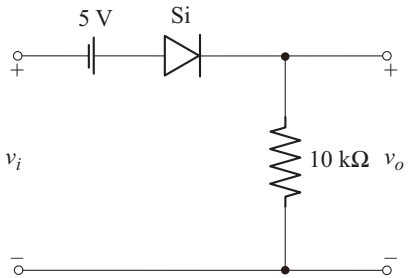
Fig. 1.45 Output waveform for square and triangular inputs

If $|V_{R_1}| = |V_{R_2}|$ then clipping level of the positive peak equals that of negative peak. This operation is called symmetical clipping and the corresponding circuit is called symmetrical double ended clipper.

Example 1.32

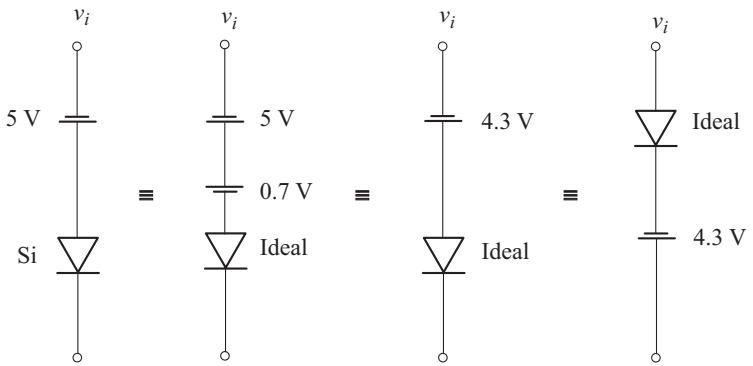
For the clipping circuit shown below, determine the transfer characteristic and sketch the output waveform.





Solution

First let us find the voltage on diode terminals.



Diode conducts for $v_i \geq -4.3$ V. The equivalent circuit during diode conduction is shown in Fig. A.

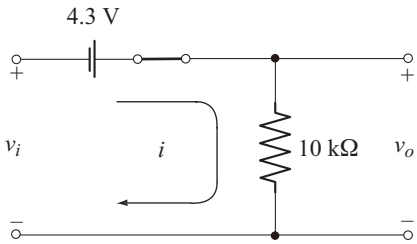


Fig. A

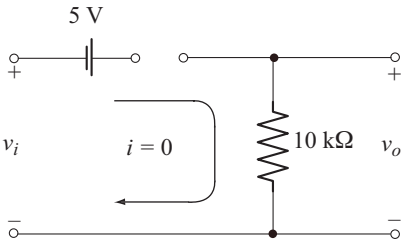


Fig. B

Writing KVL equation to the circuit of Fig. A.

$$v_i + 4.3 \text{ V} - v_o = 0$$

$$v_o = v_i + 4.3 \text{ V} \quad \text{for} \quad v_i \geq -4.3 \text{ V} \qquad \text{(A)}$$

when $v_i = 15\text{ V}$

$$v_o = 15\text{ V} + 4.3\text{ V} = 19.3\text{ V}$$

Also from Equation (A)

$$\Delta v_o = \Delta v_i$$

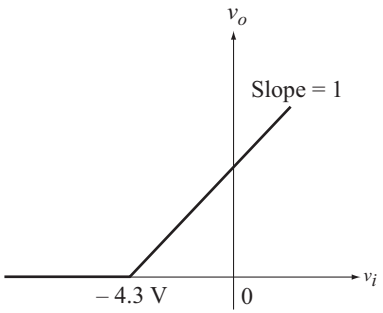
$$\Rightarrow \quad \text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 1$$

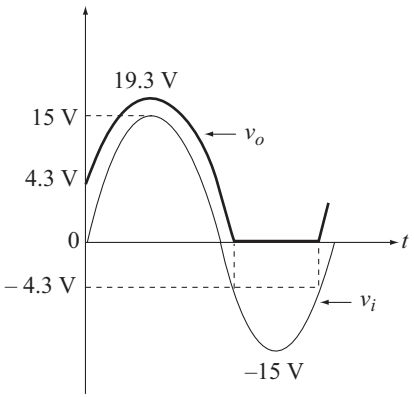
For $v_i < -4.3$ V, diode is off. The equivalent circuit is shown in Fig. B. From the equivalent circuit.

$$v_o = 0 \quad \text{for} \quad v_i < -4.3\text{ V} \tag{B}$$

$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 0$$

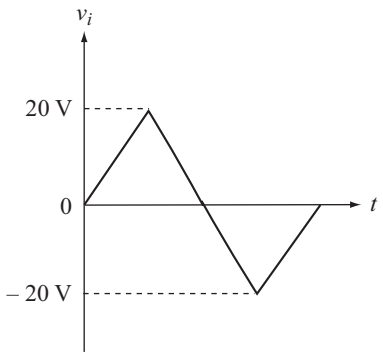
The transfer characteristic and output waveforms are shown below.

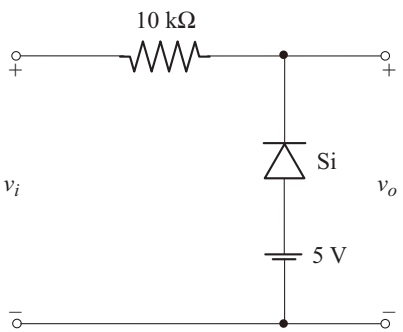




Example 1.33

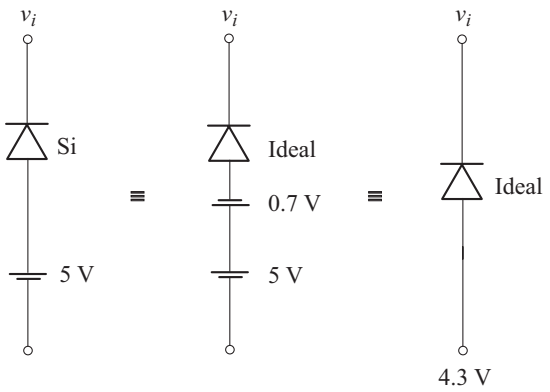
For the circuit shown below determine the transfer characteristic and sketech the output waveform.





Solution

Just prior to the conduction of diode, current through 10 kΩ resistor is zero. Hence v_i is available at the cathode of diode. Let us find the terminal voltages at the diode.



Diode conducts for $v_i \leq 4.3$ V. The equivalent circuit is shown in Fig. A.

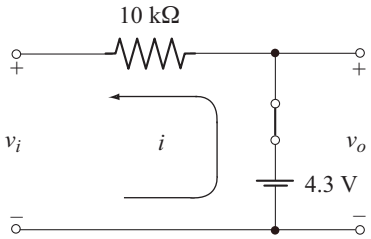


Fig. A

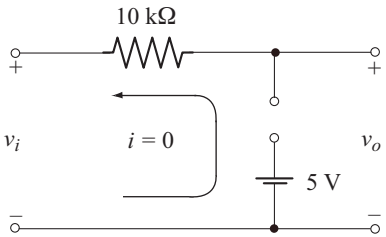


Fig. B

From the equivalent circuit of Fig. A,

$$v_o = 4.3 \text{ V} \quad \text{for } v_i \leq 4.3 \text{ V} \tag{A}$$

$$\Delta v_o = 0$$

$$\Rightarrow \quad \text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 0$$

For $v_i > 4.3$ V, diode is off and the equivalent circuit is shown in Fig. B. Writing KVL to the circuit of Fig. B,

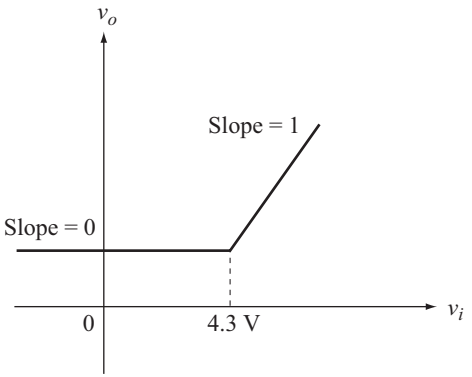
$$v_i + i\,(10 \text{ k}\Omega) - v_o = 0$$

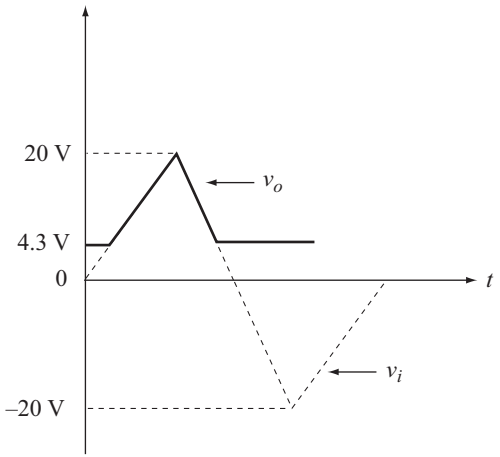
Since $\quad i = 0$

$$v_o = v_i \quad \text{for } v_i > 4.3 \text{ V} \tag{B}$$

$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 1$$

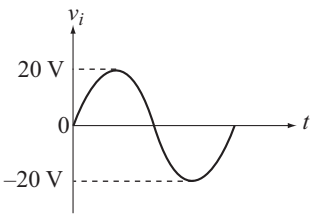
The transfer characteristic and output waveform are shown below.

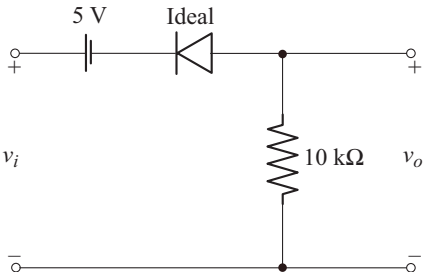




Example 1.34

For the circuit shown below determine the transfer characteristic and sketch the output waveform.





Solution

Diode conducts for $v_i \leq 5$ V. The equivalent circuit during diode conduction is shown in Fig. A.

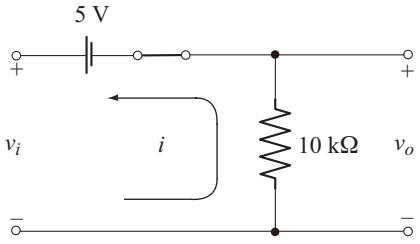


Fig. A

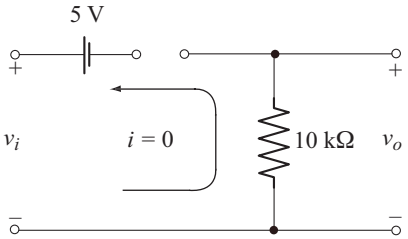


Fig. B

Applying KVL to the circuit of Fig. A, we have

$$v_i - 5\text{ V} - v_o = 0$$

$$v_o = v_i - 5\text{ V} \quad \text{for } v_i \leq 5\text{ V} \tag{A}$$

When $v_i = -20$ V

$$v_o = -20\text{ V} - 5\text{ V} = -25\text{ V}$$

Also from Equation (A)

$$\Delta v_o = \Delta v_i$$

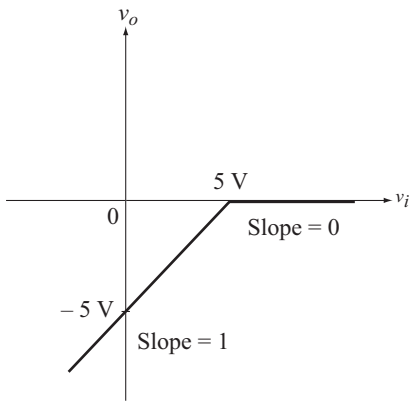
$$\Rightarrow \quad \text{Slope} = 1$$

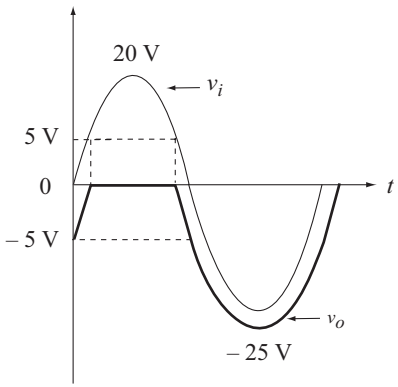
For $v_i > 5$ V, diode is off and the equivalent circuit is shown in Fig. B. We find that

$$v_o = 0 \quad \text{for } v_i > 5\text{ V} \tag{B}$$

$$\Rightarrow \quad \text{Slope} = 0$$

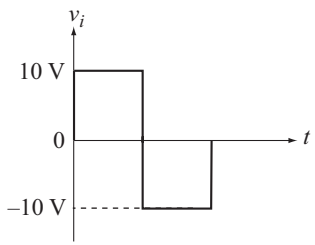
The transfer characteristic and the output waveform are shown below.

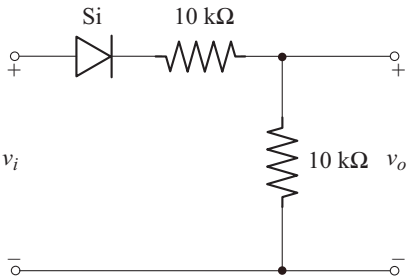




Example 1.35

For the circuit shown below sketch the output waveform for the input shown.





Solution

Diode conducts when $v_i = 10$ V. The equivalent circuit is shown in Fig. A.

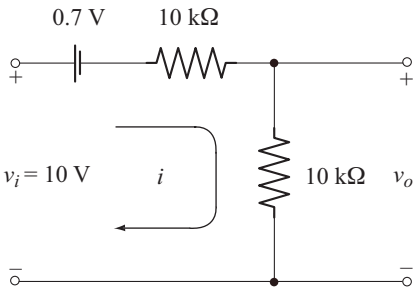


Fig. A

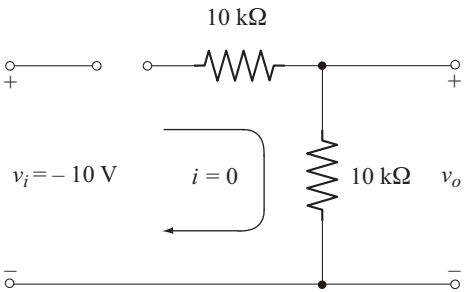


Fig. B

Applying KVL to the circuit of Fig. A.

$$10 \text{ V} - 0.7 \text{ V} - i\,(20 \text{ k}\Omega) = 0$$

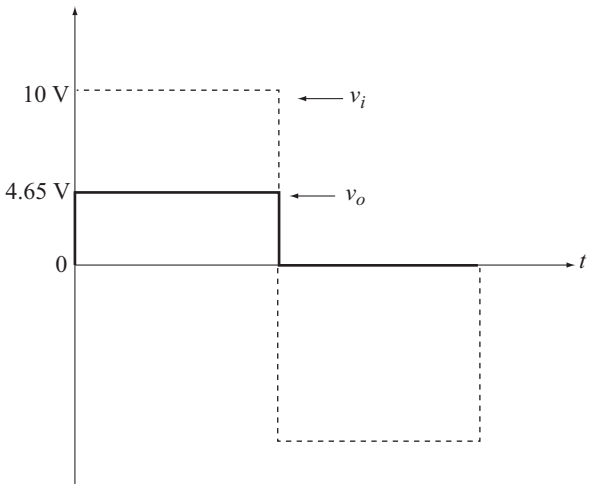
$$i = \frac{9.3 \text{ V}}{20 \text{ k}\Omega} = 0.465 \text{ mA}$$

$$v_o = i\,(10 \text{ k}\Omega) = 4.65 \text{ V}$$

When $v_i = -10$ V, diode turns off. The equivalent circuit is shown in Fig. B.

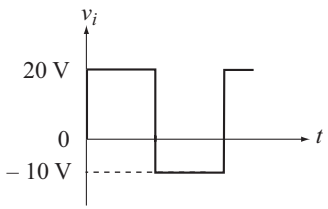
$$v_o = i\,(10 \text{ k}\Omega) = 0 \text{ V}$$

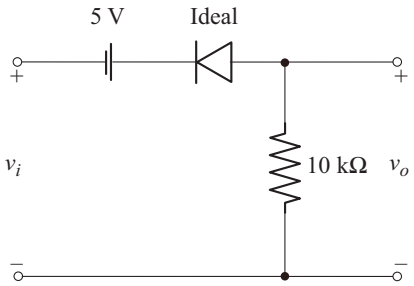
The waveform of v_o is shown below.



Example 1.36

For the circuit shown determine the transfer characteristic and sketch the waveform of v_o.





Solution

Diode conducts for $v_i \leq -5$ V. The equivalent circuit is shown in Fig. A.

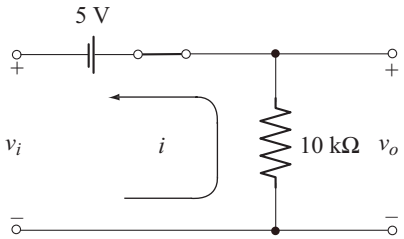


Fig. A

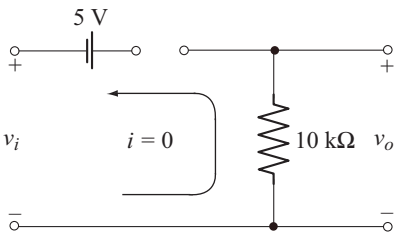


Fig. B

Applying KVL to the Circuit of Fig. A we have

$$v_i + 5\text{ V} - v_o = 0$$

$$v_o = v_i + 5\text{ V} \quad \text{for} \quad v_i \leq -5\text{ V} \tag{A}$$

$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 1$$

When $v_i = -10$ V,

$$v_o = -10\text{ V} + 5\text{ V} = -5\text{ V}$$

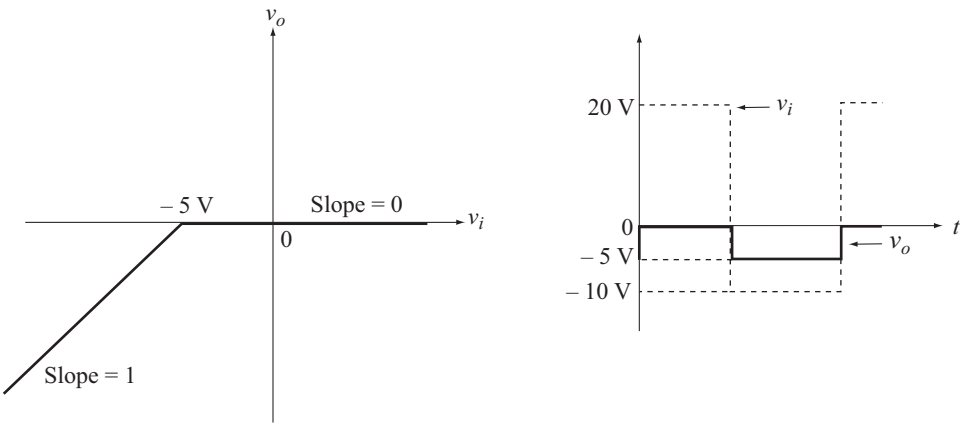
For $v_i > -5$ V, diode turns off and the equivalent circuit is shown in Fig. B. Since $i = 0$.

$$v_o = 0 \quad \text{for} \quad v_i > -5\text{ V} \tag{B}$$

$$\Rightarrow \quad \text{Slope} = 0$$

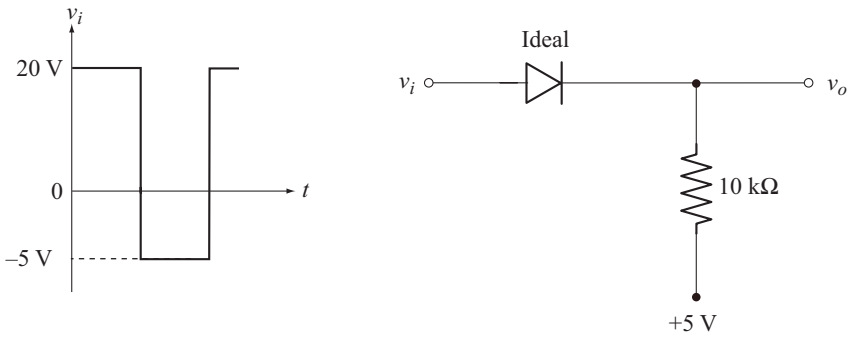
Also, $\quad v_o = 0 \quad \text{when } v_i = 20\text{ V}$

The transfer characteristic and the output waveform are shown below.



Example 1.37

For the circuit shown below determine the transfer characteristic and sketch the output voltage waveform.



Solution

Just prior to the diode conduction, no current flows through 10 kΩ resistor. Hence + 5 V is applied on the cathode terminal and therefore diode conducts for $v_i \geq 5$ V.

The equivalent circuit is shown in Fig. A.

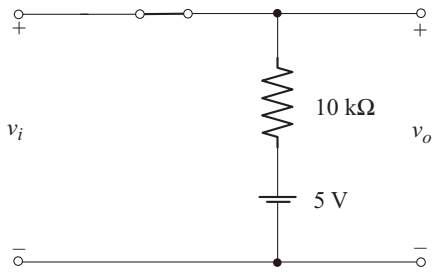


Fig. A

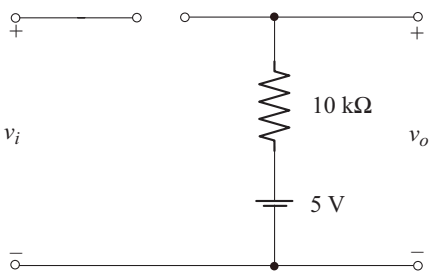


Fig. B

Applying KVL to the circuit of Fig. A, we get

$$v_i - v_o = 0$$

or $$v_o = v_i, \quad \text{for} \quad v_i \geq 5\ \text{V} \qquad \text{(A)}$$

$\Rightarrow$ $$\text{Slope} = 1$$

Also, when $$v_i = 20\ \text{V}, \quad v_o = 20\ \text{V}$$

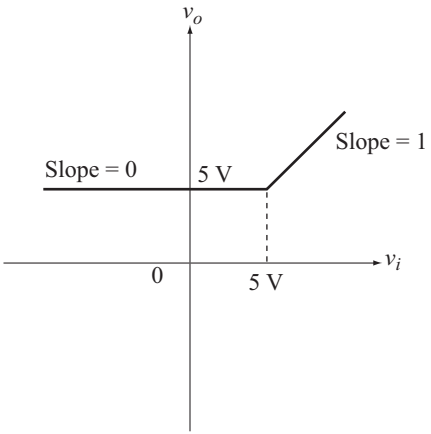
For $v_i < 5\ \text{V}$, diode turns off and the equivalent circuit is shown in Fig. B. From the equivalent circuit we find that

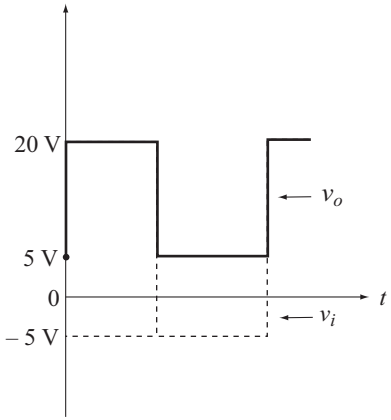
$$v_o = 5\ \text{V}, \quad \text{for } v_i < 5\ \text{V} \qquad \text{(B)}$$

$\Rightarrow$ $$\text{Slope} = 0$$

Also when $$v_i = -5\ \text{V}, \quad v_o = 5\ \text{V}$$

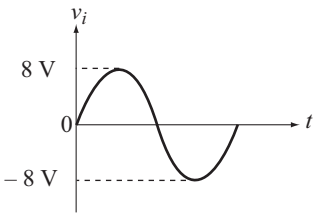
The transfer characteristic and output waveform are shown below.

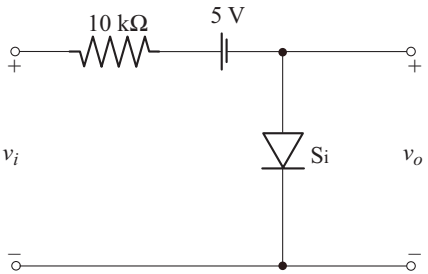




Example 1.38

For the circuit shown below sketch the output voltage waveform.





Solution

Diode conducts for $v_i \geq 5.7$ V and the equivalent circuit is shown in Fig. A.

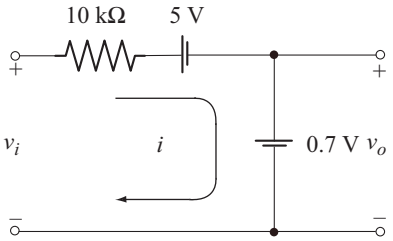


Fig. A

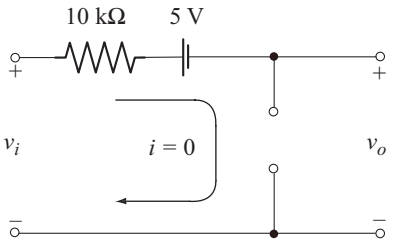


Fig. B

From the circuit of Fig. A,

$$v_o = 0.7 \text{ V} \quad \text{for} \quad v_i \geq 5.7 \text{ V} \tag{A}$$

For $v_i < 5.7$ V, diode turns off. The equivalent circuit is shown in Fig. B. Applying KVL to the circuit of Fig. B we have

$$v_i - i\,(10\ \text{k}\Omega) - 5 \text{ V} - v_o = 0$$

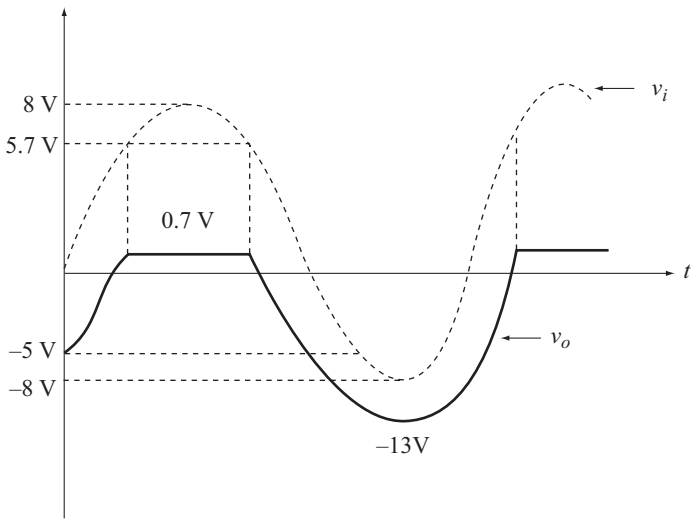
Since $$i = 0$$

$$v_o = v_i - 5 \text{ V} \quad \text{for} \quad v_i < 5.7 \text{ V} \tag{B}$$

When $$v_i = -8 \text{ V}$$

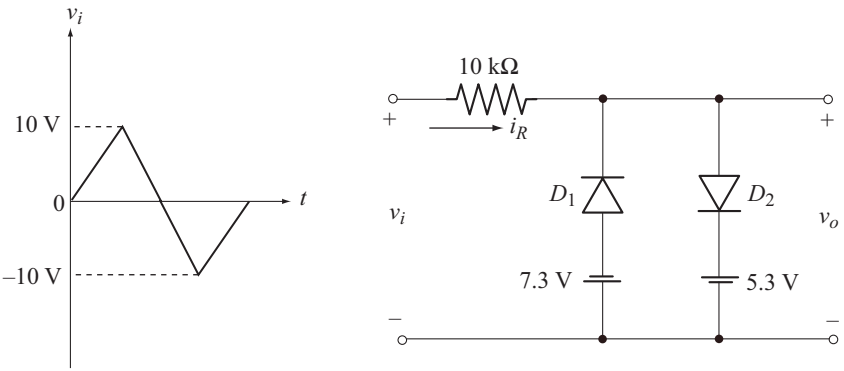
$$v_o = -8\text{V} - 5 \text{ V} = -13 \text{ V}$$

The output voltage waveform is shown below.



Example 1.39

For the circuit shown sketch the waveforms of i_R and v_o. Assume Si diodes.



Solution

The analysis of this circuit is given in section 1.22. Comparing the given circuit with that of Fig. 1.43, we have

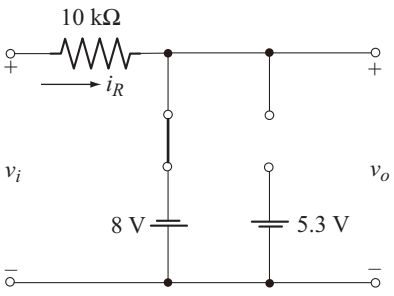
$$R = 10\ \text{k}\Omega \quad V_{R_2} = 5.3\ \text{V}$$

$$-V_{R_1} = -7.3\ \text{V} \quad \Rightarrow \quad V_{R_1} = 7.3\ \text{V}$$

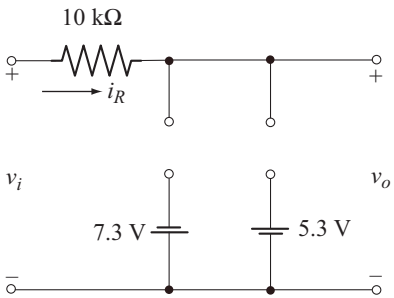
Using table 1.5, the circuit operation can be summarized as follows.

Input voltage	*Diode status*	*Output voltage*	*Slope*
$v_i \leq -8$ V	D_1 on D_2 off	$v_o = -8$ V	0
$-8\ \text{V} < v_i < 6\ \text{V}$	D_1 off D_2 off	$v_o = v_i$	1
$v_i \geq 6$ V	D_1 off D_2 on	$v_o = 6$ V	0

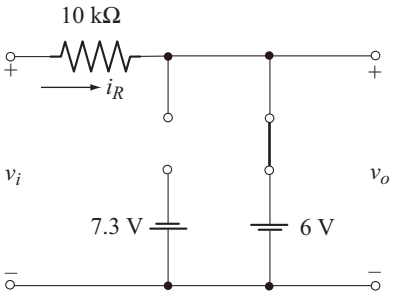
The equivalent circuits under different conditions of v_i and the transfer characteristic are shown below.



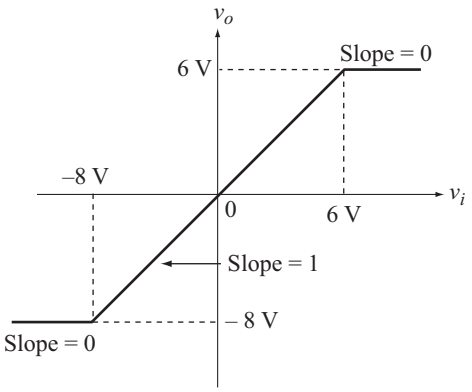
A. Equivalent circut for $v_i \leq -8$ V



B. Equivalent circut for $-8\ \text{V} < v_i < 6\ \text{V}$



C. Equivalent circut for $v_i \geq 6$ V



D. Transfer characteristics

Calculation of i_R

Applying KVL to the closed path in the equivalent circuit of Fig. A, we get

$$v_i - 10\ \text{k}\Omega\ (i_R) + 8\ \text{V} = 0$$

$$i_R = \frac{v_i + 8\ \text{V}}{10\ \text{k}\Omega} \quad \text{for} \quad v_i \leq -8\ \text{V} \tag{A}$$

When $v_i = -10$ V

$$i_R = \frac{-10\ \text{V} + 8\ \text{V}}{10\ \text{k}\Omega} = -0.2\ \text{mA}$$

From the equivalent circuit of Fig. B

$$i_R = 0, \quad \text{for} -8\text{V} < v_i < 6\ \text{V} \tag{B}$$

Finally applying KVL to the closed path in the circuit of Fig. C.

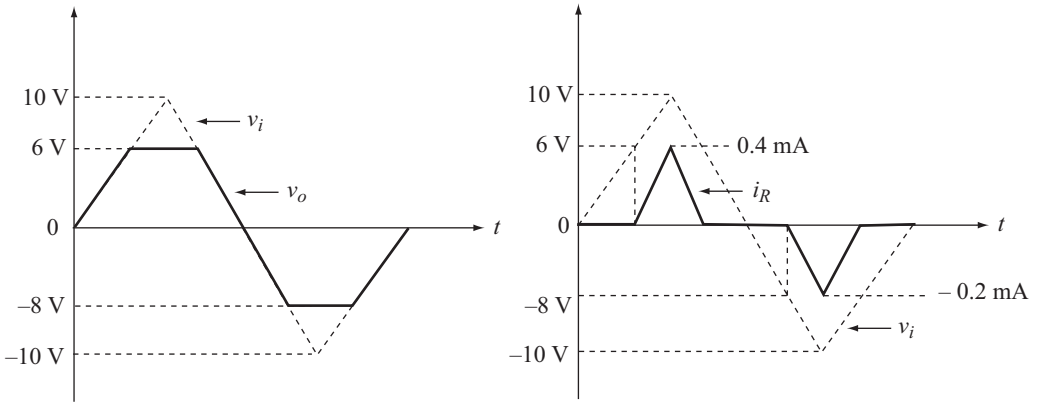
$$v_i - 10\ \text{k}\Omega\ (i_R) - 6\ \text{V} = 0$$

$$i_R = \frac{v_i - 6\ \text{V}}{10\ \text{k}\Omega} \quad \text{for} \quad v_i \geq 6\ \text{V} \tag{C}$$

When $v_i = 10$ V

$$i_R = \frac{10\ \text{V} - 6\ \text{V}}{10\ \text{k}\Omega} = 0.4\ \text{mA}$$

The waveforms of v_o and i_o are shown below.

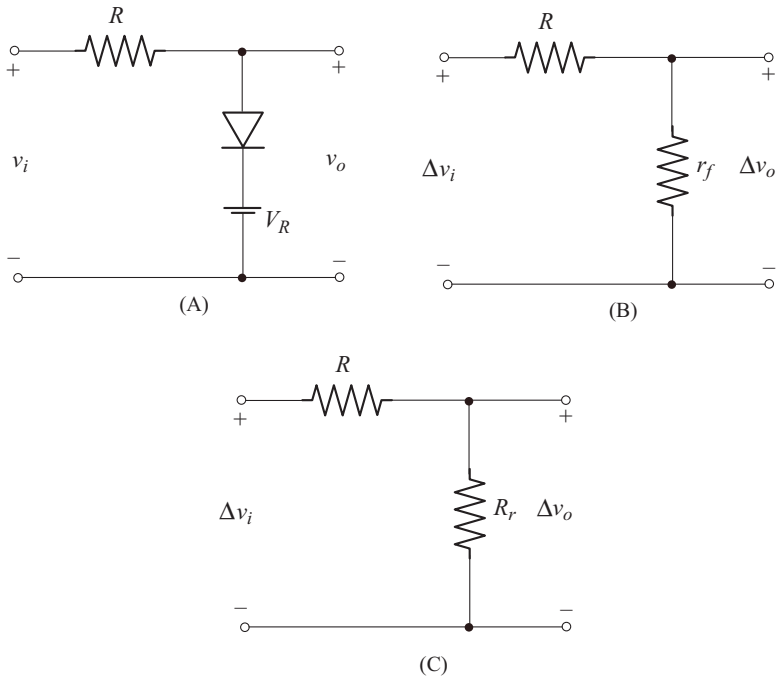


Example 1.40

Show that for a single diode clipper, a reasonable value of R is the geometric mean of r_f and R_r where r_f is the dynamic forward resistance and R_r is the reverse resistance of diode.

Solution

Let us consider the shunt clipper shown in Fig. A.



The equivalent circuit during diode conduction is shown in Fig. B. It should be noted that r_f is same as r_{av}. Since we have considered the incremental values, Δv_i and Δv_o of v_i and v_o respectively, V_K and V_R are not shown. This is because $\Delta V_K = 0$ and $\Delta V_R = 0$, since V_K and V_R are constant values.

Applying voltage division rule in the circuit of Fig. B, we get

$$\Delta v_o = \frac{r_f}{R + r_f} \Delta v_i$$

Slope of transfer characteristic is

$$\text{Slope} = \frac{\mathrm{D}v_o}{\mathrm{D}v_i} = \frac{r_f}{R + r_f}$$

For perfect clipping, slope should be zero when the diode conducts.

This requires that

$$r_f \ll R$$

Let

$$r_f = \frac{R}{K} \qquad \text{(A)}$$

where K is some arbitrary large number.

Fig. C shows the equivalent circuit when the diode is off. The slope of transfer characteristic when the diode is off is

$$\text{Slope} = \frac{\mathrm{D}v_o}{\mathrm{D}v_i} = \frac{R_r}{R + R_r}$$

For the slope to be unity when the diode is off , we require that

$$R \ll R_r \quad \text{or} \quad R_r \gg R$$

Let

$$R_r = KR \qquad \text{(B)}$$

Multiplying Equations (A) and (B) we get

$$r_f R_r = R^2$$

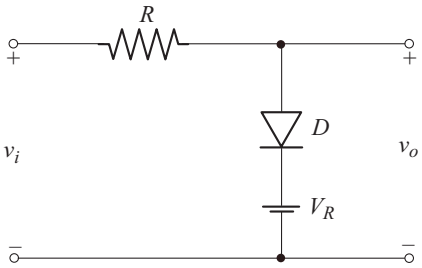
or

$$R = \sqrt{r_f R_r} \qquad \text{(C)}$$

Thus a reasonable value for R would be the geometric mean of diode forward resistance r_f and the reverse resistance R_r.

Example 1.41

For the diode clipping circuit shown, draw the input and output waveforms for (a) R = 100 Ω (b) R = 1 k Ω and (c) R = 10 k Ω given that v_i = 20 sin ωt and V_R = 10 V. Assume r_f = 100 Ω, $R_r = \infty$ and $V_K = 0$.

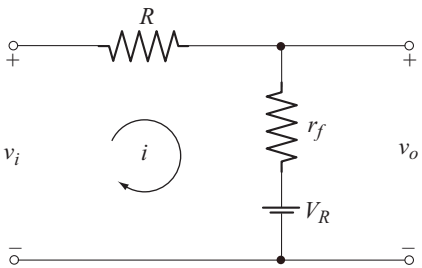


Solution:

For $v_i \geq 10$ V, D is on

For $v_i < 10$ V, D is off and hence $v_o = v_i$

The equivalent circuit when D is on is shown in the following figure.



$$v_o = i\,r_f + V_R$$

But $$i = \frac{v_i - V_R}{R + r_f}$$

$\therefore$ $$v_o = \frac{r_f}{R + r_f}(v_i - V_R) + V_R$$

v_o is maximum when v_i is maximum.

$\therefore$ $$v_{o_{\max}} = \frac{r_f}{R + r_f}(v_{i_{\max}} - V_R) + V_R$$

$$v_{i_{\max}} = 20 \text{ V}, \quad V_R = 10 \text{ V}, \quad r_f = 100\ \Omega$$

(a) For $R = 100\Omega$ $$v_{o_{\max}} = \frac{100\,\text{W}}{100\,\text{W} + 100\,\text{W}}(20 \text{ V} - 10 \text{ V}) + 10 \text{ V} = 15 \text{ V}$$

(b) For $R = 1$ kΩ $$v_{o_{\max}} = \frac{100\,\text{W}}{1000\,\text{W} + 100\,\text{W}}(20 \text{ V} - 10 \text{ V}) + 10 \text{ V} = 10.9 \text{ V}$$

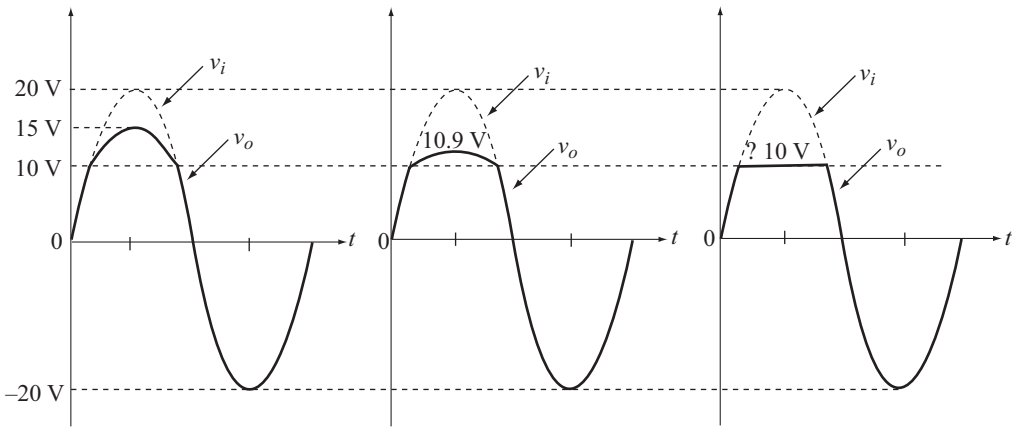
(c) For $R = 10$ kΩ $$v_{o_{\max}} = \frac{100\,\text{W}}{10000\,\text{W} + 100\,\text{W}}(20 \text{ V} - 10 \text{ V}) + 10 \text{ V} = 10.1 \text{ V}$$

When D is off $v_o = v_i$

$\therefore$ In all the three cases

$$v_{o\,\min} = v_{i\,\min} = -20 \text{ V}$$

The output plots are shown below.

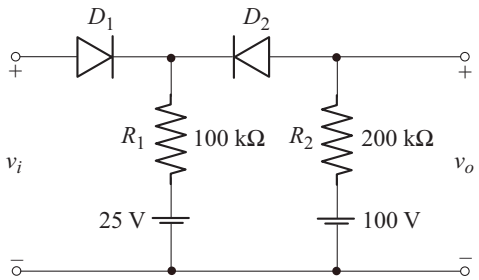


(a) R = 100 Ω **(b) R = 1000 Ω** **(c) R = 10 kΩ**

Note that clipping is better when R = 10 kΩ.

Example 1.42

Sketch the output voltage waveform over the input voltage waveform for the circuit shown, given that the input varies linearly from 0 to 150 V. Assume ideal diodes.



Solution

Ideal diodes imply, $r_f = 0$, $R_r = \infty$, $V_K = 0$.

Let $v_i = 0$ V

Then, D_1 is *off* and D_2 is on. The equivalent circuit is shown in Fig. A.

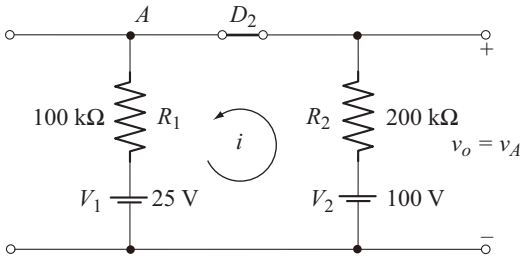


Fig. A

Applying KVL to the path of i

$$V_1 + R_1 i + R_2 i - V_2 = 0$$

$$\therefore \quad i = \frac{V_2 - V_1}{R_1 + R_2}$$

Voltage at point *A*

Applying KVL to the second branch

$$v_o + i R_2 - V_2 = 0$$

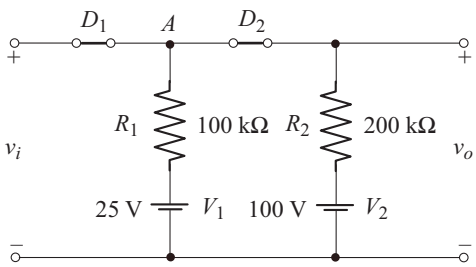
$$\therefore \quad v_A = v_o = - i R_2 + V_2$$

$$= \frac{-(V_2 - V_1) R_2}{R_1 + R_2} + V_2$$

$$= \frac{-(100\text{ V} - 25\text{ V})200\text{ kW}}{100\text{ kW} + 200\text{ kW}} + 100\text{ V}$$

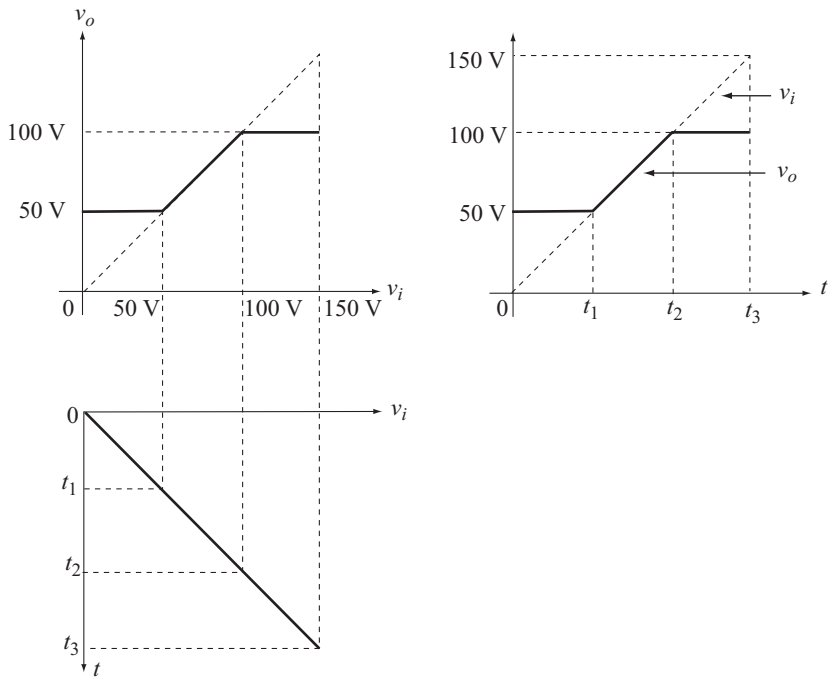
$$v_A = 50\text{ V}$$

This situation (D_1 off, D_2 on) continues until v_i reaches 50 V, just beyond which D_1 turns on and D_2 remains on and $v_o = v_i = v_A$. The equivalent circuit is shown below.



This situation continues until v_i *or* v_A reaches 100 V beyond which point D_2 turns off. Hence, D_1 is on and D_2 is *off* and v_o = 100 V.

The transfer characteristics and input-output waveforms are shown below:

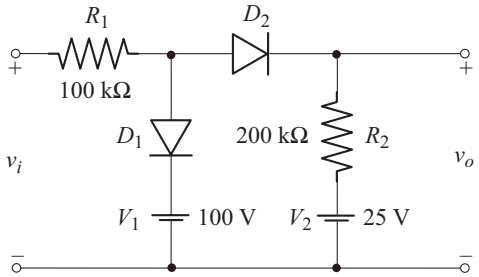


The operation of the circuit is summarised in the table given below.

Input	*Output*	*Diode status*
$v_i \leq 50$ V	$v_o = 50$ V	D_1 off, D_2 on
50 V $< v_i \leq 100$ V	$v_o = v_i$	D_1 on, D_2 on
$v_i > 100$ V	$v_o = 100$ V	D_1 on, D_2 off

Example 1.43

Repeat Example 1.42 for the circuit shown.



Solution

For $v_i < 25$ V, both D_1 and D_2 are off. Therefore, $v_o = 25$ V.

For v_i just exceeding 25 V, D_2 turns on and D_1 remains off. The equivalent circuit under this condition is shown in Fig. (A).

Applying KVL,

$$v_i - i\,(R_1 + R_2) - V_2 = 0$$

$$\therefore \quad i = \frac{v_i - V_2}{R_1 + R_2}$$

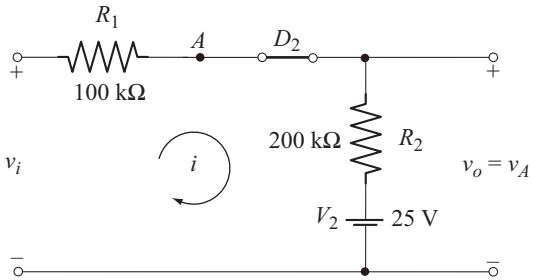


Fig. A

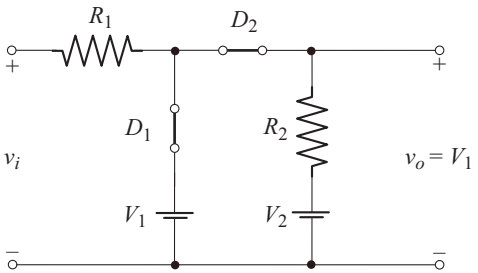


Fig. B

$$v_o = i R_2 + V_2$$

$$= \frac{R_2}{R_1 + R_2}\,(v_i - 25\text{V}) + 25\text{ V}$$

$$= \frac{2}{3}\,(v_i - 25\text{V}) + 25\text{ V}$$

The slope of the transfer characteristic is $\frac{2}{3}$. This situation continues until v_o or v_A reaches 100 V, beyond which D_1 also turns on. Let us use the above equation to calculate the value of v_i when $v_o = 100$ V.

$$100\text{ V} = \frac{2}{3}\,(v_i - 25\text{V}) + 25\text{ V}$$

$$\therefore \quad v_i = 75\text{ V} \times \frac{3}{2} + 25\text{ V}$$

$$= 137.5\text{ V}$$

Thus, when v_i reaches 137.5 volts, v_A reaches 100 V, beyond which D_1 begins to conduct.

$\therefore$ For $v_i > 137.5$ V, D_1 on and D_2 on and $v_o = 100$ V.

The equivalent circuit is shown in Fig. (B).

These results are graphically illustrated in Fig. (C).

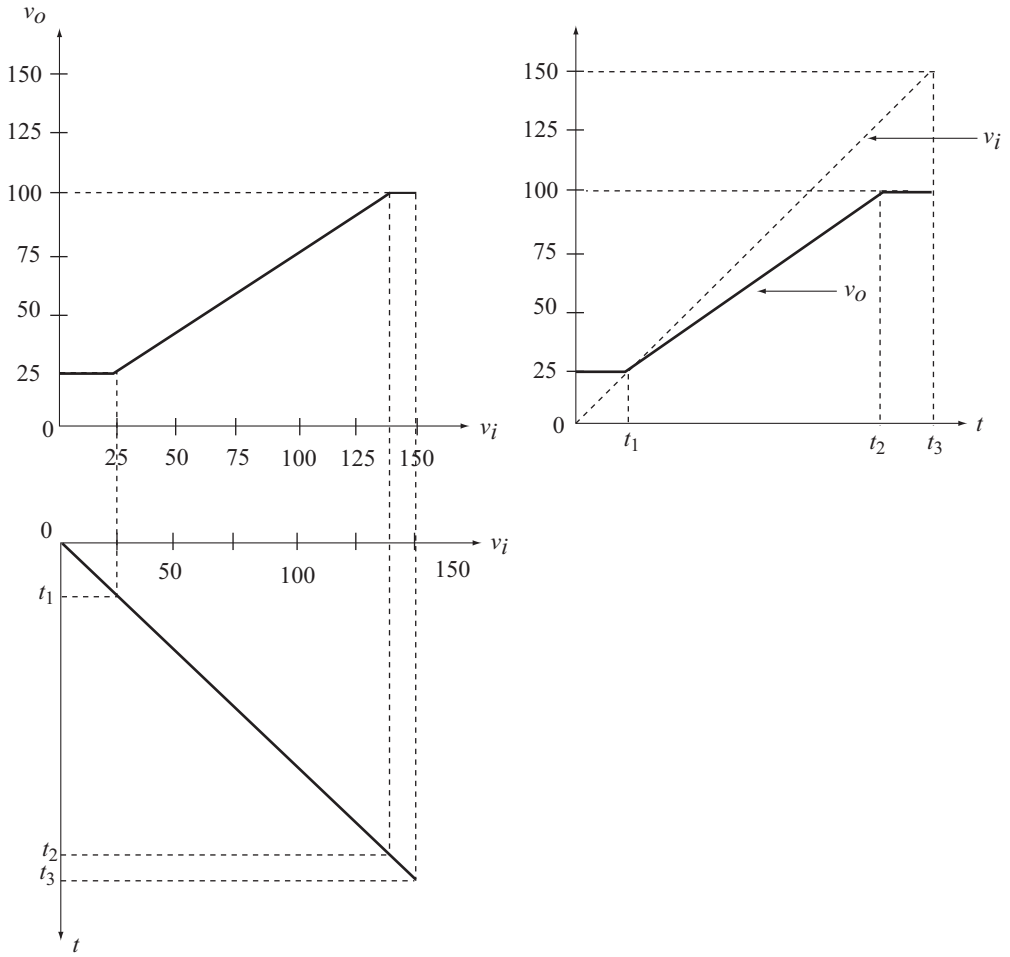


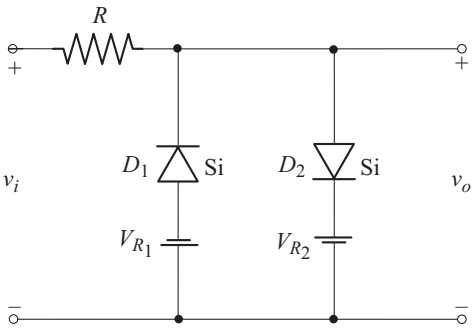
Fig. C

The circuit operation is summarised in the following table

Input	*Output*	*Slope*	*Diode status*
$v_i < 25$ V	$v_o = 25$ V	zero	D_1 off, D_2 off
$25\text{ V} \le v_i \le 137.5$ V	$v_i = \frac{2}{3}(v_i - 25\text{ V}) + 25$ V	slope = $\frac{2}{3}$	D_1 off, D_2 on
$v_i > 137.5$ V	$v_o = 100$ V	zero	D_1 on, D_2 on

Example 1.44

The circuit shown is used to square a 10 kHz sinusoidal with a peak amplitude of 50 V. Find V_{R_1} and V_{R_2}, if it is desired that the output voltage be flat for 90 % of the time. Assume $r_f = 100\ \Omega$, $R_r = 100\ \text{k}\Omega$ for the diodes. What is the reasonable value of R ?



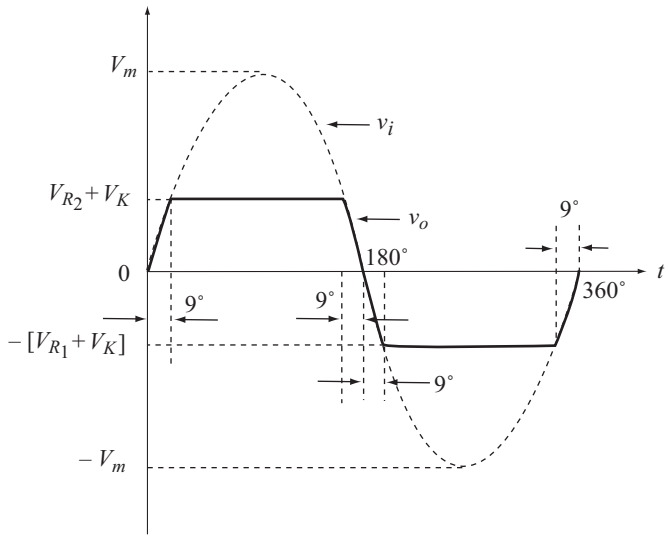
Solution

$$v_i = 50 \sin \theta$$

It is required that the output be flat for 90 % of the time. Now 100 % of the time corresponds to 360º and hence 90 % of the time corresponds to

$$360^\circ \times \frac{90}{100} = 324^\circ$$

In otherwords $v_o = v_i$ for 360º – 324º = 36º. This 36º is spread over four time segments as shown below:



Observe that the sinusoid becomes flat at 9º. Value of v_i at $\theta = 9º$ is

$$v_i = 50 \sin 9º = 7.82 \text{ V}$$

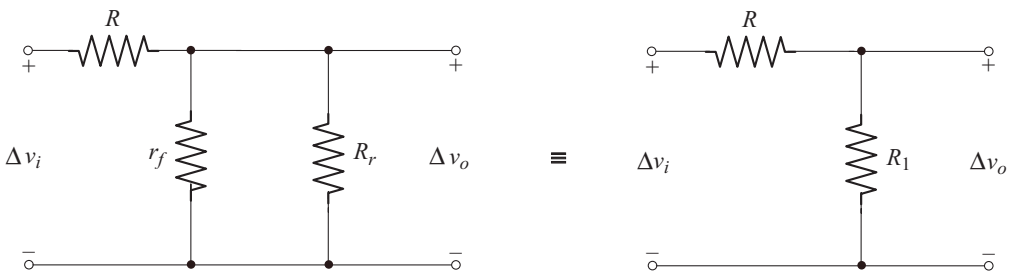
$$V_{R_1} + V_K = 7.82 \text{ V} \quad \text{and} \quad -[V_{R_2} + V_K] = -7.82 \text{ V}$$

For symmetrical clipping, $V_{R_1} = V_{R_2}$

$\therefore$ $V_{R_1} = V_{R_2} = 7.82 \text{ V} - 0.7 \text{ V} = 7.12 \text{ V}$

To find the value of *R*

Consider the equivalent circuit when D_1 is on and D_2 is off. Replace D_1 by r_f and D_2 by R_r.



$$R_1 = r_f \,||\, R_r = 0.1 \text{ k}\Omega \,||\, 100 \text{ k}\Omega = 0.099 \text{ k}\Omega$$

$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = \frac{R_1}{R + R_1}$$

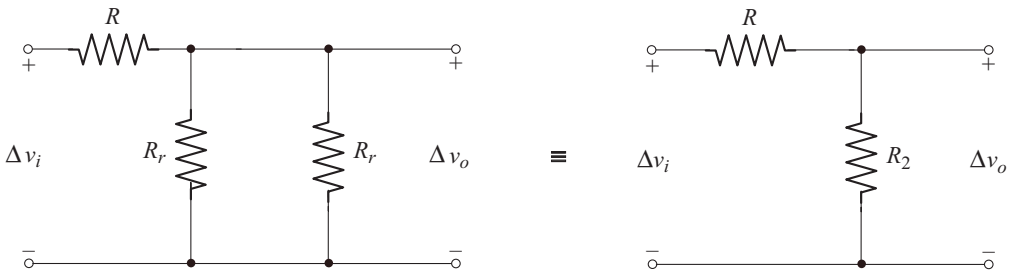
When either of the diodes conduct, slope should be zero. This requires that,

$$R \gg R_1$$

Let $R = K R_1$

or $$K = \frac{R}{R_1} \qquad \text{(A)}$$

Now let us consider the equivalent circuit when both diodes are off.



$$R_2 = R_r \,||\, R_r = \frac{R_r}{2} = 50 \text{ k}\Omega$$

$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = \frac{R_2}{R + R_2}$$

When both the diodes are off, slope should be unity. This requiers that

$$R_2 \gg R$$

Let $$R_2 = K R$$

or $$K = \frac{R_2}{R} \qquad \text{(B)}$$

Combining Equations (A) and (B)

$$\frac{R}{R_1} = \frac{R_2}{R}$$

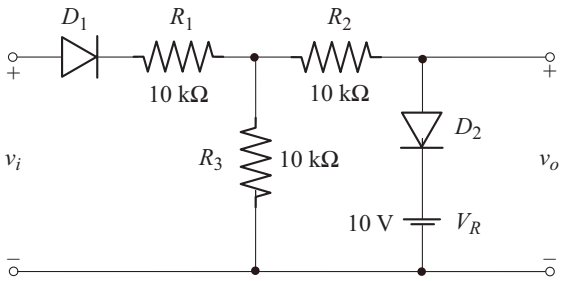
which gives $$R = \sqrt{R_2 \times R_1}$$

$$= \sqrt{50\ \text{k}\Omega \times 0.099\ \text{k}\Omega}$$

$$= 2.22\ \text{k}\Omega$$

Example 1.45

Plot the transfer characteristic of the circuit shown assuming ideal diodes and write the transfer characteristic equations. Sketch v_o if $v_i = 40 \sin \omega t$.



Solution

For $v_i < 0$, both D_1 and D_2 are *off*. Therefore, $v_o = 0$.

For $v_i \geq 0$, D_1 is *on*, D_2 is *off* and the equivalent circuit is shown in Fig. (A).

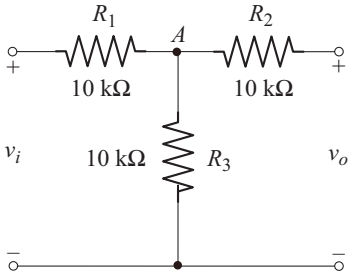


Fig. A

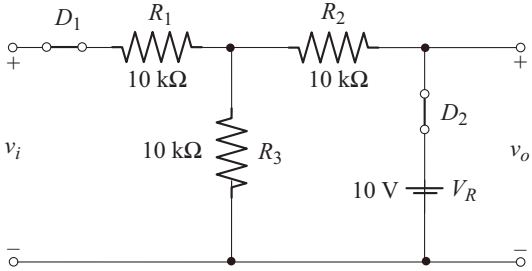


Fig. B

Since the diodes are ideal, $r_f = 0$, $R_r = \infty$ and $V_K = 0$.

$$v_o = v_A = \frac{R_3}{R_1 + R_3} \; v_i = \frac{v_i}{2}$$

$$\therefore \qquad \frac{v_o}{v_i} = \frac{1}{2} \qquad \text{(A)}$$

This situation continues until v_o reaches 10 V beyond which D_2 begins to conduct. Let us now compute v_i when v_o reaches 10 V. From Equation (A)

$$v_o = \frac{v_i}{2}$$

$$\therefore \qquad v_i = 2\, v_o = 2 \times 10 \text{ V} = 20 \text{ V}$$

For $v_i \geq 20$ volts, D_2 begins to conduct and $\therefore\ v_o = 10$ V. The equivalent circuit is shown in Fig. (B).

The transfer equations are, $v_o = \begin{cases} 0 & \text{for } v_i < 0 \\ \dfrac{v_i}{2} & \text{for } 0 \leq v_i < 20 \text{ V} \\ 10 \text{ V} & \text{for } v_i \geq 20 \text{ V} \end{cases}$

The transfer characteristic is shown in Fig. (C) and the output waveform is shown in Fig. (D) for $v_i = 40 \sin \omega t$.

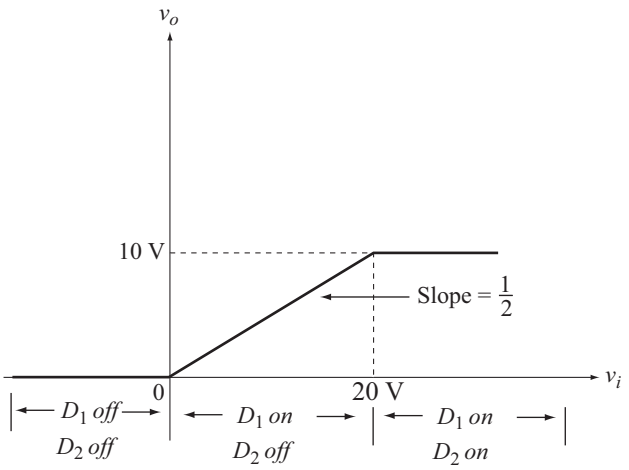


Fig. C

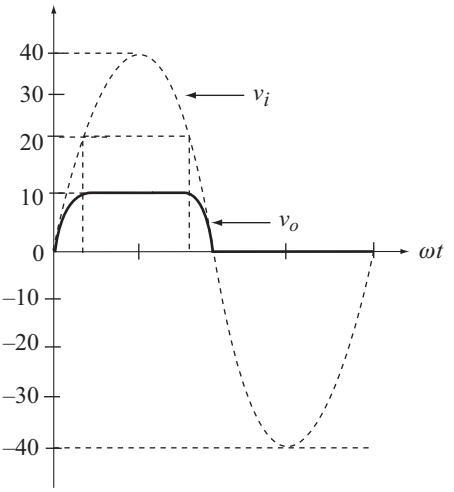
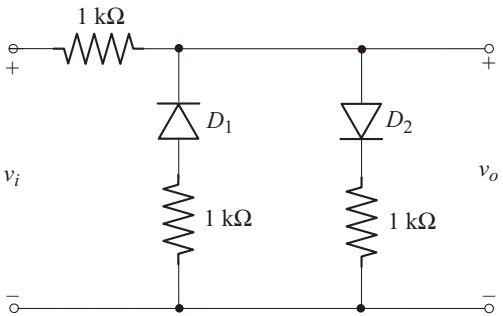


Fig. D

Example 1.46

Plot the transfer characteristic for the circuit shown and write the transfer characteristic equations. Sketch v_o if $v_i = 40 \sin \omega t$. Assume $V_K = 1$ V for the diodes.



Solution

For $v_i \leq -1$ V, D_1 is *on*, D_2 is *off* and the equivalent circuit is shown in Fig. (A).

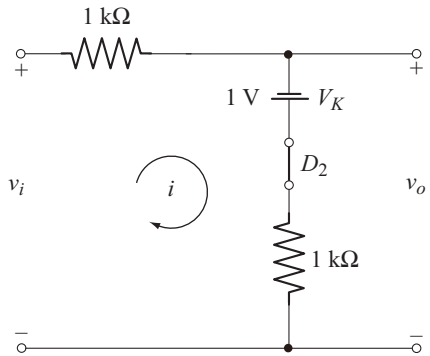


Fig. A

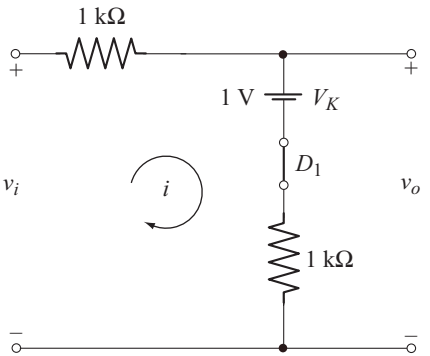


Fig. B

Applying KVL to the circuit of Fig. A.

$$v_i - i\,(1\ \text{k}\Omega) + V_K - i\,(1\ \text{k}\Omega) = 0$$

$$\therefore \quad i = \frac{v_i + V_K}{2\ \text{k}\Omega}$$

Also $v_o + V_K - i\,(1\ \text{k}\Omega) = 0$

$$v_0 = -V_K + i\,(1\ \text{k}\Omega)$$

$$= -V_K + (v_i + V_K)\left(\frac{1\ \text{k}\Omega}{2\ \text{k}\Omega}\right)$$

$$v_o = \frac{1}{2}\,(v_i - V_K) \qquad \text{(A)}$$

For $v_i \geq 1$ V, D_1 is *off*, D_2 is *on* and the equivalent circuit is shown Fig. (B).

$$v_o = V_K + i\,(1\ \text{k}\Omega)$$

But $$i = \frac{v_i - V_K}{2\ \text{k}\Omega}$$

We get $$v_o = \frac{1}{2}\,(v_i + V_K) \qquad \text{(B)}$$

For $-1\ \text{V} < v_i < 1\ \text{V}$, both D_1 and D_2 are off. Therefore,

$$v_o = v_i \qquad \text{(C)}$$

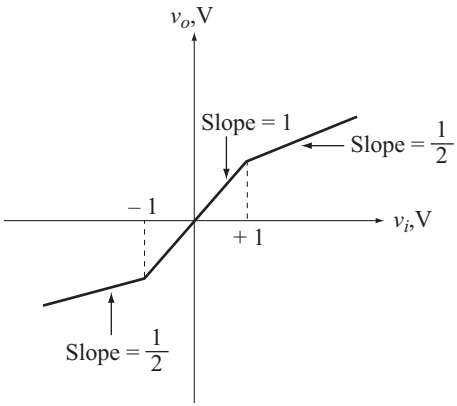
The transfer characteristic equations are

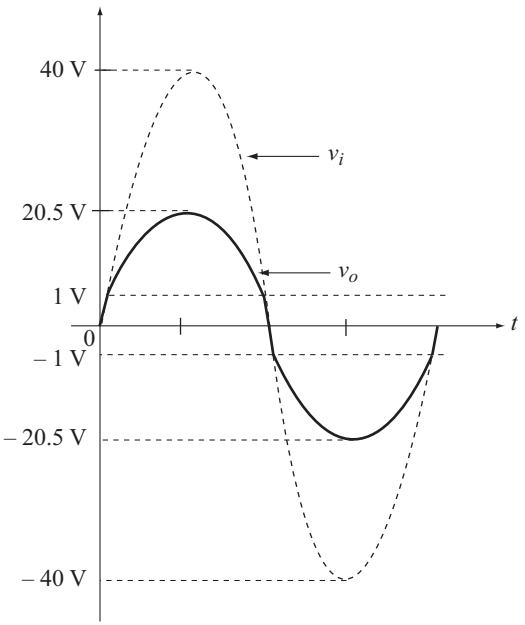
$$v_o = \begin{cases} \frac{1}{2}(v_i - 1\ \text{V}) & \text{for } v_i \leq -1\ \text{V} \\ v_i & \text{for } -1\ \text{V} < v_i < 1\ \text{V} \\ \frac{1}{2}(v_i + 1\ \text{V}) & \text{for } v_i \geq 1\ \text{V} \end{cases}$$

$\therefore$ From Equation (A), $$v_{o\min} = \frac{1}{2}\,(v_{i\min} - 1) = \frac{1}{2}\,(-40 - 1) = -20.5\ \text{V}$$

$\therefore$ From Equation (B), $$v_{o\max} = \frac{1}{2}\,(v_{i\max} + 1) = \frac{1}{2}\,(40 + 1) = 20.5\ \text{V}$$

The transfer characteristic and waveform of v_o are shown below.





Example 1.47

Repeat example 1.46 taking $V_K = 0$ V for the diodes.

Solution

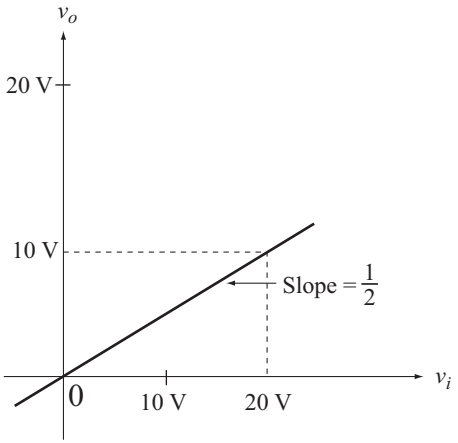
Since $V_K = 0$ V, from Equations (A), (B) and (C) of example 1.46, we find that

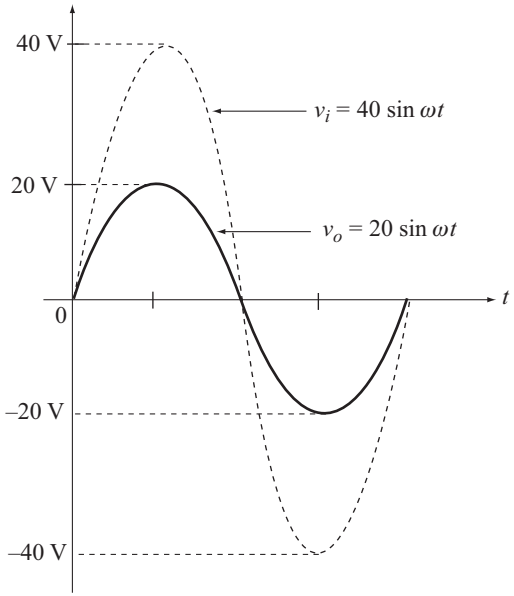
$$v_o = \frac{1}{2} v_i \quad \text{for all } v_i$$

Since $v_i = 40 \sin \omega t$ V

We get $v_o = 20 \sin \omega t$ V for all v_i

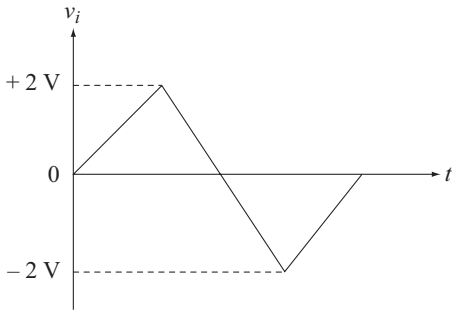
The transfer characteristic and waveform of v_o are shown below.

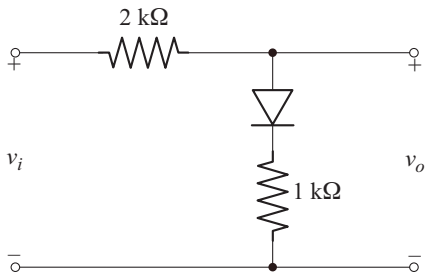




Example 1.48

Assuming an ideal diode in the circuit given below, draw the the output voltage waveform for the input signal given.





Solution

For $v_i \geq 0$, diode conducts. The equivalent circuit is shown in Fig. A.

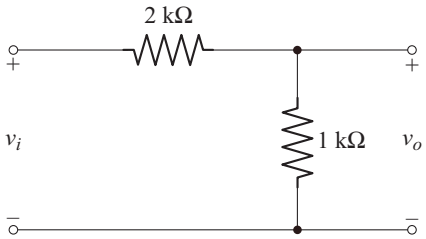


Fig. A

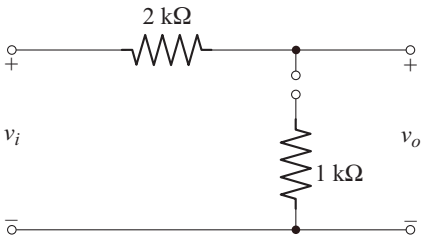


Fig. B

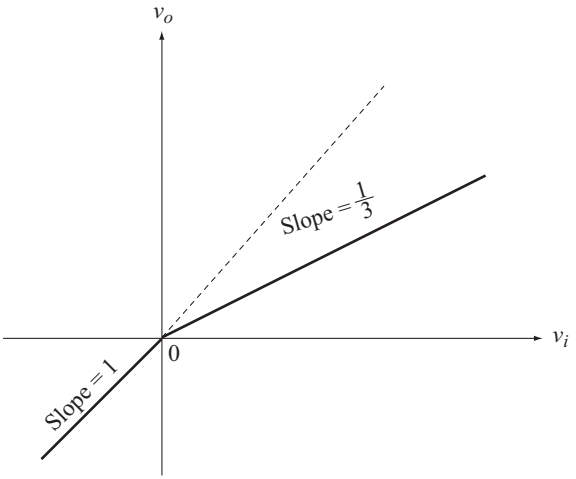
$$v_o = \left[\frac{v_i}{2\ \text{k}\Omega + 1\ \text{k}\Omega}\right] (1\ \text{k}\Omega) = \frac{1}{3}\ v_i$$

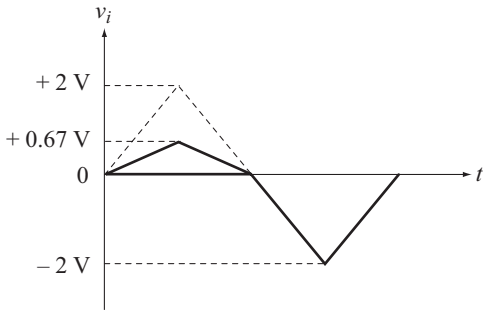
$$v_{o\max} = \frac{1}{3}\ v_{i\max}$$

$$v_{i\max} = 2\ \text{V}$$

$$\therefore \quad v_{o\max} = \frac{1}{3}(2\ \text{V}) = 0.67\ \text{V}.$$

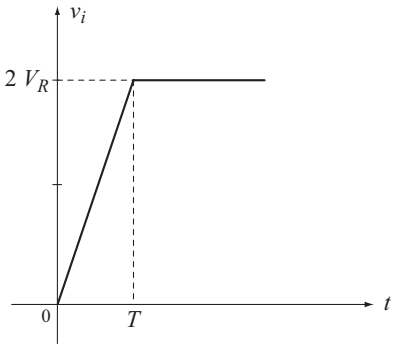
For $v_i < 0$, diode turns off. The equivalent circuit is shown in Fig. B.
From the equivalent circuit we find that $v_o = v_i$.
The transfer characteristic and the output waveform are shown below.

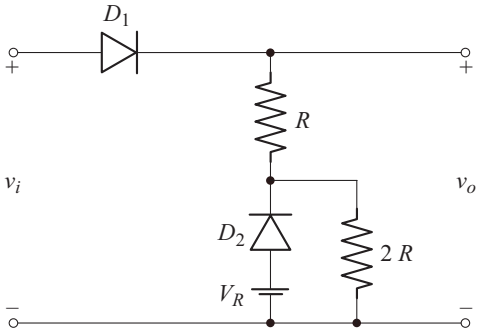




Example 1.49

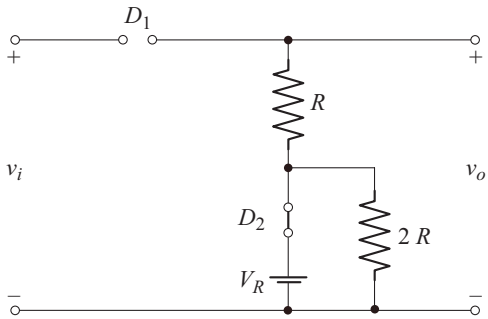
For the circuit shown below sketch the transfer characteristic and output waveform. Assume ideal diodes.





Solution

When $v_i = 0$, D_1 is off and D_2 is on. The equivalent circuit is shown below. This situation continues as long as $v_i < V_R$.



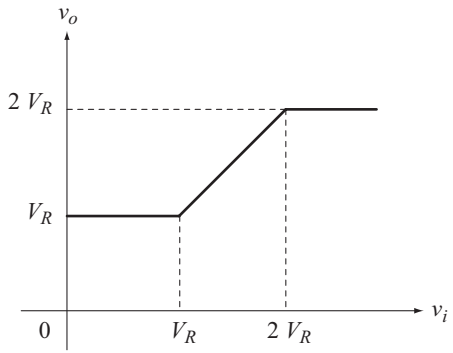
From the equivalent circuit

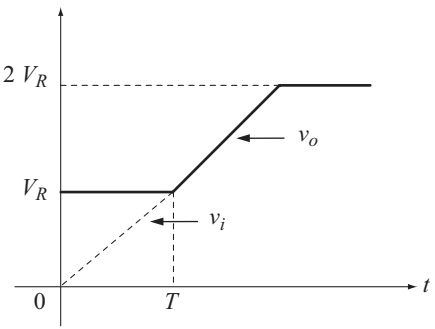
$$v_o = V_R \quad \text{for } v_i < V_R$$

D_1 conducts when v_i exceeds V_R. Under this condition, $v_o = v_i$

$$\therefore \quad v_o = \begin{cases} V_R & \text{for } 0 < v_i < V_R \\ v_i & \text{for } v_i \geq V_R \end{cases}$$

The transfer characteristics and output waveform are shown below.





Example 1.50

Sketch and explain the circuit of a double ended clipper using Si diodes which limits the output between ± 10 V.

Solution:

The operation of double ended clipper which limits both positive and negative peaks is given in section 1.22.

Since clipping is symmetrical, $V_{R_1} = V_{R_2}$

$$\therefore \quad V_{R_2} + V_K = 10 \text{ V} \quad \text{and} \quad -[V_{R_1} + V_K] = -10 \text{ V}$$

$$\Rightarrow \quad V_{R_1} = V_{R_2} = 9.3 \text{ V}$$

Example 1.51

Sketch and explain the circuit of a double ended clipper using Si diodes which limits the output between 5 V and 8 V.

Solution

The operation of double ended clipper which limits the output between two positive levels is given in section 1.21.

$$V_{R_1} - V_K = 5 \text{ V}$$

$$\Rightarrow \quad V_{R_1} = 5 \text{ V} + V_K = 5.7 \text{ V} \quad \text{and}$$

$$V_{R_2} + V_K = 8 \text{ V} \quad \Rightarrow \quad V_{R_2} = 7.3 \text{ V}$$

◆ 1.23 CLAMPING CIRCUITS

Clamping circuits are used to add dc level to the input signal. Clamping circuits are also called dc inserters or dc restorers. Clamping circuit uses diode, resistor and capacitor.

◆ 1.24 NEGATIVE CLAMPER

Figure 1.46 shows the circuit of negative clamper.

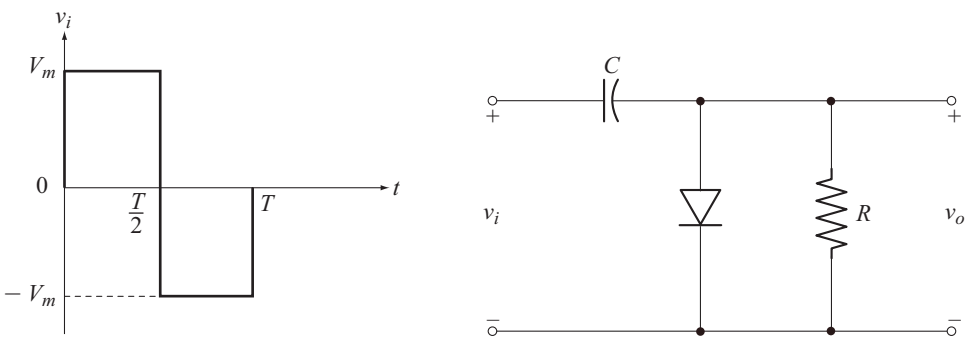


Fig. 1.46 Negative clamper

The input is a square wave which swings between $\pm V_m$ with a period $T = \frac{1}{f}$. The input can also be any other periodic waveform such as sine, triangular etc.

During the positive half cycle of v_i, the diode conducts and charges the capacitor. The charging time constant is

$$\tau_f = r_f C \tag{1.74}$$

Since the diode forward resistance is very small ($r_f \approx 0$), $\tau_f \ll \frac{T}{2}$ and hence the capacitor gets charged quickly to the peak value V_m of the input signal v_i. The equivalent circuit during diode conduction is shown in Fig. 1.47(a).

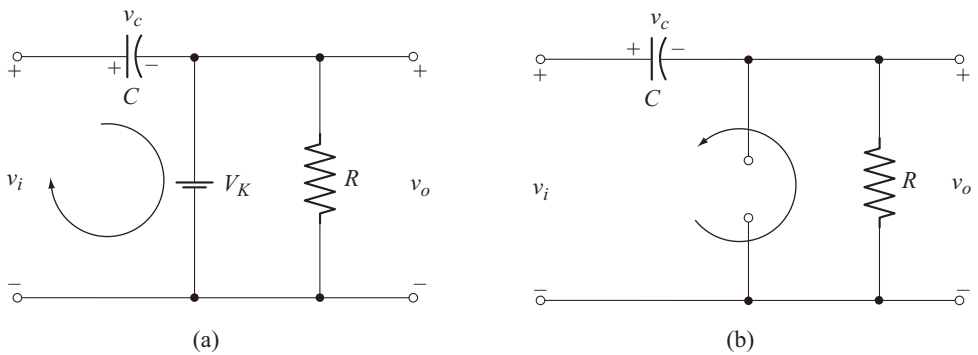


Fig. 1.47 Equivalent circuit
(a) When diode is on
(b) When diode is off

Writing KVL equation to the circuit of Fig. 1.47(a), we have

$$v_i - v_c - V_K = 0$$

$$v_c = v_i - V_K \tag{1.75}$$

When $v_i = V_m$

$$v_c = V_m - V_K \tag{1.76}$$

Note that the left plate of the capacitor is positive since the charging current enters that plate.

During the negative half cycle of v_i, the diode turns off. Now the capacitor discharges into R. The discharge time constant is

$$\tau = R C \tag{1.77}$$

The capacitor should not loose much of charge during discharge. To meet this requirement, the values of R and C are selected such that

$$5\tau \gg \frac{T}{2} \tag{1.78}$$

$$5\,RC \gg \frac{T}{2} \tag{1.79}$$

The value of five times the time constant (5 *RC*) is made much greater than half period (T/2) of the periodic input signal.

The equivalent circuit during capacitor discharge is shown in Fig. 1.47(b). Writing KVL equation to the circuit of Fig. 1.47(b) we have

$$v_i - v_c - v_o = 0$$

$$v_o = v_i - v_c \tag{1.80}$$

Since

$$v_c = V_m - V_K$$

$$v_o = v_i - [V_m - V_K] \tag{1.81}$$

Observe from Equation (1.81) that, the circuit adds a dc level of $-[V_m - V_K]$ to the input signal v_i. The output voltage levels corresponding to different input voltage levels are listed in Table 1.6.

Table 1.6 Output voltage levels of negative clamper

Input voltage level v_i	***Output voltage level***	
	Practical diode $v_o = v_i - [V_m - V_K]$	***Ideal diode*** $v_o = v_i - V_m$
0	$-[V_m - V_K]$	$-V_m$
V_m	V_K	0
$-V_m$	$-2V_m + V_K$	$-2V_m$

The output voltage waveform is shown in Fig. 1.48.

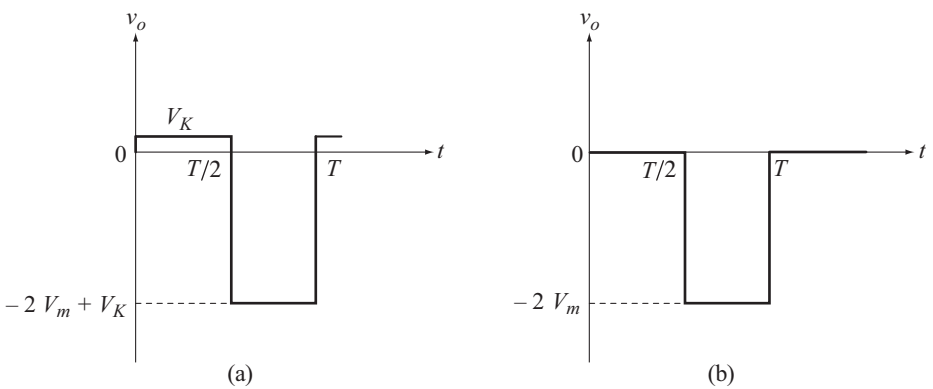


Fig. 1.48 Output voltage waveform
(a) With practical diode
(b) With ideal diode

Since the circuit adds negative dc level, it is called negative clamper. The circuit is also called positive peak clamper since the positive peak of the applied signal is clamped at 0 V as shown in Fig. 1.48(b). Also from Fig. 1.48 we observe that

$$\text{peak-to-peak input voltage} = \text{peak-to-peak output voltage} = 2\,V_m$$

Therefore in a clamper circuit

peak-to-peak output voltage is equal to peak-to-peak input voltage.

◆ 1.25 POSITIVE CLAMPER

Figure 1.49 shows the circuit of positive clamper which is obtained by simply reversing the diode in the negative clamper circuit of Fig. 1.46.

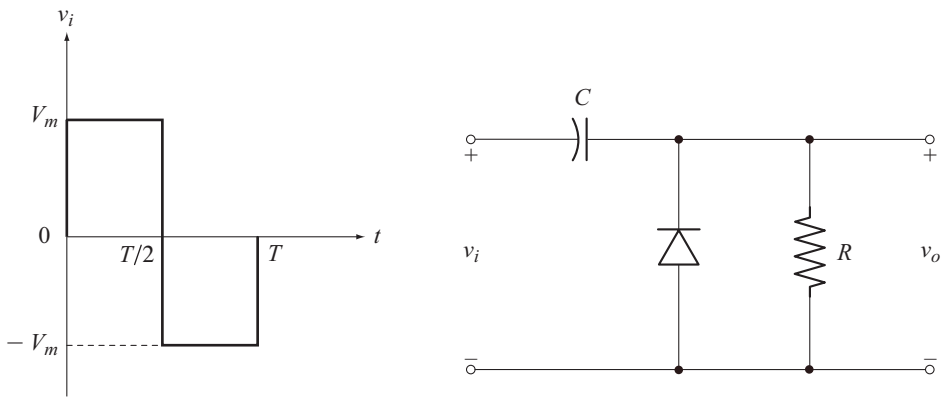


Fig. 1.49 Positive clamper

In this circuit the diode conducts during the negative half cycle of v_i and charges the capacitor to the peak value V_m, with right plate positive. Performing the analysis as outlined in the previous section, it can be shown that the circuit of Fig. 1.49 adds a dc voltage of approximately V_m to the input signal. The output voltage levels are listed in Table 1.7.

Table 1.7 Output voltage levels of positive clamper

Input voltage level v_i	***Output voltage level***	
	Practical diode $v_o = v_i + [V_m - V_K]$	***Ideal diode*** $v_o = v_i + V_m$
0	$V_m - V_K$	V_m
V_m	$2V_m - V_K$	$2\,V_m$
$-V_m$	$-V_K$	0

The output voltage waveform is shown in Fig. 1.50.

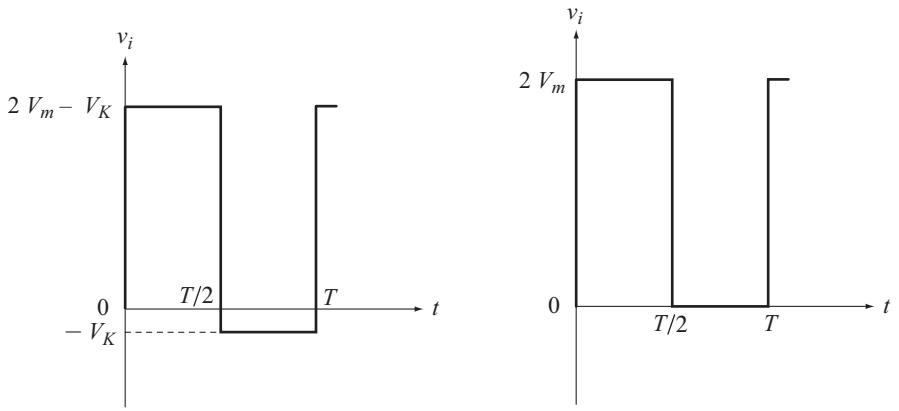


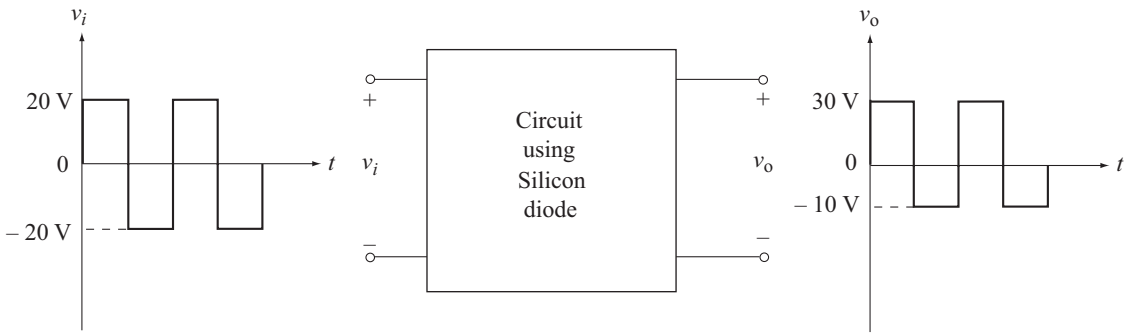
Fig. 1.50 Output voltage waveform
(a) With practical diode
(b) With ideal diode

Since the circuit adds positive dc level to the input signal, it is called positive clamper. The circuit is also called negative peak clamper, since the negative peak of the applied signal is clamped at 0 V as shown in Fig. 1.50. Once again we observe from Fig. 1.50 that, the peak-to-peak output voltage equals the peak-to-peak input voltage.

If clamping is desired at a voltage other than zero, a reference voltage V_R must be included in series with diode. Such circuits are considered later in numerical examples.

Example 1.52

Design a suitable circuit represented by the box shown below which has input and output waveforms as indicated.

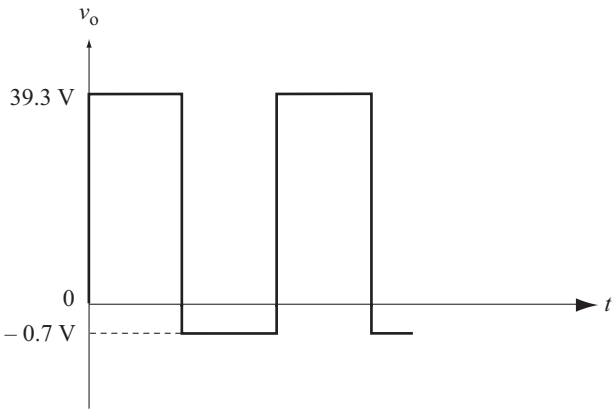


Solution

Comparing the waveforms of v_i and v_o, we find that, v_o can be obtained by shifting up v_i by 10 V. To do so, a positive dc voltage must be added to v_i. Hence we have to design a positive clamper circuit.

Let us sketch the output of positive clamper circuit of Fig. 1.49 for the given input voltage. (Refer Table 1.7)

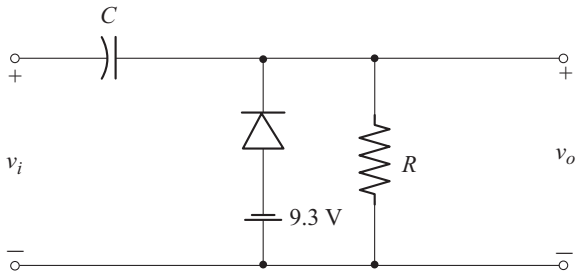
$$V_m = 20 \text{ V} \quad V_K = 0.7 \text{ V}$$



But the desired output voltage has a positive peak of 30 V. Therefore, the waveform shown above has to be shifted down by 9.3 V. This can be done by using an additional dc source V_R, whose value is given by

$$39.3 \text{ V} + V_R = 30 \text{ V}$$
$$V_R = -9.3 \text{ V}$$

This dc voltage should be placed in series with the diode. The required clamper circuit is shown below.

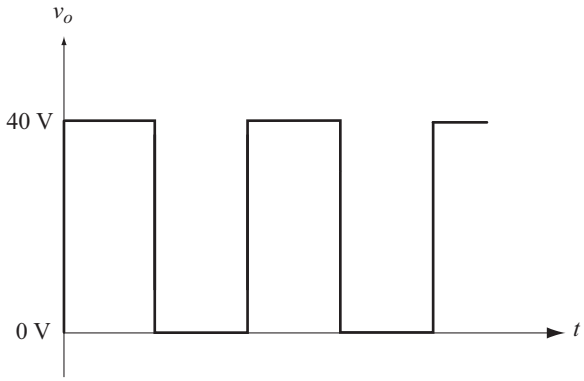


Example 1.53

Repeat Example 1.52 using ideal diode.

$$V_m = 20 \text{ V} \quad V_K = 0.$$

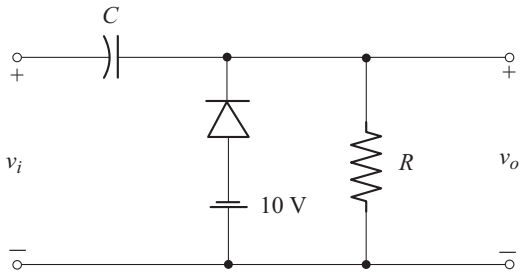
The output of positive clamper is shown below.



Since the required positive peak is 30 V,

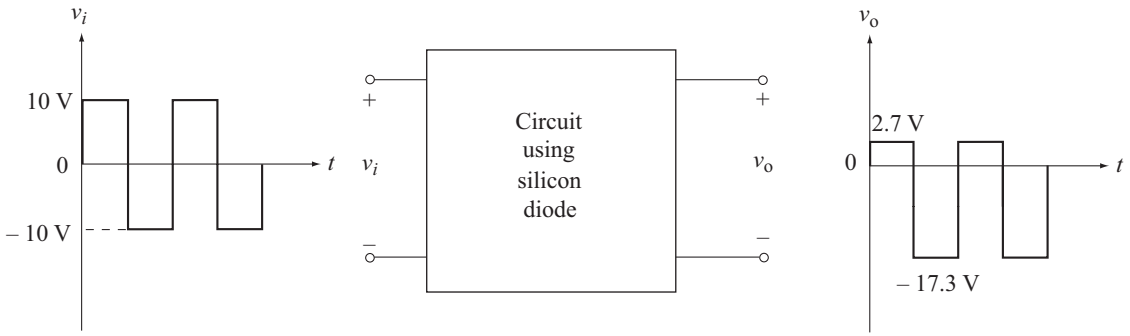
$$40 \text{ V} + V_R = 30 \text{ V}$$
$$V_R = -10 \text{ V}$$

The clamper circuit is shown below.



Example 1.54

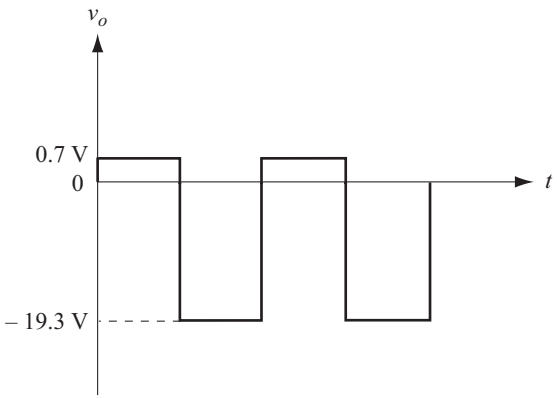
Design a suitable circuit represented by the box shown below which has the input and output waveforms as indicated.



Solution

Comparing the waveforms of v_i and v_o, we find that, v_o can be obtained by shifting down v_i by 7.3 V. To do so, a negative dc voltage must be added to v_i. Hence we have to design a negative clamper. The output of negative clamper of Fig. 1.46 for the given input is shown below. (Refer Table 1.6).

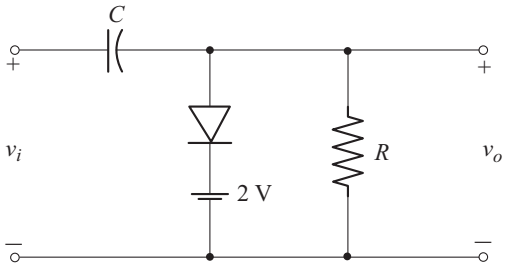
$$V_m = 10 \text{ V} \quad V_K = 0.7 \text{ V}$$



The desired output voltage has a positive peak of 2.7 V. Therefore the waveform shown above has to be shifted up by 2 V. This can be done by using an additional dc source V_R given by

$$0.7 \text{ V} + V_R = 2.7 \text{ V}$$
$$V_R = 2 \text{ V}$$

This dc voltage should be placed in series with the diode. The required clamper circuit is shown below.



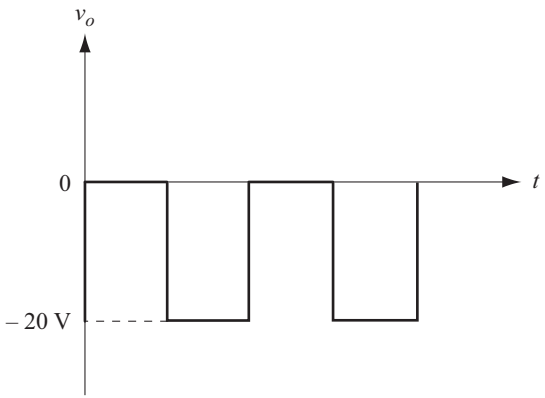
Example 1.55

Repeat Example 1.54 using ideal diode.

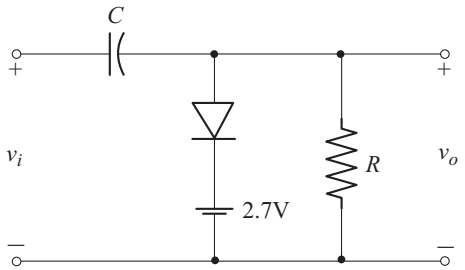
Solution

$$V_m = 10 \text{ V} \quad V_K = 0$$

The output of negative clamper is shown below.

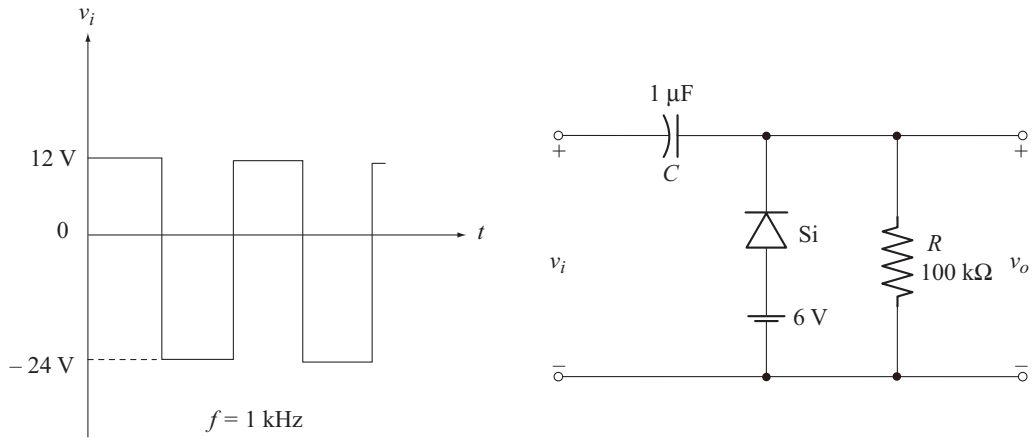


Since the required positive peak is 2.7 V, the waveform shown should be shifted up by 2.7 V. Therefore a dc source of voltage 2.7 V must be placed in series with the diode as shown below.



Example 1.56

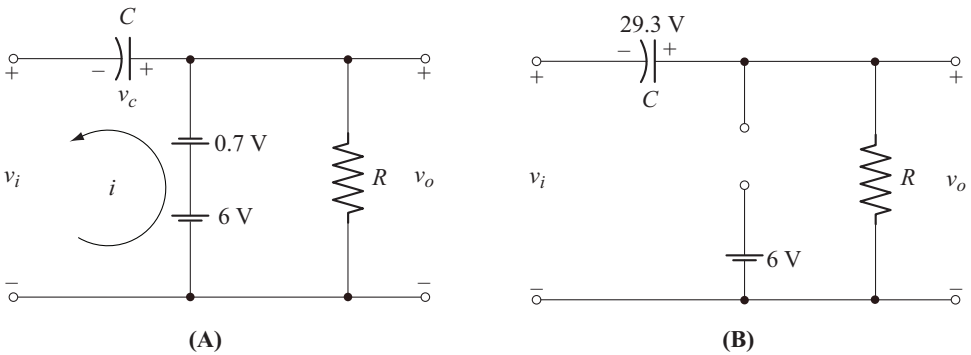
For the circuit shown below find and plot the waveform of v_o for the input indicated.



Solution

Step 1: To find the capacitor voltage when the diode is conducting.

Diode conducts when $v_i = -24$ V. The equivalent circuit is shown in Fig. A.



Applying KVL to the current path in the circuit of Fig. A we have

$$v_i + v_c + 0.7\text{ V} - 6\text{ V} = 0 \qquad \text{(A)}$$

$$v_c = -v_i + 5.3\text{ V}$$

When $v_i = -24$ V, the capacitor charges to

$$v_c = -(-24\text{ V}) + 5.3\text{ V} = 29.3\text{ V}$$

Note that the right plate of capacitor is positive.

Step 2: To find the output voltage levels when the diode is off

When $v_i = 12$ V, the diode is off. The equivalent circuit is shown in Fig. B.

KVL equation to the circuit of Fig. B is

$$v_i + 29.3\text{ V} - v_o = 0$$

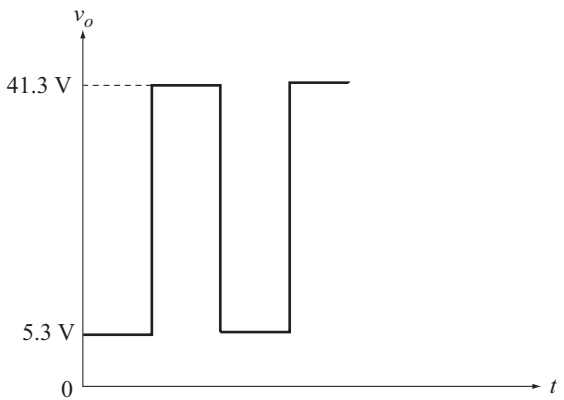
$$v_o = v_i + 29.3\text{ V} \qquad \text{(B)}$$

Observe from Equation (B) that, the circuit adds a dc level of 29.3 V to the input signal v_i. Let us find the output levels corresponding to the two input levels using Equation (B).

When $v_i = 12$ V, $v_o = 12\text{ V} + 29.3\text{ V} = 41.3\text{ V}$

When $v_i = -24$ V, $v_o = -24\text{ V} + 29.3\text{ V} = 5.3\text{ V}$

The output waveform is shown below.



Peak-to-peak input voltage = 12 V – (– 24 V) = 36 V

Peak-to-peak output voltage = 41.3 V – 5.3 V = 36 V

Note that peak-to-peak output voltage = peak-to-peak input voltage.

Example 1.57

Repeat example 1.56 assuming ideal diode.

Solution

For ideal diode, $V_K = 0$

From Equation (A),

$$v_c = -v_i + 6 \text{ V}$$

When $v_i = -24$ V

$$v_c = -(-24 \text{ V}) + 6 \text{ V} = 30 \text{ V}$$

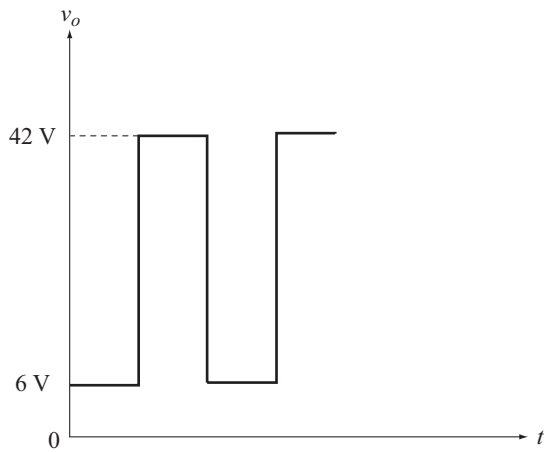
From Equation (B),

$$v_o = v_i + 30 \text{ V}$$

When $v_i = 12$ V, $v_o = 12 \text{ V} + 30 \text{ V} = 42 \text{ V}$

When $v_i = -24$ V, $v_o = -24 \text{ V} + 30 \text{ V} = 6 \text{ V}$

The output waveform is shown below.

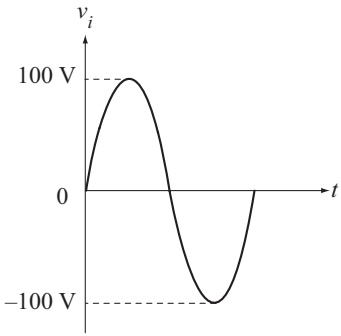


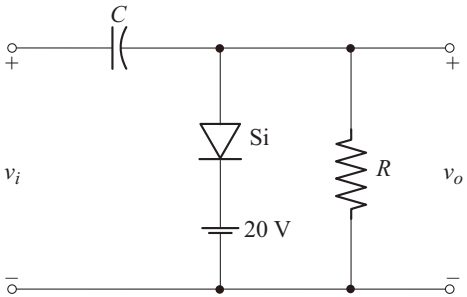
Once again we note that

Output peak-to-peak = input peak-to-peak = 36 V

Example 1.58

For the circuit shown find and plot the output waveform for the input indicated. Also sketch the output waveform assuming ideal diode.

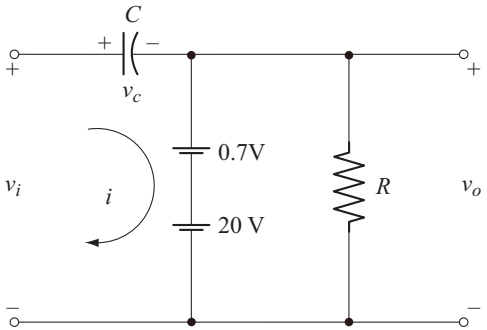




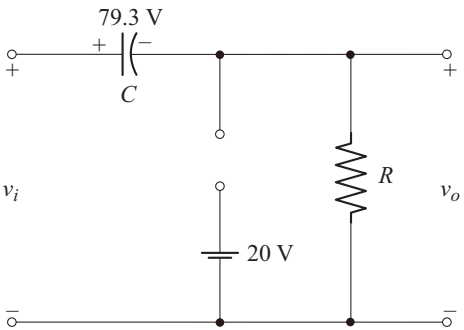
Solution

Step 1 : To find capacitor voltage when diode is conducting

Diode conducts during the positive half cycle of v_i. The equivalent circuit is shown in Fig. A.



(A)



(B)

Applying KVL to the current path in the circuit of Fig. A.

$$v_i - v_c - 0.7\text{ V} - 20\text{ V} = 0 \qquad \text{(A)}$$

$$v_c = v_i - 20.7\text{ V}$$

When v_i = 100 V, the capacitor charges to

$$v_c = 100\text{ V} - 20.7\text{ V} = 79.3\text{ V}$$

Step 2 : To find the output voltage levels when the diode is off

Diode turns off during the negative half cycle of v_i. The equivalent circuit is shown in Fig. B.

KVL equation to the circuit of Fig. B is

$$v_i - 79.3\text{ V} - v_o = 0$$

$$v_o = v_i - 79.3 \text{ V} \quad \text{(B)}$$

When $v_i = 100$ V, $v_o = 100 \text{ V} - 79.3 \text{ V} = 20.7 \text{ V}$

When $v_i = -100$ V, $v_o = -100 \text{ V} - 79.3 \text{ V} = -179.3 \text{ V}$

Output Waveform with Ideal Diode

From Equation (A),

$$v_c = v_i - 20 \text{ V}$$

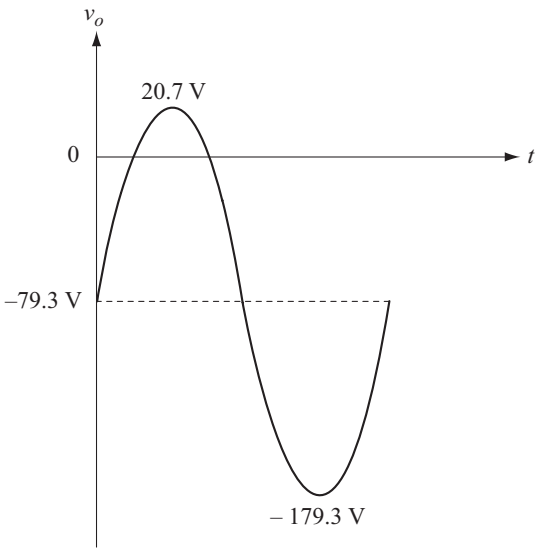
When $v_i = 100$ V, $v_c = 100 \text{ V} - 20 \text{ V} = 80 \text{ V}$

From Equation (B) $v_o = v_i - 80$ V

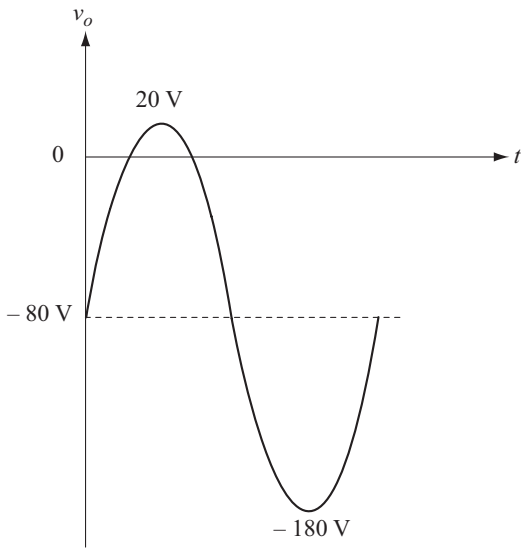
When $v_i = 100$ V, $v_o = 100 \text{ V} - 80 \text{ V} = 20 \text{ V}$

When $v_i = -100$ V, $v_o = -100 \text{ V} - 80 \text{ V} = -180 \text{ V}$

The output waveforms are shown below.



Output waveform with Si diode



Output waveform with ideal diode

Note that in each case

output peak-to-peak = input peak-to-peak = 200 V

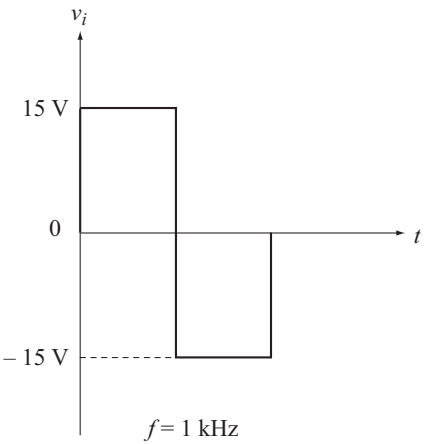
Example 1.59

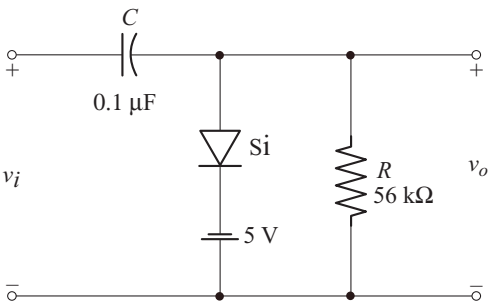
For the circuit shown below

(a) Calculate 5 τ

(b) Compare 5 τ with half period ($T/2$) of the applied signal

(c) Sketch the output waveform





Solution

(a) $\tau = RC = (56\ \text{k}\Omega)\ (0.1\ \mu\text{F}) = 5.6\ \text{ms}$

$5\ \tau = 5\ (5.6\ \text{mS}) = 28\ \text{mS}$

(b) $f = 1\ \text{kHz} \qquad T = \dfrac{1}{f}$

$$T = \frac{1}{1\ \text{kHz}} = 1\ \text{ms} \quad \Rightarrow \quad \frac{T}{2} = 0.5\ \text{ms}$$

$$\frac{5\tau}{\left[\frac{T}{2}\right]} = \frac{28\ \text{ms}}{0.5\ \text{ms}} = 56$$

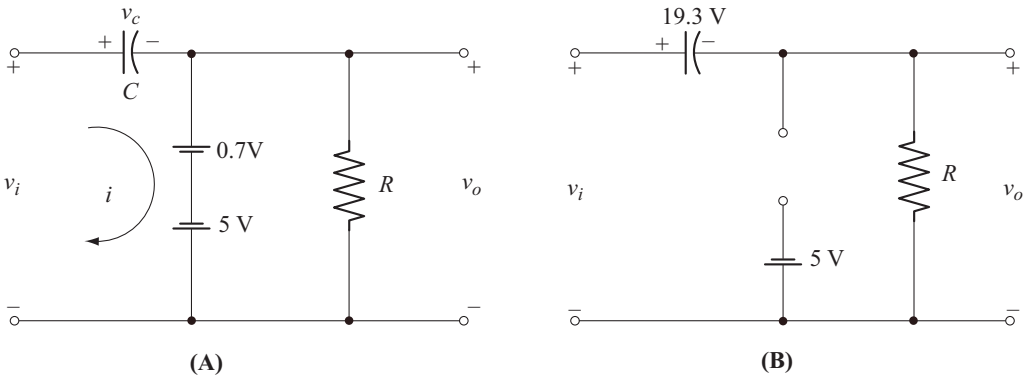
$$\therefore \qquad 5\tau = 56\ \left[\frac{T}{2}\right] \quad \Rightarrow \quad 5\tau \gg \frac{T}{2}$$

Due to this large time constant the discharge of the capacitor is very minimal when the diode is off.

(c) To find and plot v_o

Step 1: To find the capacitor voltage when the diode is conducting

Diode conducts when $v_i = 15$ V. The equivalent circuit is shown in Fig. A.



Applying KVL to the current path in the circuit of Fig. A, we have

$$v_i - v_c - 0.7\text{ V} + 5\text{ V} = 0$$

$$v_c = v_i + 4.3\text{ V}$$

When $v_i = 15$ V, the capacitor charges to

$$v_c = 15\text{ V} + 4.3\text{ V} = 19.3\text{ V}$$

Step 2: To find output voltage levels when the diode is off

Diode turns off when $v_i = -15$ V. The equivalent circuit is shown in Fig. B.

KVL equation to the circuit of Fig. B is

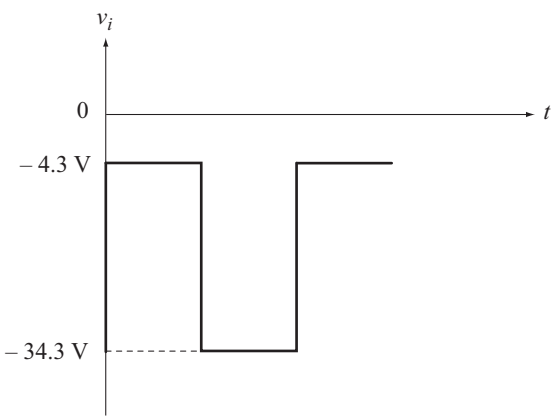
$$v_i - 19.3\text{ V} - v_0 = 0$$

$$v_0 = v_i - 19.3\text{ V}$$

When $v_i = 15$ V, $v_o = 15\text{ V} - 19.3\text{ V} = -4.3\text{ V}$

When $v_i = -15$ V, $v_o = -15\text{ V} - 19.3\text{ V} = -34.3\text{ V}$

The output waveform is shown below.



Note that, output peak-to-peak = input peak-to-peak = 30 V

Exercise Problems

1.1 A full-wave bridge rectifier using silicon diodes is supplying a resistive load of 1 kΩ. It is supplied from an ac source of 100 V at 50 Hz. Calculate

(a) DC output voltage

(b) DC load current

1.2 The input to a clipping circuit is a sine wave of peak value 25 V. Design the component values such that the output should have its positive peak clipped at 15 V and negative peak at – 18 V.

1.3 Design the values of R and C for a clamping circuit for which the input signal is a square wave of frequency 1 kHz.

1.4 Design a clamping circuit to obtain an output with positive peak at 20 V and negative peak at – 10 V. The input is a square wave of ± 15 V at 1 kHz. Assume silicon diode.

1.5 A shunt clipper employs a diode which has r_f = 100 Ω and R_r = 100 kΩ. Calculate the reasonable value of R.

Chapter 2

TRANSISTOR BIASING

Biasing a bipolar junction transistor essentially means establishing the desired value of collector-emitter voltage V_{CE} and the collector current I_C, to ensure that the amplifier will have the proper gain and input impedance with undistorted output voltage swing. These values of V_{CE} and I_C are together known as the *quiescent operating point* or *Q*-point.

Now, one of the basic problems with the transistor amplifier is establishing and maintaining proper values of quiescent V_{CE} and I_C in the circuit. A quiescent voltage or current refers to the values under dc conditions in the absence of any ac input signal. The quiescent value of voltages and currents are maintained by using configurations that assure stability against variations in temperature. Variations in temperature affects several critical transistor parameters such as reverse saturation current I_{CO}, base-emitter voltage in the active region V_{EE} and current gain β.

This chapter analyses various bias configurations and techniques for maintaining the quiescent operating point stable against variations in temperature. The concepts are introduced with a generous number of illustrative examples and in-depth analysis of different configurations.

◆ 2.1 THE OPERATING POINT

The transistor needs to be operated in an appropriate region of its characteristics depending on the application of the circuit in which it is being used. The dc currents and voltages in the circuit are established by using a resistive network along with a dc power supply. This process is called *biasing*.

Let us recollect the common-emitter output characteristics of an *n-p-n* transistor. The common emitter configuration and its output characteristics are shown in Fig. 2.1.

The three regions of operation of the transistor are termed as active region, cut-off region and saturation region.

The region in the characteristics shown in Fig. 2.1(b) above $I_B = 0$ mA and to the right of a few tenths of volts of V_{CE} is the active region. It is the region where you observe an increase in the collector current with increase in base current. The base-emitter junction is forward biased while the base-collector junction is reverse biased in this region.

The region where the base-emitter junction is reverse biased below 0.1 V for germanium and 0 V for silicon is the cut-off region. In this region, the emitter current is zero and the transistor is non-conducting. In this region the base-emitter junction as well as the base-collector junction is reverse biased.

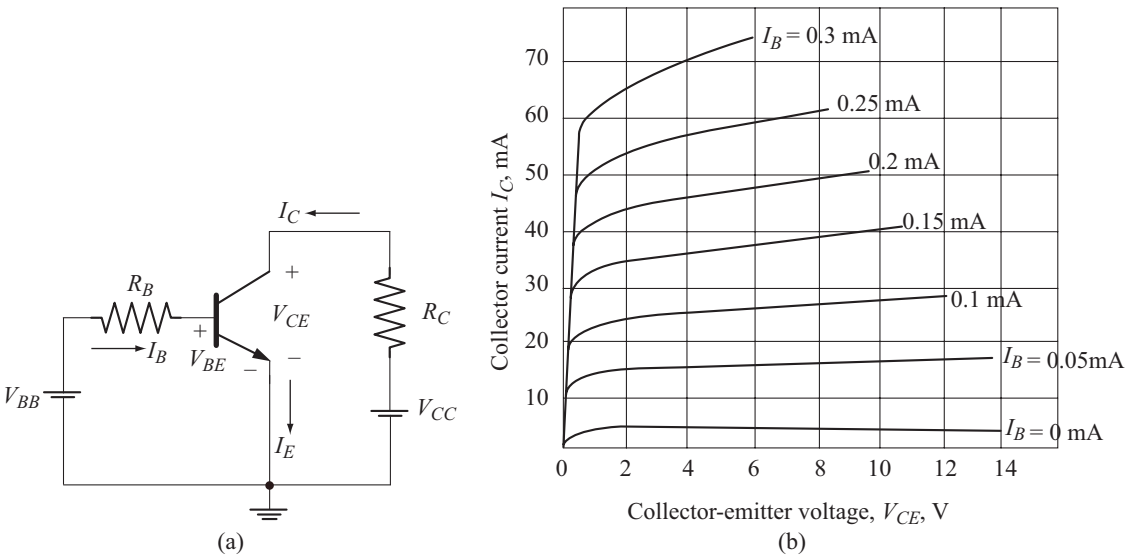


Fig. 2.1 The common-emitter configuration and its output characteristics

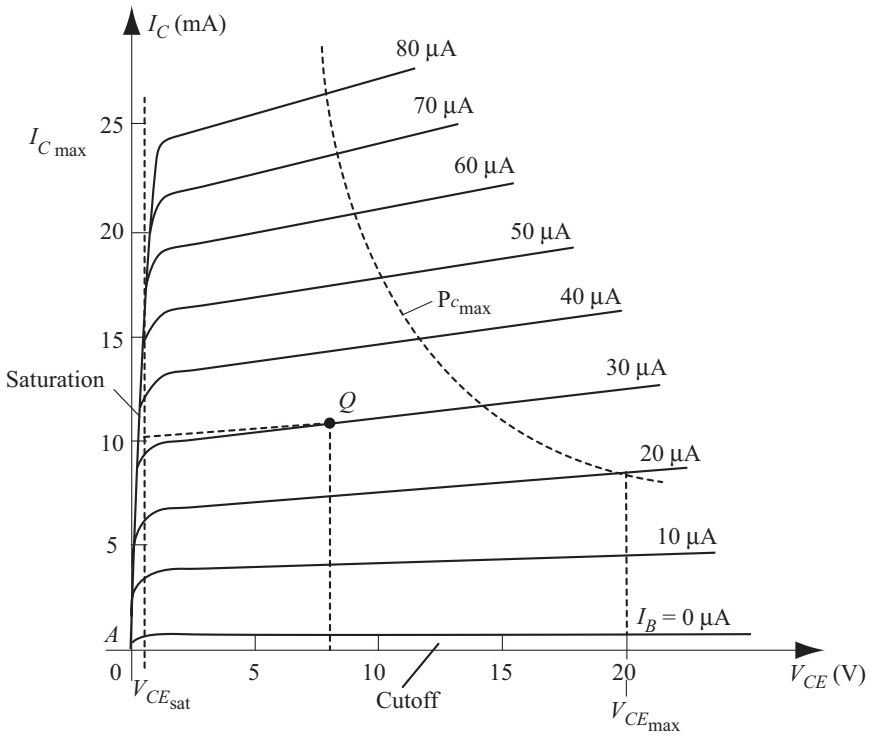


Fig. 2.2 Illustration of operating point

The region very close to $V_{CE} = 0$ where all the curves appear to merge and fall rapidly to the origin is called the *saturation region*. In this region, V_{CE} is a few tenths of volts while I_C is considerably large. In the saturation region the base-emitter and the base-collector junctions are forward biased.

The transistor is required to be biased from cut-off to saturation and vice-versa when it is being used as a switch. It must be biased in the active region when being used as an amplifier. The transistor functions linearly when its operation is restricted to the active region. For transistor amplifiers, we need to establish an operating point on the characteristics to define a region of operation by fixing the dc current and voltages.

The operating point of a transistor for $I_C = 10$ mA and $V_{CE} = 8$ V is marked as Q in the characteristics shown in Fig. 2.2.

Since, the operating point is a fixed point on the characteristics, it is also referred to as the quiescent point or Q-point. The Q-point can be fixed anywhere in the active region bounded as shown in Fig. 2.2 and as tabulated in Table 2.1.

Table 2.1 Boundaries of the active region

Boundary	*Limiting factor*
Left bound	Saturation region
Top Bound	$I_{C\,\max}$
Bottom bound	Cut-off region
Right bound	$P_{C\,\max}$

$P_{C\,\max}$ is the maximum power dissipation which the device can withstand.

◆ 2.2 DC LOAD LINE

As in the case of a diode, a line called the dc load line can be drawn on the characteristics of the transistor also, which represents the applied load. The intersection of the load line with the characteristics will determine the operating point. Let us now see how to draw the dc load line.

Consider the collector circuit of a biased transistor shown along with its characteristics in Fig. 2.3.

The KVL Equation for the collector circuit is

$$\therefore \qquad V_{CC} = I_C R_C + V_{CE} \tag{2.1}$$

The V_{CE} axis intercept can be found by letting $I_C = 0$ in Equation (2.1).

$\therefore$ $V_{CE} = V_{CC}$ and the intercept is at $(V_{CC}, 0)$. The I_C axis intercept can be found by letting $V_{CE} = 0$ in Equation (2.1).

$$\therefore \qquad I_C = \frac{V_{CC}}{R_C} \text{ and the intercept is at } \left(0, \frac{V_{CC}}{R_C}\right)$$

The load line is plotted by joining these two intercepts as shown in Fig. 2.3(b).

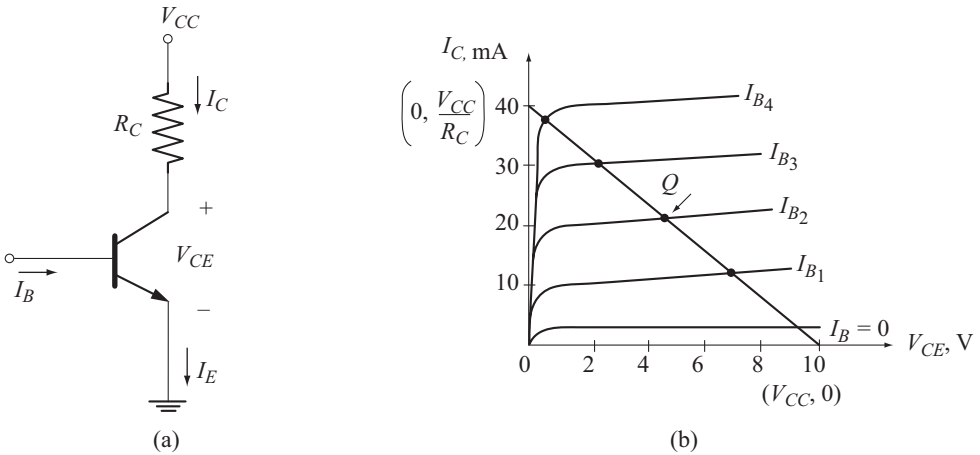


Fig. 2.3 Biased transistor along with its characteristics showing the dc load line

The equation for the dc load line in the slope intercept from can be written from Equation (2.1) as

$$I_C = \left(-\frac{1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C} \tag{2.2}$$

where the slope is $\left(-\frac{1}{R_C}\right)$ while the intercept is $\left(\frac{V_{CC}}{R_C}\right)$. The intersection of this load line with the output characteristics would result in a number of possible operating points. However, the operating point is chosen around the middle of the load line to provide an equal swing of I_C and V_{CE} about the point. This would ensure that the transistor remains in the active region during its entire operation and not stray temporarily into the cut-off or saturation regions. The coordinates of an optimum operating point is therefore $\left(\frac{V_{CC}}{2}, \frac{V_{CC}}{2R_C}\right)$.

◆ 2.3 REASONS FOR INSTABILITY OF THE OPERATING POINT

Having selected and biased the transistor at a desired operating point, the effect of temperature on various device parameters can cause this operating point to drift.

Let us now look at the effects of temperature on transistor parameters. The reasons for instability of the operating point may be listed as

- Variation of leakage current, I_{CO} with temperature
- Variation of current gain, β with temperature and
- Variation of base-emitter voltage, V_{BE} with temperature.

The sensitivity of these parameters to temperature variations can be stated as follows:

- I_{CO}, the reverse saturation current doubles for every 10ºC increase in temperature
- V_{BE} decreases in magnitude by 2.5 mV for every ºC rise in temperature. Generally at room temperature V_{BE} is 0.7 V for silicon transistors and 0.2 V for germanium transistors.
- β increases with rise in temperature.

Any of these factors or all of these factors could cause the operating point to drift from the desired location as fixed by the selected values V_{CE} and I_C in the output characteristics. Typical variations of these parameters at different temperatures for a silicon transistor are shown in Table 2.2.

Table 2.2 Typical variations of I_{CO}, V_{BE} and β with temperature

Temperature	I_{CO}	V_{BE}	β
– 65° C	0.0002 nA	0.85 V	20
25° C	0.1 nA	0.65 V	50
100° C	20 nA	0.48 V	80
175° C	3300 nA	0.3 V	120

We know that the collector current for the common emitter configuration is given by

$$I_C = \beta I_B + (\beta + 1) I_{CO} \tag{2.3}$$

As I_{CO} increases with temperature, I_C also increases resulting in a further increase in temperature which in turn increases β. This further increases I_C and the resulting cumulative effect causes the operating point to drift into the saturation region.

◆ 2.4 STABILITY FACTORS

Transistor circuits must be designed to provide a certain extent of temperature stability so that changes in temperature result in minimal changes in operating point. The maintenance of the operating point at the desired value is specified by stability factors, which represents the extent of change of operating point due to variation in temperature.

A stability factor, can be defined for each of the parameters that affect bias stability as follows:

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} \quad \text{at constant } \beta \text{ and } V_{BE}$$

or

$$S(I_{CO}) = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{\beta,\, V_{BE} \text{ constant}} \tag{2.4}$$

Similarly,

$$S(V_{BE}) = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\, \beta \text{ constant}} \tag{2.5}$$

and

$$S(\beta) = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO},\, V_{BE} \text{ constant}} \tag{2.6}$$

Observe from these equations that, for circuits with low stability factors, change in collector current ΔI_C is small when I_{CO}, V_{BE} and β changes with temperature. Hence circuits with low stability factors are relatively stable and insensitive to variations in temperature.

Total Change in Collector Current

From Equations (2.4) to (2.6) we can write an expression for the total change in the collector current as

$$\Delta I_C = \frac{\partial I_C}{\partial I_{CO}} \Delta I_{CO} + \frac{\partial I_C}{\partial V_{BE}} \Delta V_{BE} + \frac{\partial I_C}{\partial \beta} \Delta\beta \qquad (2.7)$$

or

$$\Delta I_C = S(I_{CO}) \Delta I_{CO} + S(V_{BE}) \Delta V_{BE} + S(\beta) \Delta\beta \qquad (2.8)$$

Lower stability factors therefore imply lower variations in the collector current.

◆ 2.5 FIXED-BIAS CIRCUIT

There are several circuit configurations through which the transistor current and voltage can be adjusted in order to fix the operating point. Fixed-bias, emitter-bias or self-bias and voltage divider bias are some common schemes. In this section, the fixed bias circuit is presented. Figure 2.4 shows a typical fixed-bias circuit.

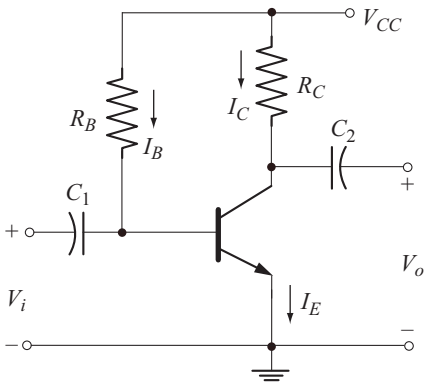


Fig. 2.4 Fixed-bias circuit

The dc equivalent circuit can be written by replacing the capacitors with open circuits (since capacitors block dc) as shown in Fig. 2.5.

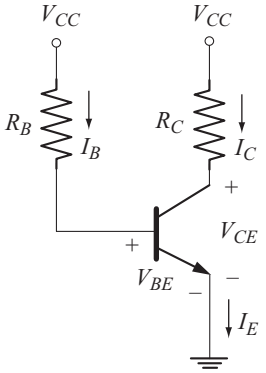


Fig. 2.5 DC equivalent circuit of the fixed-bias circuit

Writing Kirchhoff's voltage law equation to the base-emitter circuit, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

or
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{2.9}$$

Now let us look at the collector-emitter circuit. The magnitudes of the collector current and base current neglecting I_{CO} are related by

$$I_C = \beta I_B \tag{2.10}$$

where β is the dc current gain in common-emitter configuration. Observe from Equation (2.9), that I_B is decided by R_B while I_C is decided by β. Thus, R_C has no role in the value of I_C when the transistor is the active region. However, the value of I_C determines the value of V_{CE}.

Writing Kirchhofffs voltage law equation to the collector-emitter circuit of Fig. 2.5, we get

$$V_{CC} = I_C R_C + V_{CE} \tag{2.11}$$

or
$$V_{CE} = V_{CC} - I_C R_C \tag{2.12}$$

Transistor in Saturation

Figure 2.6 shows the transistor operating in the saturation region.

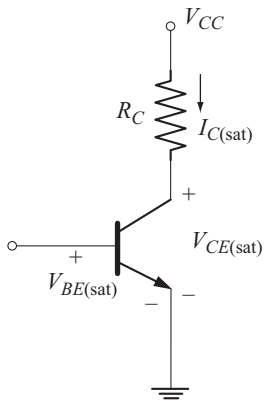


Fig. 2.6 Transistor in saturation

From Equation (2.11), the collector current in saturation, $I_{C\,(sat)}$ is given by

$$I_{C\,(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \tag{2.13}$$

But
$$V_{CE\,(sat)} \approx 0$$

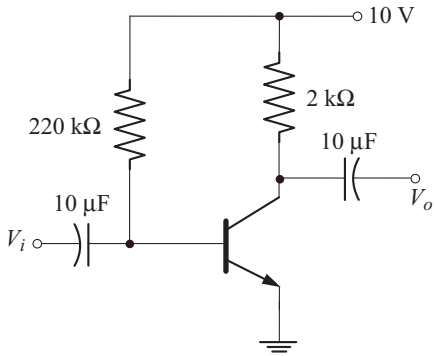
$\therefore$
$$I_{C\,(sat)} \approx \frac{V_{CC}}{R_C} \tag{2.14}$$

Note that in the saturation region I_C is solely decided by R_C.

Example 2.1

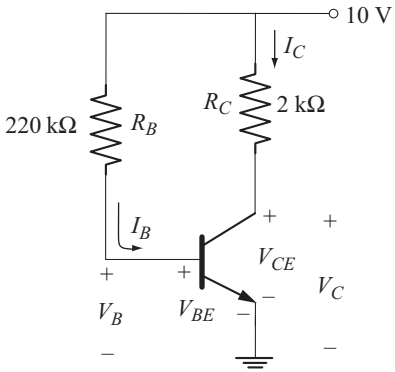
For the fixed-bias circuit shown, assuming $V_{BE} = 0.7$ V and $\beta = 60$ find

(a) Quiescent values of base and collector currents
(b) Quiescent value of V_{CE}
(c) Base-ground and collector-ground voltages
(d) Base-collector voltage
(e) Quiescent values of I_C and V_{CE} for $\beta = 110$



Solution

Treating the coupling capacitors as open circuits, let us mark the various currents and voltages in the circuit.



(a) Quiescent values of base and collector currents

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10\,\text{V} - 0.7\,\text{V}}{220\,\text{kW}} = 42.27\ \mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = 60 \times 42.27\ \mu\text{A} = 2.54\ \text{mA}$$

(b) Quiescent value of V_{CE}

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore \quad V_{CEQ} = V_{CC} - I_{CQ} R_C = 10 - (2.54\ \text{mA})(2\ \text{k}\Omega) = 4.92\ \text{V}$$

(c) Base and collector voltages with respect to ground

$$V_B = V_{BE} = 0.7 \text{ V}$$
$$V_C = V_{CE} = 4.92 \text{ V}$$

(d) Base-collector voltage

$$V_{BC} = V_B - V_C = 0.7 \text{ V} - 4.92 \text{ V} = -4.22 \text{ V}$$

(e) When $\beta = 110$

I_{BQ} is not affected by change in β.

$\therefore$ $I_{BQ} = 42.27\ \mu\text{A}$ [as obtained in part (a)]

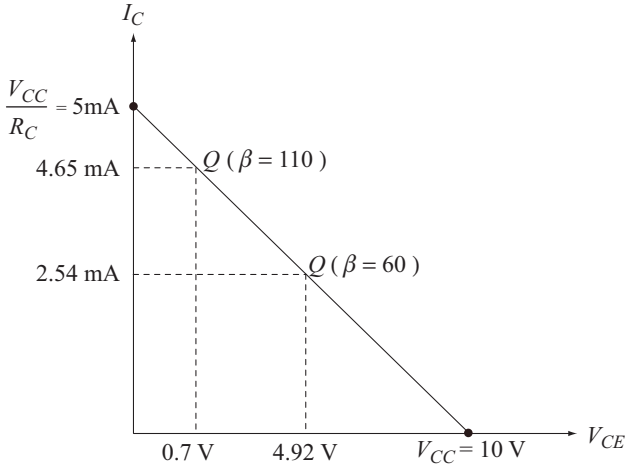
$\therefore$ $I_{CQ} = \beta I_{BQ} = 110 \times 42.27\ \mu\text{A} = 4.65 \text{ mA}$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10 \text{ V} - (4.65 \text{ mA} \times 2 \text{ k}\Omega) = 0.7 \text{ V}$$

Let us now tabulate the Quiescent point for $\beta = 60$ and $\beta = 110$

β	I_{BQ}	I_{CQ}	V_{CEQ}
60	42.27 μA	2.54 mA	4.92 V
110	42.27 μA	4.65 mA	0.7 V

The Q points are indicated on the dc load line in the following figure.



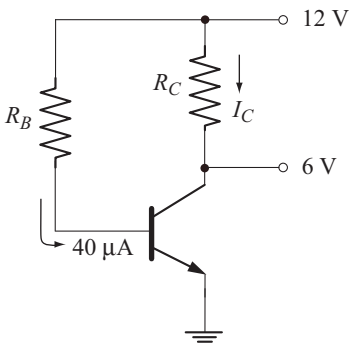
Observe that, when β changes from 60 to 110, the Q point shifts from the middle of the active region to near saturation. Therefore fixed bias circuit has very poor stability of the operating point. The reason for this is that, there is no change in the value of the base current.

Example 2.2

For the fixed-bias circuit shown, determine

(a) Collector current, I_C
(b) Collector resistance, R_C
(c) Base resistance, R_B
(d) V_{CE}

Assume $\beta = 80$ and $V_{BE} = 0.7$ V.



Solution

(a) Collector current

$$I_C = \beta I_B = (80)\,(40\ \mu A) = 3.2\ mA$$

(b) Collector resistance

Given $V_C = 6$ V

$$V_{CE} = V_C = 6\ V$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12\,V - 6\,V}{3.2\,mA} = 1.875\ k\Omega$$

(c) Base resistance

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12\,V - 0.7\,V}{40\ \mu A} = 282.5\ k\Omega$$

(d) V_{CE}

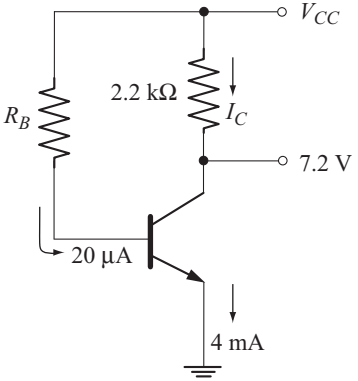
V_{CE} = Voltage from collector to emitter
$= V_C = 6$ V.

Example 2.3

For the circuit shown, find

(a) I_C (b) V_{CC} (c) β (d) R_B

Assume $V_{BE} = 0.7$ V.



Solution

$I_B = 20\ \mu A \quad I_E = 4\ mA \quad V_{CE} = 7.2\ V$

$V_{BE} = 0.7\ V \quad R_C = 2.2\ k\Omega$

We are required to find I_C and V_{CC}.

(a) $I_C + I_B = I_E$

$\therefore \quad I_C = I_E - I_B = 4\ mA - 0.02\ mA = 3.98\ mA$

(b) $V_{CC} = I_C R_C + V_{CE}$

$= (3.98\ mA \times 2.2\ k\Omega) + 7.2\ V$

$= 15.956\ V$

Let $V_{CC} = 16\ V$

(c) $\beta = \dfrac{I_C}{I_B} = \dfrac{3.98\ mA}{0.02\ mA} = 199$

(d) $R_B = \dfrac{V_{CC} - V_{BE}}{I_B} = \dfrac{16\ V - 0.7\ V}{0.02\ mA} = 765\ k\Omega$

Example 2.4

(a) For the fixed-bias circuit, $R_B = 50\ k\Omega$, $R_C = 500\ \Omega$, $V_{CC} = 10\ V$. Find the coordinates of the operating point. Draw the dc load line and locate the operating point on the dc load line. Assume silicon transistor with $\beta = 50$ and $V_{BE} = 0.7\ V$.

(b) Find the new operating point if the transistor is replaced by a similar transistor with $\beta = 100$. Comment on the stability of the circuit.

Solution

(a) $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{10\ V - 0.7\ V}{50\ kW} = 0.186\ mA$

$I_C = \beta I_B = 50 \times 0.186\ mA = 9.3\ mA$

Writing KVL equation for the the collector circuit,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C$$

$$= 10 \text{ V} - (9.3 \text{ mA} \times 0.5 \text{ k}\Omega) = 5.35 \text{ V}$$

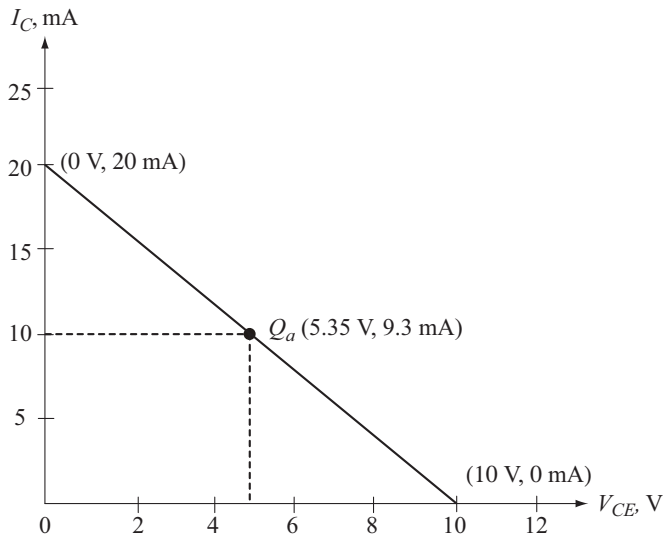
Therefore the operating point is at $(V_{CE}, I_C) = (5.35 \text{ V}, 9.3 \text{ mA})$

Let $$Q_a = (5.35 \text{ V}, 9.3 \text{ mA})$$

The current axis intercept of the load line is

$$\frac{V_{CC}}{R_C} = \frac{10 \text{ V}}{0.5 \text{ kW}} = 20 \text{ mA}$$

and the voltage axis intercept is $V_{CC} = 10$ V. The load line is plotted by joining (0 V, 20 mA) and (10 V, 0 mA) as shown below:



The *Q*-point is nearly at the center of the load line.

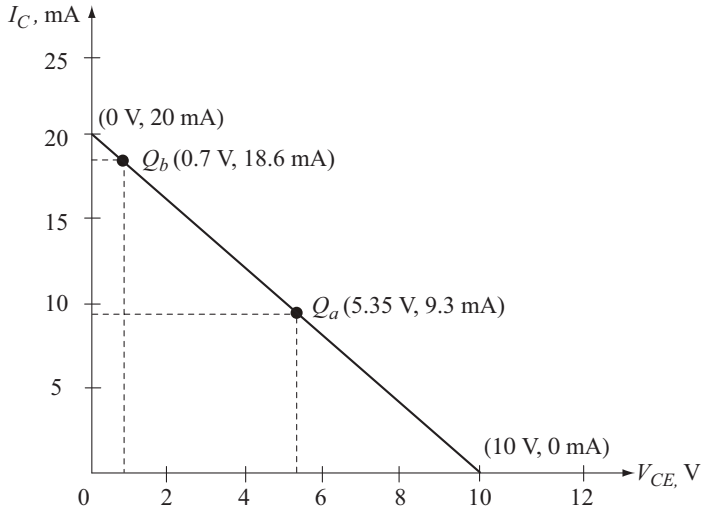
(b) Now, let us locate the new position of the operating point when a transistor with $\beta = 100$ is used.

The base current is obviously not affected and remains at $I_B = 0.186$ mA.

$$I_C = \beta I_B = 100 \times 0.186 \text{ mA} = 18.6 \text{ mA}$$

and $$V_{CE} = V_{CC} - I_C R_C = 10 \text{ V} - (18.6 \text{ mA})\ (0.5 \text{ k}\Omega) = 0.7 \text{ V}$$

The *Q*-point now shifts to $Q_b = (0.7 \text{ V}, 18.6 \text{ mA})$.



The *Q*-point has moved into the saturation region. In general, fixed-bias circuits do not provide stability against variation in β.

◆ 2.6 LOAD LINE ANALYSIS OF THE FIXED-BIAS CIRCUIT

We know that the load line is constructed on the output characteristics joining (0, V_{CC}/ R_C) and (V_{CC}, 0). The effect of variation in I_B on the *Q*-point is shown in Fig 2.7.

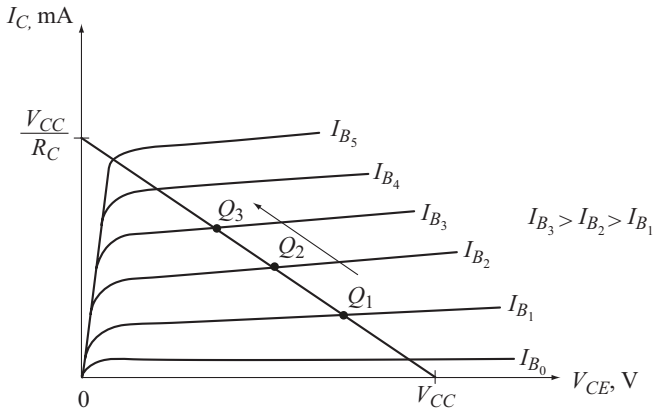


Fig. 2.7 Effect of variation in base current on Q-point

If the value of I_B is increased by decreasing the value of base resistance R_B, the *Q*-point moves up the load line gradually towards saturation.

Now, if V_{CC} is kept constant and if collector resistance R_C is increased, keeping base current I_B fixed, the *Q*-point moves to the left into saturation as shown in Fig. 2.8.

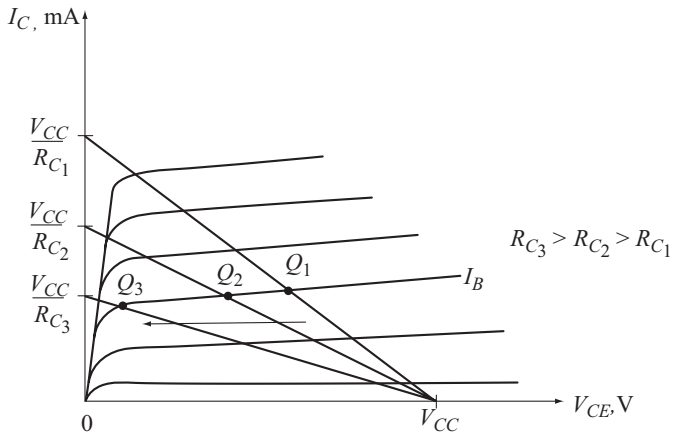


Fig. 2.8 Effect of variation in collector resistance on Q-point

If we now keep R_C fixed while decreasing V_{CC}, the Q-point once again moves towards the left into saturation as shown in Fig. 2.9.

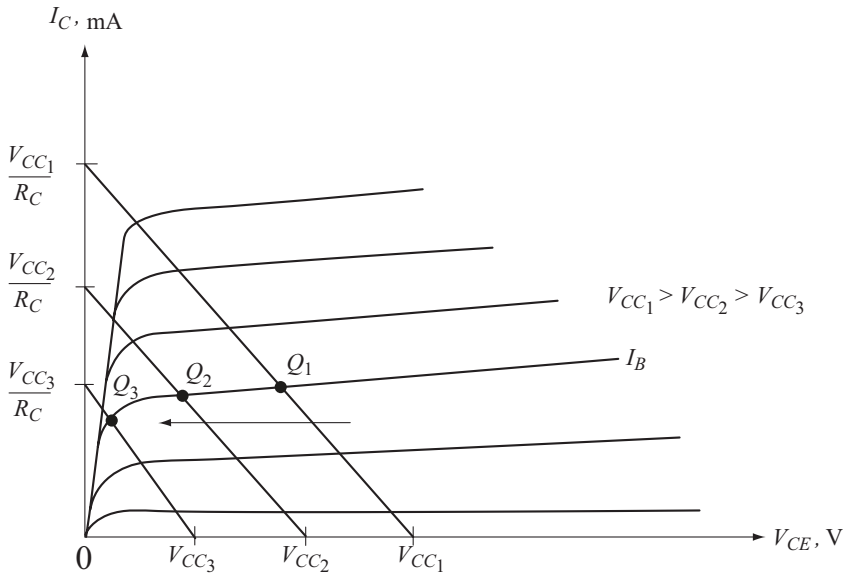


Fig. 2.9 Effect of Variation in V_{CC} on Q-point

◆ 2.7 EMITTER-BIAS CIRCUIT

The addition of an emitter resistance improves the stability of the fixed-bias circuit. Such a configuration known as an emitter-bias or self-bias circuit is shown in Fig. 2.10.

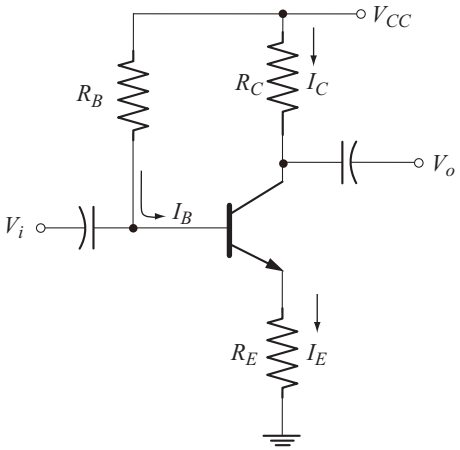


Fig. 2.10 Emitter-bias circuit

Let us proceed with the analysis of this circuit.

Base-emitter Circuit

The base-emitter dc circuit is shown in Fig. 2.11.

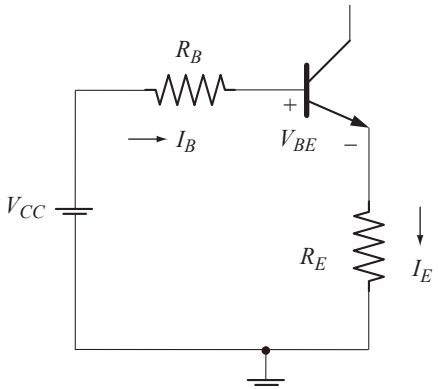


Fig. 2.11 Base-emitter dc circuit of emitter-bias circuit

Applying Kirchoff's voltage law to the base-emitter circuit, we have

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \tag{2.15}$$

$$I_E = I_C + I_B$$

Using $I_C = \beta I_B$ we have

$$I_E = \beta I_B + I_B$$

$$I_E = (\beta + 1) I_B \tag{2.16}$$

Substituting for I_E in Equation (2.15),

$$V_{CC} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E$$

$$\therefore \quad V_{CC} - V_{BE} = I_B [R_B + (\beta + 1) R_E]$$

or

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \tag{2.17}$$

Stability of the Q-point

Now, let us examine how this circuit stabilizes the operating point. Let us assume for reasons such as increase in temperature, the collector current, I_C increases. This results in an increase in the emitter current, I_E. From Equation (2.15)

$$V_{CC} - V_{BE} = I_B R_B - I_E R_E \tag{2.18}$$

The left hand side of Equation (2.18) is a constant. An increase in I_E increases $I_E R_E$ and to maintain constant ($V_{CC} - V_{BE}$), the term $I_B R_B$ must decrease; R_B being constant, I_B reduces. This in turn reduces I_C ($I_C = \beta I_B$), there by stabilizing I_C.

With $R_E = 0$, Equation (2.17) reduces to Equation (2.9) as expected. From Equation (2.17) it is clear that the equivalent resistance at the base is

$$R_{B\text{eq}} = R_B + (\beta + 1) R_E \tag{2.19}$$

Thus, the resistance R_E in the emitter circuit gets reflected as $(\beta + 1) R_E$ in the base circuit. Resistance R_E provides a negative feedback to the circuit which minimizes drift in the operating point in comparison with the fixed-bias circuit.

Collector-emitter Circuit

The collector-emitter dc circuit is shown in Fig. 2.12.

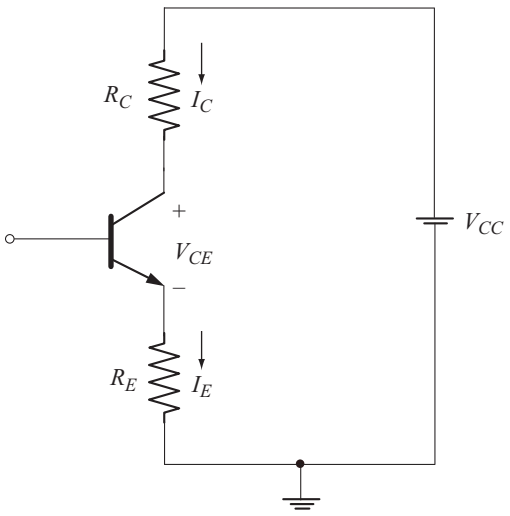


Fig. 2.12 Collector-emitter dc circuit of emitter-bias circuit

Applying Kirchoff's voltage law, we have,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \tag{2.20}$$

Substituting $I_E \simeq I_C$,

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \tag{2.21}$$

Let us now get the nomenclature clear:

Let V_C = Voltage from collector to ground
V_B = Voltage from base to ground and
V_E = Voltage from emitter to ground
$\therefore$ V_E = Voltage across R_E

$$V_E = I_E R_E \tag{2.22}$$

V_C = Collector-emitter voltage + Voltage from emitter to ground

$$V_C = V_{CE} + V_E \tag{2.23}$$
$$= V_{CE} + I_E R_E$$

Substituting for $(V_{CE} + I_E R_E)$ from Equation (2.20)

$$V_C = V_{CC} - I_C R_C \tag{2.24}$$

V_B = Base-emitter voltage + voltage from emitter to ground

$$V_B = V_{BE} + V_E \tag{2.25}$$
$$= V_{BE} + I_E R_E \tag{2.26}$$

Substituting for $(V_{BE} + I_E R_E)$ from Equation (2.15)

$$V_B = V_{CC} - I_B R_B \tag{2.27}$$

Saturation Level

When the transistor is in saturation

$$V_{CE} = V_{CE\,(sat)} \approx 0 \text{ V}$$

and

$$I_C = I_{C\,(sat)}$$

Substituting this condition in Equation (2.20) and taking $I_E \approx I_C$ we have

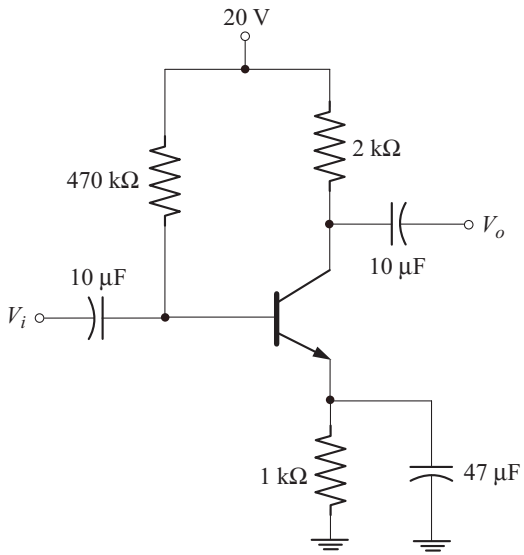
$$V_{CC} = I_{C\,(sat)} [R_C + R_E]$$

$$I_{C\,(sat)} = \frac{V_{CC}}{R_C + R_E} \tag{2.28}$$

Example 2.5

For the emitter-bias circuit shown using silicon transistor with $V_{BE} = 0.7$ V and $\beta = 60$, find,

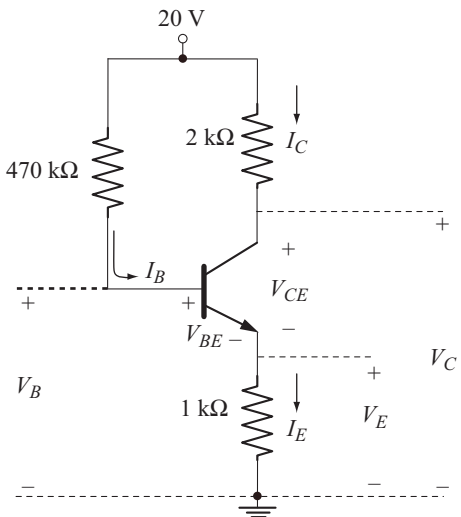
(a) Base current and collector current
(b) V_{CE}
(c) Collector, emitter and base voltages to ground
(d) V_{BC}
(e) Estimate I_C and V_{CE} for $\beta = 110$.



Solution

(a) Base current and collector current

For dc analysis we can treat capacitors as open circuit



From Equation (2.17)

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ kW} + (61 \times 1\text{ kW})} = 36.34\ \mu\text{A}$$

$$I_C = \beta I_B = 60 \times 36.34\ \mu\text{A} = 2.18\text{ mA}$$

(b) V_{CE}

From Equation (2.21)

$$\begin{aligned} V_{CE} &= V_{CC} - I_C (R_C + R_E) \\ &= 20\text{ V} - 2.18\text{ mA}\ [2\text{ k}\Omega + 1\text{ k}\Omega] \\ &= 13.46\text{ V} \end{aligned}$$

(c) Collector, emitter and base voltages to ground

From Equation (2.24)

$$V_C = V_{CC} - I_C R_C = 20\text{ V} - (2.18\text{ mA} \times 2\text{ k}\Omega) = 15.64\text{ V}$$

From Equation (2.23)

$$V_E = V_C - V_{CE} = 15.64\text{ V} - 13.46\text{ V} = 2.18\text{ V}$$

From Equation (2.25)

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2.18\text{ V} = 2.88\text{ V}$$

(d) V_{BC}

$$\begin{aligned} V_{BC} &= \text{Voltage from base to collector} \\ &= \text{Voltage from base to ground} - \text{Voltage from collector to ground} \\ &= V_B - V_C = 2.88\text{ V} - 15.64\text{ V} = -12.76\text{ V} \end{aligned}$$

V_{BC} is negative as expected.

(e)
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ kW} + [110+1]1\text{ kW}} = 33.22\ \mu\text{A}$$

$$I_C = \beta I_B = 110 \times 33.22\ \mu\text{A} = 3.65\text{ mA}$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_C (R_C + R_E) \\ &= 20\text{ V} - 3.65\text{ mA}\ [2\text{ k}\Omega + 1\text{ k}\Omega] \\ &= 9.05\text{ V} \end{aligned}$$

Let us now tabulate the quiescent currents and voltage for $\beta = 60$ and $\beta = 110$.

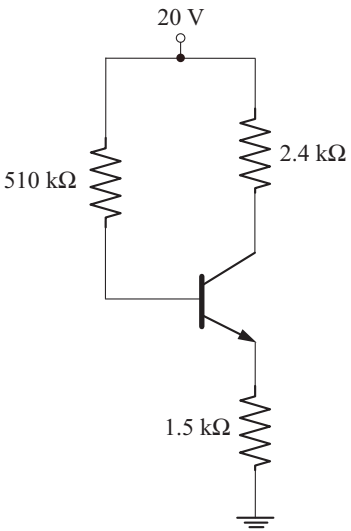
β	I_{BQ}	I_{CQ}	V_{CEQ}
60	36.34 μA	2.18 mA	13.46 V
110	33.22 μA	3.65 mA	9.05 V

Observe that the effect of the negative feedback through the inclusion of the emitter resistance has been to reduce the base current inspite of β being nearly doubled. The operating point remains very much in the active region. Compare this with the results obtained in Example 2.1(e).

Example 2.6

For the emitter-bias circuit shown using silicon transistor with $V_{BE} = 0.7$ V and $\beta = 100$, find

(a) Quiescent values of base current, collector current and collector to emitter voltage.
(b) Voltage at collector, base and emitter with respect to ground.



Solution

(a) I_B, I_C and V_{CE}

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$= \frac{20\text{ V} - 0.7\text{ V}}{510\text{ kW} + (101)(1.5\text{ kW})} = 29.18\ \mu\text{A}$$

$$I_C = \beta I_B = (100)\ (29.18\ \mu\text{A}) = 2.92\text{ mA}$$

$$V_{CE} = V_{CC} - I_C\,[R_C + R_E]$$

$$= 20\text{ V} - (2.92\text{ mA})\ (2.4\text{ k}\Omega + 1.5\text{ k}\Omega) = 8.61\text{ V}$$

$$V_C = V_{CC} - I_C R_C = 20\text{ V} - (2.92\text{ mA})\ (2.4\text{ k}\Omega) = 13\text{ V}$$

$$V_E = I_E R_E = [I_B + I_C]\ R_E$$

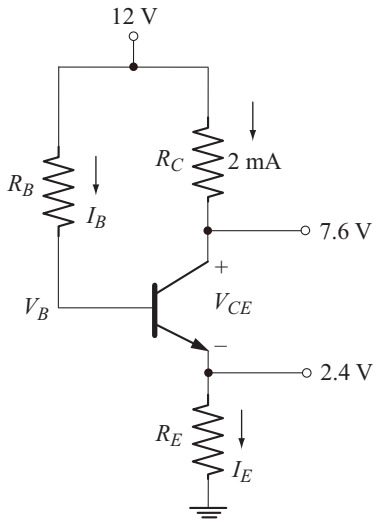
$$= [29.18\ \mu\text{A} + 2.92\text{ mA}]\ [1.5\text{ k}\Omega] = 4.42\text{ V}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 4.42\text{ V} = 5.12\text{ V}$$

Example 2.7

For the circuit shown, using silicon transistor with $V_{BE} = 0.7$ V and $\beta = 80$ find

(a) All resistance values (b) V_{CE} and V_B



Solution

Given $V_C = 7.6$ V, $V_E = 2.4$ V, $I_C = 2$ mA

(a) Circuit resistances

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{12 \text{ V} - 7.6 \text{ V}}{2 \text{ mA}} = 2.2 \text{ k}\Omega$$

Since, the emitter and the collector currents are approximately equal,

$$I_E \simeq I_C = 2 \text{ mA}$$

$$\therefore \quad R_E = \frac{V_E}{I_E} = \frac{2.4 \text{ V}}{2 \text{ mA}} = 1.2 \text{ k}\Omega$$

$$I_C = \beta I_B$$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{80} = 0.025 \text{ mA}$$

Writing KVL equation to the base-emitter circuit,

$$V_{CC} = I_B R_B + V_{BE} + V_E$$

$$\therefore \quad I_B R_B = V_{CC} - V_{BE} - V_E = 12 \text{ V} - 0.7 \text{ V} - 2.4 \text{ V} = 8.9 \text{ V}$$

$$\therefore \quad R_B = \frac{8.9 \text{ V}}{I_B} = \frac{8.9 \text{ V}}{0.025 \text{ mA}} = 356 \text{ k}\Omega$$

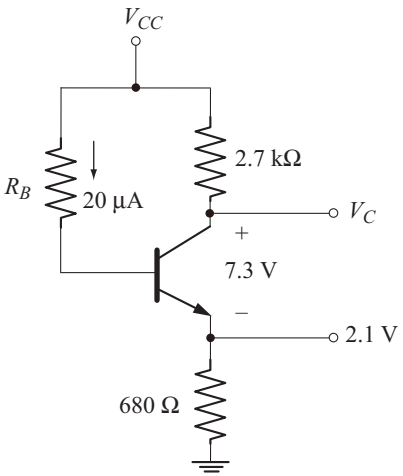
(b) $V_{CE} = V_C - V_E = 7.6\text{ V} - 2.4\text{ V} = 5.2\text{ V}$

and $V_B = V_{BE} + V_E = 0.7\text{ V} + 2.4\text{ V} = 3.1\text{ V}$

Example 2.8

The circuit shown below uses silicon transistor with $V_{BE} = 0.7$ V. Calculate

(a) β (b) V_{CC} (c) R_B (d) V_C (e) $I_{C\,(sat)}$



Solution

(a) β

Given the voltage across the emitter resistance, we can obtain the emitter current as

$$I_E = \frac{V_E}{R_E} = \frac{2.1\text{ V}}{680\text{ W}} = 3.09\text{ mA}$$

The emitter current is approximately equal to collector current.

$$\therefore \quad I_C = 3.09\text{ mA}$$

Now $$\beta = \frac{I_C}{I_B} = \frac{3.09\text{ mA}}{20\ \mu\text{A}} = 154.5$$

(b) V_{CC}

From the KVL equation for the collector emitter circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + V_E$$
$$= (3.09\text{ mA} \times 2.7\text{ k}\Omega) + 7.3\text{ V} + 2.1\text{ V} = 17.74\text{ V}$$

(c) R_B

Writing the KVL equation for the base-emitter circuit

$$V_{CC} = I_B R_B + V_{BE} + V_E$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE} - V_E}{I_B}$$

$$= \frac{17.74\ \text{V} - 0.7\ \text{V} - 2.1\ \text{V}}{20\ \mu\text{A}} = 747\ \text{k}\Omega$$

(d) V_C

$$V_C = V_{CE} + V_E = 7.3\ \text{V} + 2.1\ \text{V} = 9.4\ \text{V}$$

(e) $I_{C\,(\text{sat})}$

$$I_{C\,(\text{sat})} = \frac{V_{CC}}{R_C + R_E} = \frac{17.74\ \text{V}}{2.7\ \text{kW} + 680\ \text{W}} = 5.248\ \text{mA}$$

◆ 2.8 VOLTAGE DIVIDER BIAS OR UNIVERSAL BIAS CIRCUIT

In both the fixed-bias and the emitter-bias circuits, the quiescent values of I_C and V_{CE}, i.e., the quiescent point is a function of dc current gain β of the transistor. We know that this current gain β is sensitive to temperature and its value keeps varying. A biasing circuit independent or less dependant on β such as the voltage-divider bias circuit is therefore desirable. A voltage divider bias circuit is shown in Fig. 2.13.

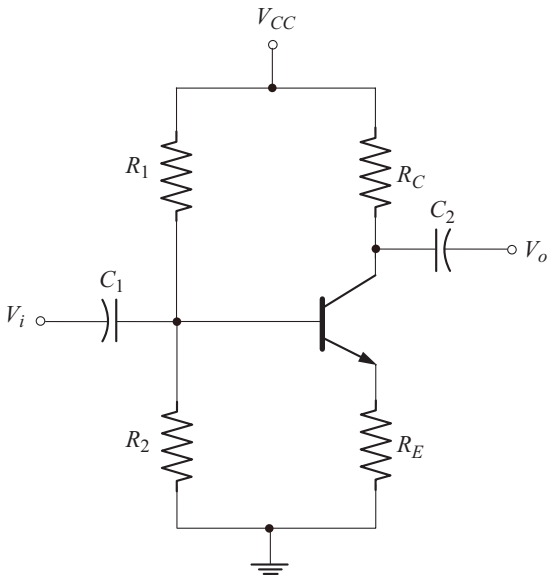


Fig. 2.13 Voltage divider bias or universal bias circuit

The voltage divider bias circuit can be analysed in two methods. First one is the exact method and the second one is the approximate method. Let us analyse the circuit using each of these methods.

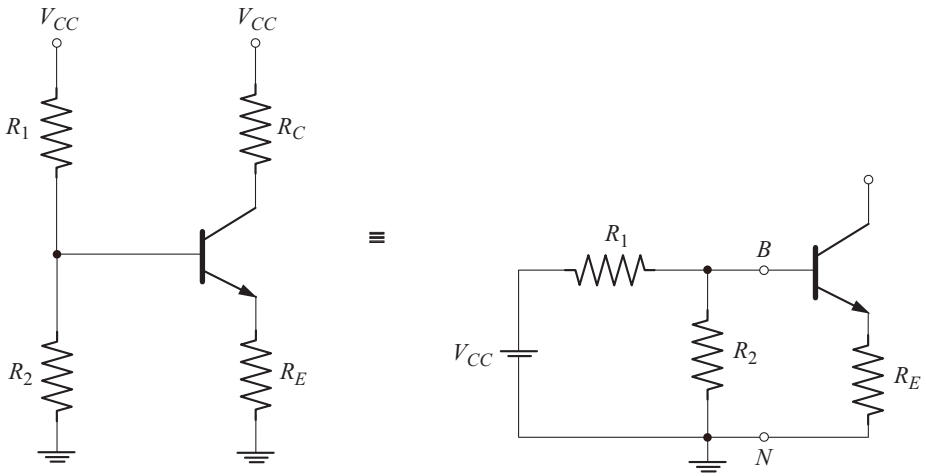


Fig. 2.14 Base circuit of voltage divider bias circuit

2.8.1 Exact Analysis

The input side of the circuit of Fig. 2.13 is redrawn in Fig. 2.14 for the dc analysis.

The Thevenin equivalent of the circuit comprising of V_{CC}, R_1 and R_2 of Fig. 2.14 is drawn in Fig. 2.15(a).

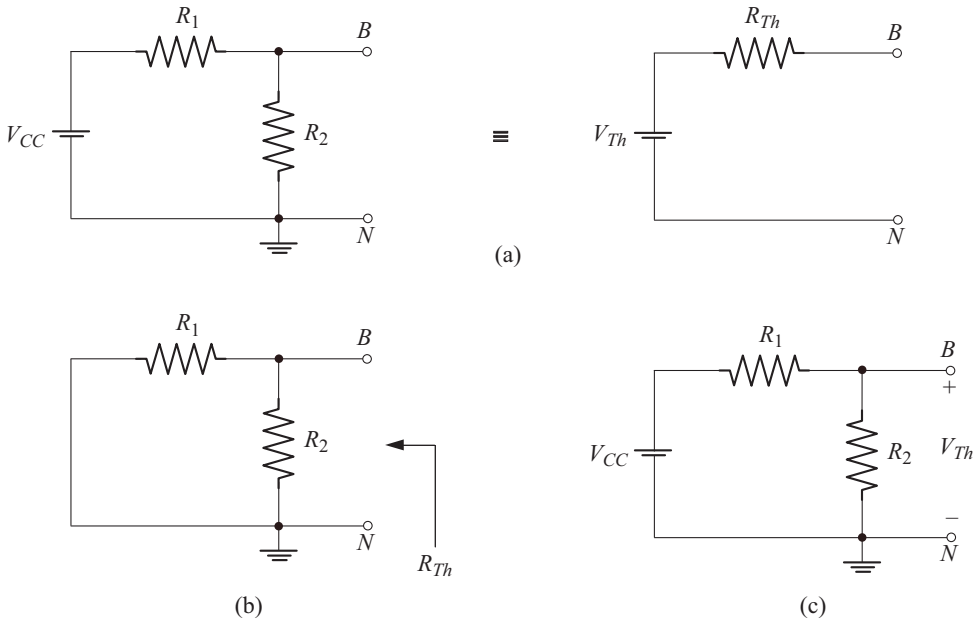


Fig. 2.15 (a) Thevenin equivalent
(b) Determination of R_{Th}
(c) Determination of V_{Th}

The Thevenin equivalent of the circuit to the left of *B* and *N* in Fig. 2.14 can be written by computing the Thevenin resistance and Thevenin voltage as seen between *B* and *N*.

To find the Thevenin resistance R_{Th}, V_{CC} is reduced to zero in the circuit of Fig. 2.15(a). The resulting circuit is shown in Fig. 2.15(b).

From Fig. 2.15(b), Thevenin resistance is

$$R_{Th} = R_1 \parallel R_2$$

or

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

and from Fig. 2.15(c), Thevenin voltage is

$$V_{Th} = V_{CC} \frac{R_2}{R_1 + R_2}$$

The circuit of Fig. 2.14 is redrawn in Fig. 2.16 after substituting the Thevenin equivalent between *B* and *N*.

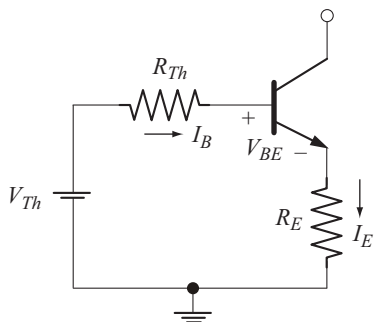


Fig. 2.16 Base circuit with Thevenin equivalent

Applying Kirchhoff's voltage law to the base-emitter circuit in Fig. 2.16, we get

$$V_{Th} = R_{Th} I_B + V_{BE} + I_E R_E \tag{2.29}$$

Now

$$I_C + I_B = I_E \tag{2.30}$$

and

$$I_C = \beta I_B$$

Substituting in Equation (2.30)

$$\beta I_B + I_B = I_E$$

or

$$I_E = (\beta + 1) I_B \tag{2.31}$$

Equation (2.29) now becomes

$$V_{Th} = R_{Th} I_B + V_{BE} + (\beta + 1) I_B R_E$$

$$V_{Th} - V_{BE} = [R_{Th} + (\beta + 1) R_E] I_B$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{Th} + (\beta + 1) R_E} \tag{2.32}$$

The collector circuit of Fig. 2.13 is shown in Fig 2.17.

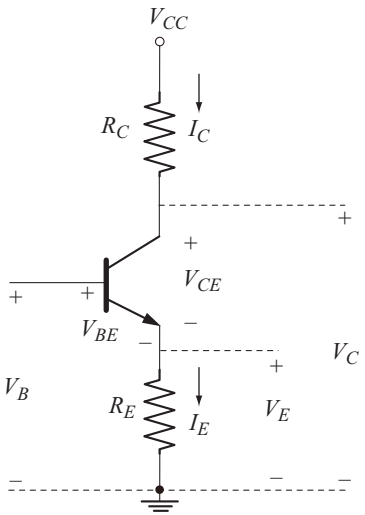


Fig. 2.17 Collector circuit of voltage divider bias

Applying KVL to the collector circuit of Fig. 2.17,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \tag{2.33}$$

Using
$$I_C \simeq I_E \tag{2.34}$$

Equation (2.33) thus become

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{2.35}$$

Further from Fig. 2.17,

V_E = Voltage across R_E

$$V_E = I_E R_E \tag{2.36}$$

V_C = Collector to ground voltage

$$V_C = V_{CE} + V_E \tag{2.37}$$

V_B = Base to ground voltage

$$V_B = V_{BE} + V_E \tag{2.38}$$

In this circuit also negative feedback is provided through the emitter resistance. As a result I_C and V_{CE} become almost independent of β. For this reason voltage divider bias is also called as beta independent circuit.

Transistor Saturation

When the transisitor is in saturation

$$V_{CE} = V_{CE(\text{sat})} \approx 0 \text{ V}$$

and
$$I_C = I_{C(\text{sat})}$$

Substuiting this condition in Equation (2.33) and taking $I_E \approx I_C$, we get

$$V_{CC} = I_{C(\text{sat})} [R_C + R_E]$$

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E} \tag{2.39}$$

Note that Equation (2.39) is same as that obtained for emitter bias circuit in Equation (2.28).

2.8.2 Approximate Analysis

We know that, the resistance R_E in the emitter circuit gets reflected as $(1+\beta)\, R_E$ in the base circuit. Therefore the circuit between base and ground of Fig. 2.14 can be replaced by an equivalent resistance. $R_i = (1+\beta)\, R_E$ as shown in Fig. 2.18.

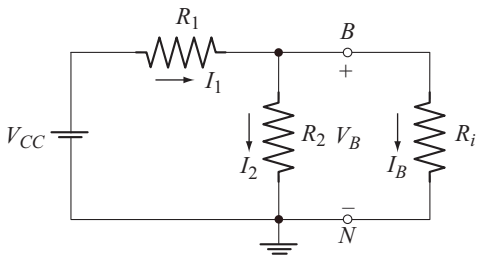


Fig. 2.18 Input circuit for approximate analysis

For the circuit of Fig. 2.18 using KCL we can write

$$I_1 = I_2 + I_B \tag{2.40}$$

$$R_i = (1+\beta)\, R_E \approx \beta\, R_E, \quad \text{since } \beta \gg 1$$

$$I_B = \frac{V_B}{R_i} \quad \text{and} \quad I_2 = \frac{V_B}{R_2}$$

if $$R_i = \beta\, R_E \geq 10\, R_2 \tag{2.41}$$

then $I_B \leq 0.1\, I_2$, hence I_B can be neglected in Equation (2.40). As a result we get

$$I_1 \approx I_2$$

Applying KVL to the circuit of Fig. 2.18 we get

$$V_{CC} = I_1 R_1 + I_2 R_2 = I_2 [R_1 + R_2]$$

$\therefore$ $$I_2 = \frac{V_{CC}}{R_1 + R_2}$$

Now $$V_B = I_2 R_2$$

or $$V_B = \frac{V_{CC} R_2}{R_1 + R_2} \tag{2.42}$$

Observe that expression for V_B is identical to that of V_{Th}

But $$V_B = V_E + V_{BE}$$

$\therefore$ $$V_E = V_B - V_{BE} \tag{2.43}$$

The emitter current I_E is given by

$$I_E = \frac{V_E}{R_E} \tag{2.44}$$

and $$I_C \approx I_E \tag{2.45}$$

From the KVL equation of collector - emitter circuit

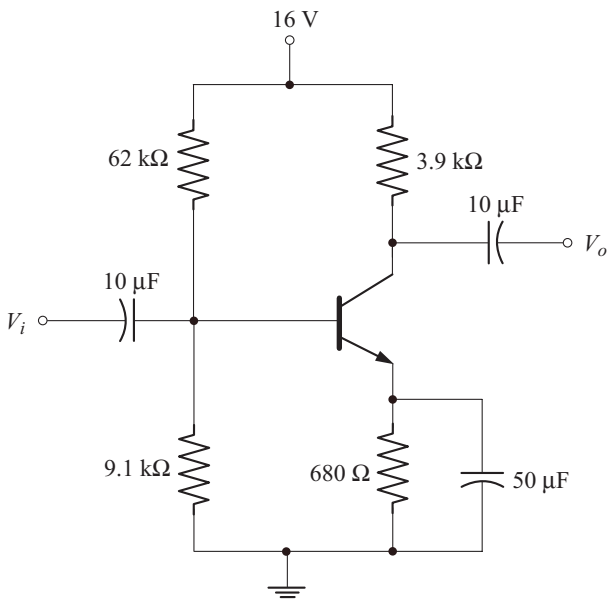
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Using $$I_C \approx I_E$$

$$V_{CE} = V_{CC} - I_C [R_C + R_E] \tag{2.46}$$

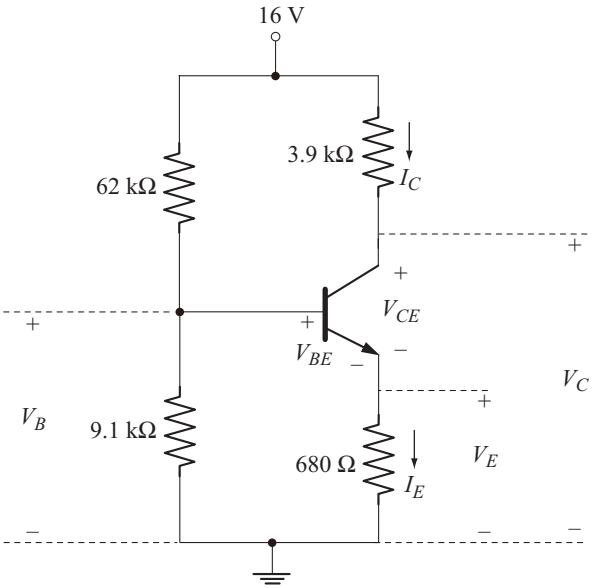
Example 2.9

(a) Find the quiescent base current, collector current and V_{CE} for the circuit shown using silicon transistor with $V_{BE} = 0.7$ V and $\beta = 80$.
(b) Determine the values of collector, emitter and base voltages with respect to ground.
(c) Repeat (a) for $\beta = 150$.
(d) Draw the dc load line and locate the Q points corresponding to $\beta = 80$ and $\beta = 150$.



Solution

Let us draw the dc circuit with all voltages and currents marked.



(a)
$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{62\ \text{kW}' \ 9.1\ \text{kW}}{62\ \text{kW} + 9.1\ \text{kW}} = 7.94\ \text{k}\Omega$$
$$V_{Th} = V_{CC}\,\frac{R_2}{R_1 + R_2} = 16\ \text{V} \times \frac{9.1\ \text{kW}}{62\ \text{kW} + 9.1\ \text{kW}} = 2.05\ \text{V}$$

The base current can now be obtained from

$$I_{BQ} = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$
$$= \frac{2.05\ \text{V} - 0.7\ \text{V}}{7.94\ \text{kW} + (80 + 1)0.68\ \text{kW}} = 21.42\ \mu\text{A}$$
$$I_{CQ} = \beta I_B = 80 \times 21.42\ \mu\text{A} = 1.71\ \text{mA}$$
$$V_{CEQ} = V_{CC} - I_C\,(R_C + R_E)$$
$$= 16\ \text{V} - 1.71\ \text{mA}\ [3.9\ \text{k}\Omega + 0.68\ \text{k}\Omega] = 8.17\ \text{V}$$

(b) Collector to ground voltage is

$$V_C = V_{CC} - I_C R_C = 16\ \text{V} - (1.71\ \text{mA} \times 3.9\ \text{k}\Omega) = 9.33\ \text{V}$$

Emitter to ground voltage is

$$V_E = I_E R_E \simeq I_C R_E = 1.71\ \text{mA} \times 0.68\ \text{k}\Omega = 1.16\ \text{V}$$

and the base to ground voltage is

$$V_B = V_{BE} + V_E = 0.7\ \text{V} + 1.16\ \text{V} = 1.86\ \text{V}$$

(c) Now for $\beta = 150$

$$I_{BQ} = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2.05\text{ V} - 0.7\text{ V}}{7.94\text{ kW} + (150 + 1)0.68\text{ kW}} = 12.2\ \mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = 150 \times 12.2\ \mu\text{A} = 1.83\text{ mA}$$

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

$$= 16\text{ V} - 1.83\text{ mA}\ (3.9\ \text{k}\Omega + 0.68\ \text{k}\Omega) = 7.62\text{ V}$$

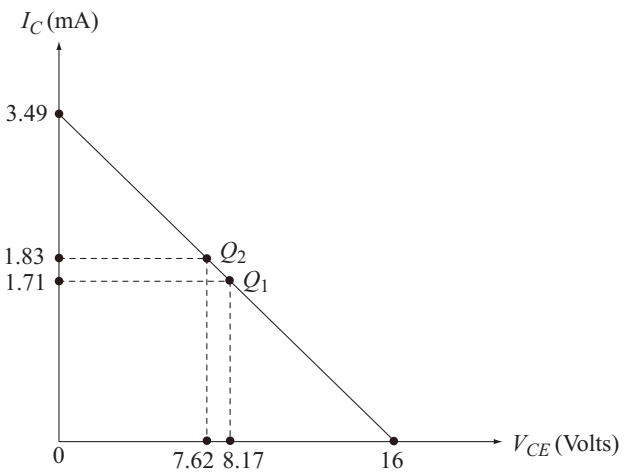
Let us now tabulate the quiescent currents and voltage for $\beta = 80$ and $\beta = 150$.

β	I_{BQ}	I_{CQ}	V_{CEQ}
80	21.42 μA	1.71 mA	8.17 V
150	12.2 μA	1.83 mA	7.62 V

Observe that even on nearly doubling current gain β, I_{BQ} reduces by almost half while I_{CQ} and V_{CEQ} marginally change indicating good stability of the operating point. Compare this with the results obtained in Examples 2.1 and 2.6. In the case of the voltage divider bias circuit, the base current drastically reduces to keep the increase in collector current, due to increase in β at a minimum.

(d) DC load line

$$I_{C\,(\text{sat})} = \frac{V_{CC}}{R_C + R_E} = \frac{16\text{ V}}{3.9\text{ kW} + 0.68\text{ kW}} = 3.49\text{ mA}$$

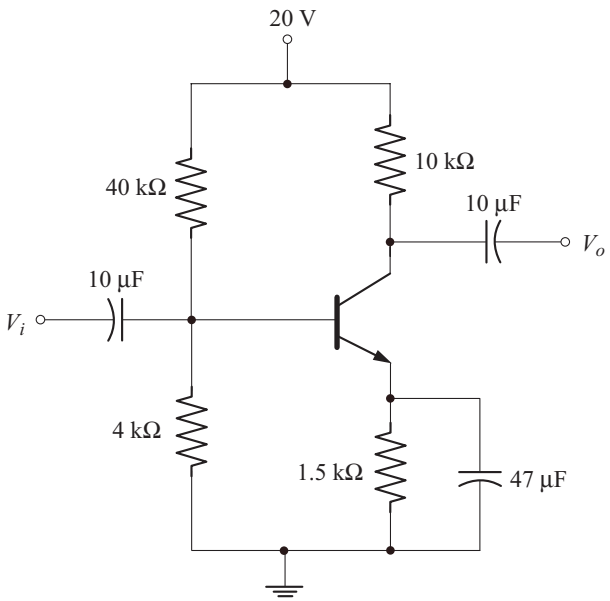


Example 2.10

For the voltage divider bias configuration shown below.

(a) Find I_C and V_{CE} using exact analysis.
(b) Find I_C and V_{CE} using approximate analysis.
(c) Find $I_{C\,(sat)}$.
(d) Compare the results obtained (a) and (b) and comment.

Assume silicon transistor with $\beta = 150$.



Solution

(a) ***Exact Analysis***

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(40\,\text{kW})(4\,\text{kW})}{40\,\text{kW} + 4\,\text{kW}} = 3.63\ \text{k}\Omega$$

$$V_{Th} = \frac{V_{CC}\ R_2}{R_1 + R_2} = \frac{(20\ \text{V})\ (4\ \text{kW})}{40\ \text{kW} + 4\ \text{kW}} = 1.82\ \text{V}$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_E}$$

$$= \frac{1.82\ \text{V} - 0.7\,\text{V}}{3.63\ \text{kW} + (151)(1.5\ \text{kW})} = 4.86\ \mu\text{A}$$

$$I_C = \beta I_B = (150)\ (4.86\ \mu\text{A}) = 0.729\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C\,[R_C + R_E]$$

$$= 20\ \text{V} - 0.729\ \text{mA}\,[10\ \text{k}\Omega + 1.5\ \text{k}\Omega] = 11.62\ \text{V}$$

(b) ***Approximate Analysis***

$$\beta R_E = (150)\,(1.5\ \text{k}\Omega) = 225\ \text{k}\Omega$$
$$10\,R_2 = (10)\,(4\ \text{k}\Omega) = 40\ \text{k}\Omega$$

Note that $\beta R_E > 10\,R_2$
Hence we can use approximate analysis

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = 1.82\ \text{V} \quad (\text{same as } V_{Th})$$
$$V_E = V_B - V_{BE} = 1.82\ \text{V} - 0.7\ \text{V} = 1.12\ \text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{1.12\ \text{V}}{1.5\ \text{kW}} = 0.746\ \text{mA}$$
$$I_C \approx I_E = 0.746\ \text{mA}$$
$$V_{CE} = V_{CC} - I_C\,[R_C + R_E]$$
$$= 20\ \text{V} - 0.746\ \text{mA}\,[10\ \text{k}\Omega + 1.5\ \text{k}\Omega] = 11.42\ \text{V}$$

(c) $$I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E} = \frac{20\ \text{V}}{10\ \text{kW} + 1.5\ \text{kW}} = 1.74\ \text{mA}$$

(d) The results of exact and approximate analysis are compared in the following table

Parameter	*Exact analysis*	*Approximate analysis*
I_C	0.729 mA	0.746 mA
V_{CE}	11.62 V	11.42 V

Observe that there is only a slight difference in the values since the condition $\beta R_E \geq 10\,R_E$ is satisfied.

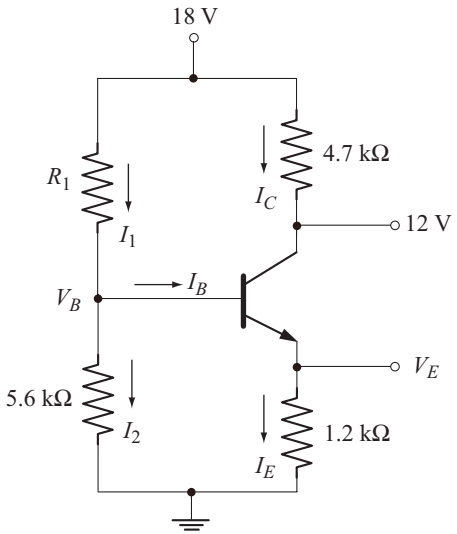
Example 2.11

For the circuit shown in the figure below using silicon transistor with $V_{BE} = 0.7$ V. Find

(a) Collector current

(b) Emitter and base voltages with respect to ground

(c) Value of resistance R_1.



Solution

(a) $$V_{CC} = I_C R_C + V_C$$

$$\therefore \quad I_C = \frac{V_{CC} - V_C}{R_C} = \frac{18\text{ V} - 12\text{ V}}{4.7\text{ kW}} = 1.27\text{ mA}$$

(b) $$V_E = I_E R_E \approx I_C R_E = (1.27\text{ mA})\,(1.2\text{ k}\Omega) = 1.52\text{ V}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 1.52\text{ V} = 2.22\text{ V}$$

(c) $$V_{CC} = I_1 R_1 + I_2 R_2 \qquad \text{(A)}$$

KCL at node V_B yields $$I_1 = I_B + I_2$$

Neglecting I_B, we get $$I_1 \approx I_2$$

Now from Equation (A) we have

$$R_1 + R_2 = \frac{V_{CC}}{I_2} \qquad \text{(B)}$$

But $V_B = I_2 R_2$

$$\therefore \quad I_2 = \frac{V_B}{R_2} = \frac{2.22\text{ V}}{5.6\text{ kW}} = 0.39\text{ mA}$$

From Equation (B) we have

$$R_1 + R_2 = \frac{18\text{ V}}{0.39\text{ mA}} = 46.15\text{ k}\Omega$$

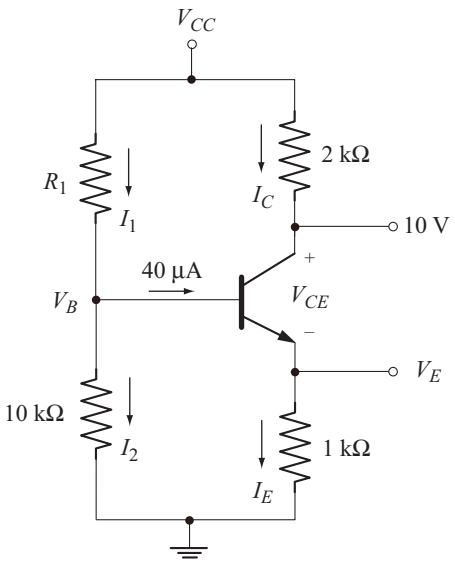
$$R_1 = 46.15\text{ k}\Omega - R_2 = 46.15\text{ k}\Omega - 5.6\text{ k}\Omega = 40.55\text{ k}\Omega$$

Example 2.12

For the voltage divider bias configuration shown below determine

(a) I_C and V_E
(b) V_{CC} and V_{CE}
(c) V_B and R_1

Assume silicon transistor with $\beta = 80$.



Solution

(a) I_C and V_{CE}

$$I_C = \beta I_B = (80)\,(40\ \mu A) = 3.2\ mA$$
$$I_E = I_B + I_C = 40\ \mu A + 3.2\ mA = 3.24\ mA$$
$$V_E = I_E R_E = (3.24\ mA)\,(1\ k\Omega) = 3.24\ V$$

(b) V_{CC} and V_{CE}

$$V_{CC} = I_C R_C + V_C = (3.2\ mA)\,(2\ k\Omega) + 10\ V = 16.4\ V$$
$$V_{CE} = V_C - V_E = 10\ V - 3.2\ V = 6.76\ V$$

(c) V_B and R_1

$$V_B = V_{BE} + V_E = 0.7\ V + 3.24\ V = 3.94\ V$$
$$V_{CC} = I_1 R_1 + V_B$$
$$R_1 = \frac{V_{CC} - V_B}{I_1} \qquad \text{(A)}$$
$$I_1 = I_B + I_2$$

$$I_2 = \frac{V_B}{R_2} = \frac{3.94\text{ V}}{10\text{ kW}} = 0.394\text{ mA}$$

Now $$I_1 = 40\ \mu\text{A} + 0.394\text{ mA} = 0.434\text{ mA}$$

From Equation (A)

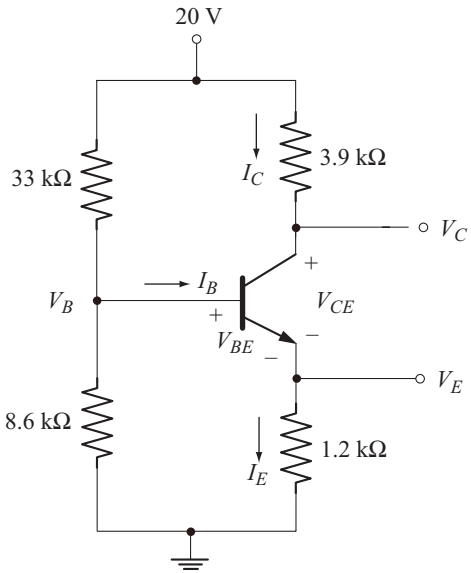
$$R_1 = \frac{16.4\text{ V} - 3.94\text{ V}}{0.434\text{ mA}} = 28.7\ \text{k}\Omega$$

Example 2.13

For the voltage-divider configuration shown below, using the approximate analysis calculate

(a) V_B
(b) I_B and I_C
(c) V_E and V_{CE}

Assume silicon transistor with $\beta = 110$.



Solution

$$\beta R_E = (110)\,(1.2\ \text{k}\Omega) = 132\ \text{k}\Omega$$
$$10\,R_2 = (10)\,(8.6\ \text{k}\Omega) = 86\ \text{k}\Omega$$

Since $\beta R_E > 10\,R_2$, we can use approximate analysis

(a) V_B

$$V_B = V_{Th} = \frac{V_{CC}R_2}{R_1 + R_2} = \frac{(20\text{ V})\,(8.6\text{ kW})}{33\text{ kW} + 8.6\text{ kW}} = 4.13\text{ V}$$

(b) I_B and I_C

$$V_B = V_{BE} + I_E R_E = V_{BE} + [1 + \beta] I_B R_E$$

$$I_B = \frac{V_B - V_{BE}}{[1+\beta]R_E} = \frac{4.13 \text{ V} - 0.7 \text{ V}}{(111)\,(1.2 \text{ kW})} = 25.75 \text{ μA}$$

$$I_C = \beta I_B = (110)\,(25.75 \text{ μA}) = 2.83 \text{ mA}$$

(c) V_E and V_{CE}

$$V_E = I_E R_E$$

$$I_E = I_B + I_C = 25.75 \text{ μA} + 2.83 \text{ mA} = 2.85 \text{ mA}$$

$$V_E = (2.85 \text{ mA})\,(1.2 \text{ kΩ}) = 3.42 \text{ V}$$

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

$$V_{CE} = V_{CC} - I_C R_C - V_E$$

$$= 20 \text{ V} - (2.83 \text{ mA})\,(3.9 \text{ kΩ}) - 3.42 \text{ V} = 5.54 \text{ V}$$

◆ 2.9 COLLECTOR FEEDBACK BIAS

The collector feedback bias circuit is realized by introducing feedback path from the collector to base as shown in Fig. 2.19. The operating point of this circuit is less sensitive to variations in temperature and β when compared to the fixed-bias and emitter-bias circuits.

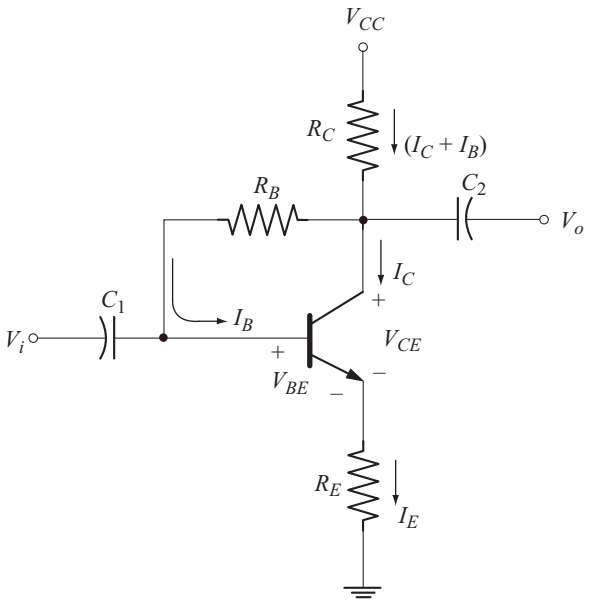


Fig. 2.19 Collector feedback bias circuit

Expressions for I_B and I_C

The dc circuit is shown in Fig. 2.20.

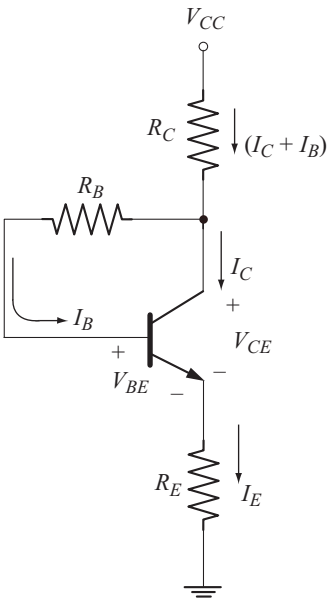


Fig. 2.20 DC circuit

Writing the Kirchhoff's voltage law equation for the base-emitter circuit, we get

$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE} + I_E R_E \tag{2.47}$$

Now $I_C + I_B \simeq I_C$ since $I_B \ll I_C$

and $I_C \simeq I_E$

$\therefore$ Equation (2.47) becomes

$$V_{CC} = I_C R_C + I_B R_B + V_{BE} + I_C R_E$$

Substituting $I_C = \beta I_B$

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE} + \beta I_B R_E$$

$$V_{CC} = I_B R_B + \beta (R_C + R_E) I_B + V_{BE}$$

$$\therefore \quad I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)} \tag{2.48}$$

On comparision with Equation (2.17), it is clear that in the collector feedback circuit besides R_E, collector resistance R_C also gets reflected in the base circuit.

Collector current,

$$I_C = \beta I_B$$

$$\therefore \quad I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + \beta (R_C + R_E)} \tag{2.49}$$

If β is large, then $\beta\,[R_C + R_E] \gg R_B$

$$\therefore \qquad R_B + \beta\,[R_C + R_E] \approx \beta\,[R_C + R_E]$$

Now Equation (2.49) reduces to

$$I_C \approx \frac{V_{CC} - V_{BE}}{R_C + R_E} \tag{2.50}$$

Observe that the collector current becomes independent of β under these conditions and hence is independent of variations in β.

Expression for V_{CE}

Applying KVL to the collector-emitter circuit of Fig. 2.20 we get

$$V_{CC} = R_C\,[I_C + I_B] + V_{CE} + I_E R_E \tag{2.51}$$

As in the computation of base current,

$$I_C + I_B \simeq I_C \quad \text{and} \quad I_E \simeq I_C$$

$$\therefore \qquad V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$\therefore \qquad V_{CE} = V_{CC} - I_C\,(R_C + R_E) \tag{2.52}$$

which is the same as Equation (2.35) derived for the voltage-divider bias circuit.

Transistor Saturation

When the transistor is in saturation, $V_{CE\,(\text{sat})} \approx 0$. From Equation (2.52), the collector current at saturation is given by

$$I_{C\,(\text{sat})} = \frac{V_{CC}}{R_C + R_E} \tag{2.53}$$

Observe that $I_{C\,(\text{sat})}$ is same as that of emitter bias and voltage divider bias circuits given in Equations (2.28) and (2.39) respectively.

Example 2.14

The following circuit values are given for the collector feedback bias circuit of Fig. 2.19.
$V_{CC} = 12$ V $\quad R_C = 4.7$ kΩ $\quad R_B = 220$ kΩ $\quad R_E = 1$ kΩ. Assuming silicon transistor

(a) Find the operating point for the circuit shown using silicon transistor with $\beta = 90$.

(b) Find the operating point for $\beta = 150$.

Solution

(a) When $\beta = 90$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{12\text{ V} - 0.7\text{ V}}{220\text{ kW} + 90(4.7\text{ kW} + 1\text{ kW})} = 15.42\ \mu\text{A}$$

$$I_C = \beta I_B = 90 \times 15.42\ \mu\text{A} = 1.39\text{ mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$
$$= 12\text{ V} - 1.39\text{ mA} \times (4.7\text{ k}\Omega + 1\text{ k}\Omega) = 4.08\text{ V}$$

(b) For $\beta = 150$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{12\text{ V} - 0.7\text{ V}}{220\text{ kW} + 150(4.7\text{ kW} + 1\text{ kW})} = 10.51\ \mu\text{A}$$

$$I_C = \beta I_B = 150 \times 10.51\ \mu\text{A} = 1.58\text{ mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$
$$= 12\text{ V} - 1.58\text{ mA}\ (4.7\text{ k}\Omega + 1\text{ k}\Omega) = 3\text{V}$$

Let us now tabulate the results for $\beta = 90$ and $\beta = 150$.

β	I_{BQ}	I_{CQ}	V_{CEQ}
90	15.42 μA	1.39 mA	4.08 V
150	10.51 μA	1.58 mA	3V

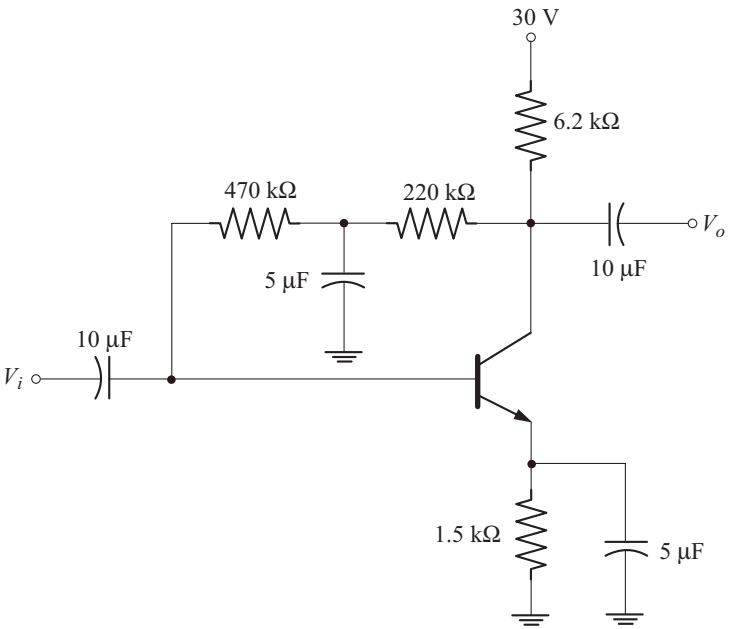
Observe that a large change in β causes a small shift in the operating point well within the active region.

Example 2.15

For the circuit shown below, determine

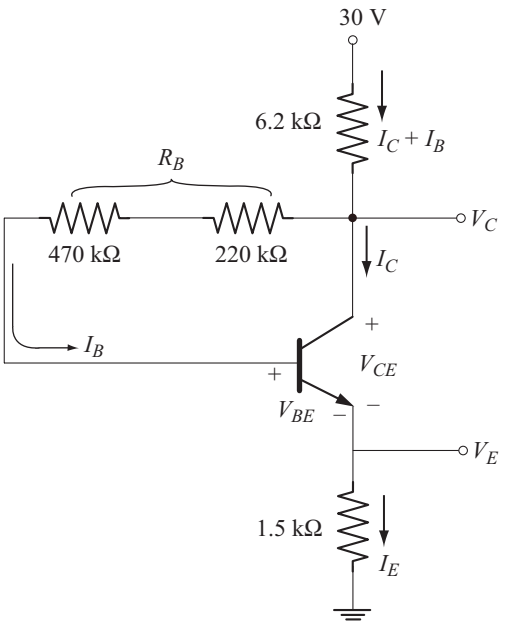
(a) I_B and I_C (b) V_{CE} and V_C (c) V_E and $I_{C\,(sat)}$

Assume silicon transistor with $\beta = 100$.



Solution

Let us write the dc circuit by open circuiting all capacitors.



From the circuit

$$R_B = 470\ \text{k}\Omega + 220\ \text{k}\Omega = 690\ \text{k}\Omega$$

(a) I_B and I_C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{30\ \text{V} - 0.7\ \text{V}}{690\ \text{kW} + 100[6.2\ \text{kW} + 1.5\ \text{kW}]} = 20.07\ \mu\text{A}$$

$$I_C = \beta I_B = (100)\ (20.07\ \mu\text{A}) = 2.01\ \text{mA}$$

(b) V_{CE} and V_C

$$V_{CE} = V_{CC} - I_C\,[R_C + R_E] \qquad [\text{Neglecting } I_B]$$
$$= 30\ \text{V} - 2.01\ \text{mA}\ [6.2\ \text{k}\Omega + 1.5\ \text{k}\Omega] = 14.52\ \text{V}$$
$$V_C = V_{CC} - I_C R_C = 30\ \text{V} - (2.01\ \text{mA})\ (6.2\ \text{k}\Omega) = 17.54\ \text{V}$$

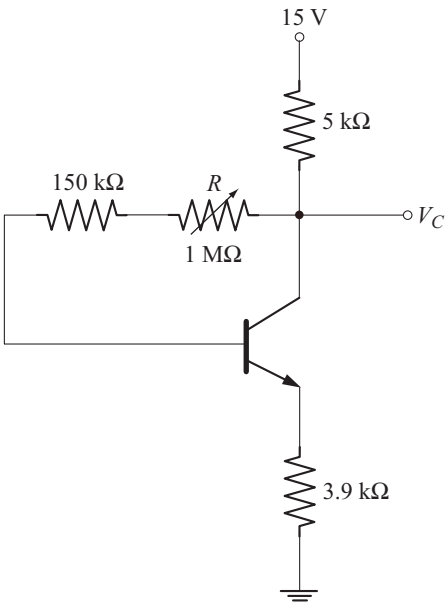
(c) V_E and $I_{C\,(\text{sat})}$

$$V_E = I_E R_E \approx I_C R_E = (2.01\ \text{mA})\ (1.5\ \text{k}\Omega) = 3.02\ \text{V}$$

$$I_{C\,(\text{sat})} = \frac{V_{CC}}{R_C + R_E} = \frac{30\ \text{V}}{6.2\ \text{kW} + 1.5\ \text{kW}} = 3.89\ \text{mA}$$

Example 2.16

For the circuit shown determine the range of possible values for V_C. Assume silicon transistor with $\beta = 200$.



Solution:

Let $R_B = 150\ \text{k}\Omega + R$

R varies between 0 and 1 MΩ.

When $R = 0\ \Omega$, $R_B = 150\ \text{k}\Omega$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{15\ \text{V} - 0.7\ \text{V}}{150\ \text{kW} + 200(5\ \text{kW} + 3.9\ \text{kW})} = 7.4\ \mu\text{A}$$

$$I_C = \beta I_B = (200)\ (7.4\ \mu\text{A}) = 1.48\ \text{mA}$$

$$V_C = V_{CC} - [I_C + I_B]\ R_C$$

$$= 15\ \text{V} - [1.48\ \text{mA} + 7.4\ \mu\text{A}]\ 5\ \text{k}\Omega = 7.56\ \text{V}$$

When $R = 1\ \text{M}\Omega$, $R_B = 150\ \text{k}\Omega + 1\ \text{M}\Omega = 1.15\ \text{M}\Omega$

$$I_B = \frac{15\ \text{V} - 0.7\ \text{V}}{1.15\ \text{MW} + 200(5\ \text{kW} + 3.9\ \text{kW})} = 4.88\ \mu\text{A}$$

$$I_C = \beta I_B = (200)\ (4.88\ \mu\text{A}) = 0.976\ \text{mA}$$

$$V_C = 15\ \text{V} - [0.976\ \text{mA} + 4.88\ \mu\text{A}]\ 5\ \text{k}\Omega = 10\ \text{V}$$

V_C changes from 7.56 V to 10 V when R is varied from 0 to 1 MΩ.

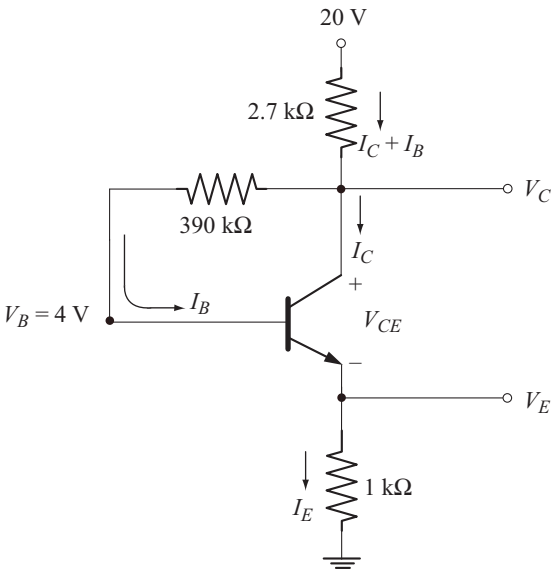
Example 2.17

For the circuit shown below determine

(a) V_E and I_E

(b) V_C and I_B

(c) I_C, V_{CE} and β



Solution

(a) V_E and I_E

$$V_B = V_{BE} + V_E$$
$$V_E = V_B - V_{BE} = 4\text{ V} - 0.7\text{ V} = 3.3\text{ V}$$
$$I_E = \frac{V_E}{R_E} = \frac{3.3\text{ V}}{1\text{ k}\Omega} = 3.3\text{ mA}$$

(b) V_E and I_B

$$V_{CC} = (I_C + I_B)\,R_C + V_C$$
$$V_C = V_{CC} - I_E\,R_C = 20\text{ V} - (3.3\text{ mA})\,(2.7\text{ k}\Omega) = 11.09\text{ V}$$
$$I_B = \frac{V_C - V_B}{R_B} = \frac{11.09\text{ V} - 4\text{ V}}{390\text{ k}\Omega} = 18.17\ \mu\text{A}$$

(c) I_C, V_{CE} and β

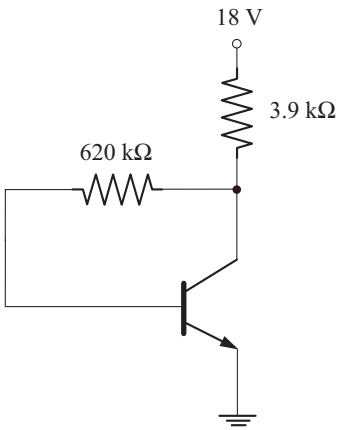
$$I_C = I_E - I_B = 3.3\text{ mA} - 18.17\ \mu\text{A} = 3.28\text{ mA}$$
$$V_{CE} = V_C - V_E = 11.09\text{ V} - 3.3\text{ V} = 7.79\text{ V}$$
$$\beta = \frac{I_C}{I_B} = \frac{3.28\text{ mA}}{18.17\ \mu\text{A}} = 180.5$$

Example 2.18

For the circuit shown below calculate

(a) I_{CQ} and V_{CEQ}
(b) V_E and V_B
(c) V_C and V_{BC}

Assume silicon transistor with $\beta = 150$.



Solution

The given circuit is nothing but collector feedback circuit with $R_E = 0\ \Omega$.

(a) I_{CQ} and V_{CEQ}

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta\left[R_C + R_E\right]} = \frac{18\text{ V} - 0.7\text{ V}}{620\text{ k}\Omega + (150)(3.9\text{ k}\Omega)} = 14.35\ \mu\text{A}$$

$$I_C = \beta\, I_B = (150)\ (14.35\ \mu\text{A}) = 2.15\text{ mA}$$

$$V_{CE} = V_{CC} - [I_C + I_B]\, R_C$$

$$= 18\text{ V} - [2.15\text{ mA} + 14.35\ \mu\text{A}]\ [3.9\text{ k}\Omega] = 9.55\text{ V}$$

(b) V_E and V_B

$$V_E = I_E R_E = (I_E)\ (0\ \Omega) = 0\text{ V}$$

$$V_B = V_{BE} + V_E = V_{BE} = 0.7\text{ V}$$

(c) V_C and V_{BC}

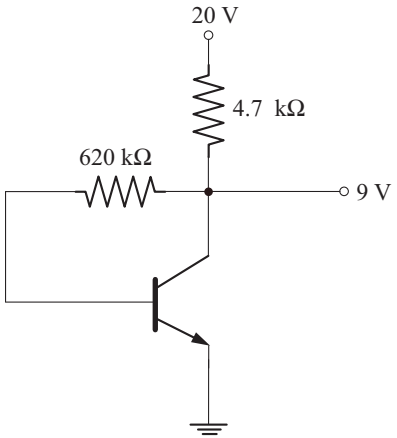
$$V_C = V_{CE} + V_E = V_{CE} = 9.55\text{ V}$$

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 9.55\text{ V} = -8.85\text{ V}$$

Example 2.19

For the circuit shown below calculate

(a) I_B and I_C (b) β and V_{CE}



Solution

Given $V_C = 9$ V

Since $R_E = 0\ \Omega$

$$V_E = 0 \text{ V}$$

$$\therefore \quad V_C = V_{CE} = 9 \text{ V}$$

and $$V_B = V_{BE} = 0.7 \text{ V}$$

(a) I_B and I_C

$$I_B = \frac{V_C - V_B}{R_B} = \frac{9 \text{ V} - 0.7 \text{ V}}{620 \text{ k}\Omega} = 13.38\ \mu\text{A}$$

$$I_C = \frac{V_{CC} - V_C}{R_C} = \frac{20 \text{ V} - 9 \text{ V}}{4.7 \text{ k}\Omega} = 2.34 \text{ mA}$$

(b) β and V_{CE}

$$\beta = \frac{I_C}{I_B} = \frac{2.34 \text{ mA}}{13.38\ \mu\text{A}} = 174.88$$

$$V_{CE} = V_C = 9 \text{ V}$$

Example 2.20

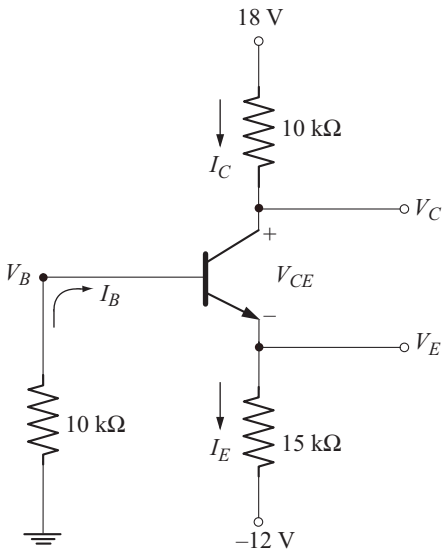
For the circuit shown below determine

(a) I_B and I_C

(b) V_E and V_B

(c) V_C and V_{CE}

Assume silicon transistor with $\beta = 150$.



Solution

(a) I_B and I_C

Applying KVL to base-emitter circuit, we get

$$-I_B\,(10\ \text{k}\Omega) - V_{BE} - I_E\,(15\ \text{k}\Omega) + 12\ \text{V} = 0 \qquad \text{(A)}$$

$$I_E = (1+\beta)\,I_B = 151\,I_B$$

Using this relation in Equation (A) we have

$$12\ \text{V} - V_{BE} = I_B\,(10\ \text{k}\Omega) + 151\,I_B\,(15\ \text{k}\Omega)$$

$$I_B = \frac{12\ \text{V} - 0.7\ \text{V}}{10\ \text{k}\Omega + (151)(15\ \text{k}\Omega)} = 4.96\ \mu\text{A}$$

$$I_C = \beta\,I_B = (150)\,(4.96\ \mu\text{A}) = 0.744\ \text{mA}$$

(b) V_E and V_B

$$I_E = \frac{V_E - (-12\ \text{V})}{15\ \text{k}\Omega}$$

$$\Rightarrow \quad V_E = I_E\,(15\ \text{k}\Omega) - 12\ \text{V}$$

$$I_E = I_B + I_C = 4.96\ \mu\text{A} + 0.744\ \text{mA} = 0.748\ \text{mA}$$

Now

$$V_E = (0.748\ \text{mA})\,(15\ \text{k}\Omega) - 12\ \text{V} = -0.78\ \text{V}$$

$$V_B = V_{BE} + V_E = 0.7\ \text{V} - 0.78\ \text{V} = -0.08\ \text{V}$$

(c) V_C and V_{CE}

$$\begin{aligned} V_C &= V_{CC} - I_C R_C \\ &= 18\text{ V} - (0.744\text{ mA})\,(10\text{ k}\Omega) = 10.56\text{ V} \\ V_{CE} &= V_C - V_E = 10.56\text{ V} - (-0.78\text{ V}) = 11.34\text{ V} \end{aligned}$$

Example 2.21

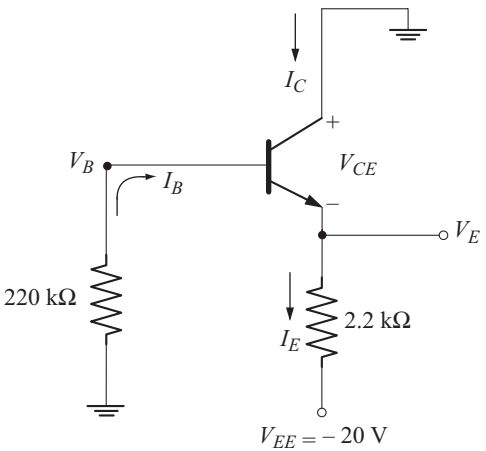
For the circuit shown below determine

(a) I_B, I_C and I_E

(b) V_B and V_E

(c) V_C and V_{CE}

Assume silicon transistor with $\beta = 100$.



Solution

(a) I_B, I_C and I_E

Applying KVL to base emitter circuit we have

$$-I_B\,(220\text{ k}\Omega) - V_{BE} - I_E\,(2.2\text{ k}\Omega) + 20\text{ V} = 0 \qquad \text{(A)}$$

$$I_E = (1+\beta)\,I_B = 101\,I_B$$

Solving for I_B from Equation (A), we obtain

$$I_B = \frac{20\text{ V} - 0.7\text{ V}}{220\text{ k}\Omega + (101)(2.2\text{ k}\Omega)} = 43.64\ \mu\text{A}$$

$$I_C = \beta\, I_B = (100)\,(43.64\ \mu\text{A}) = 4.36\text{ mA}$$

$$I_E = I_B + I_C = 43.64\ \mu\text{A} + 4.36\text{ mA} = 4.4\text{ mA}$$

(b) V_B and V_E

$$I_E = \frac{V_E - (-20\text{ V})}{2.2\text{ k}\Omega}$$

$$\Rightarrow \quad V_E = I_E(2.2\text{ k}\Omega) - 20\text{ V}$$

$$= (4.4\text{ mA})(2.2\text{ k}\Omega) - 20\text{ V} = -10.32\text{ V}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} - 10.32\text{ V} = -9.62\text{ V}$$

Alternatively

$$V_B = -I_B(220\text{ k}\Omega) = -(43.64\ \mu\text{A})(220\text{ k}\Omega) = -9.6\text{ V}$$

(c) V_C and V_{CE}

Since the collector terminal is grounded

$$V_C = 0\text{ V}$$

$$V_{CE} = V_C - V_E = 0\text{ V} - (-10.32\text{ V}) = 10.32\text{ V}$$

Example 2.22

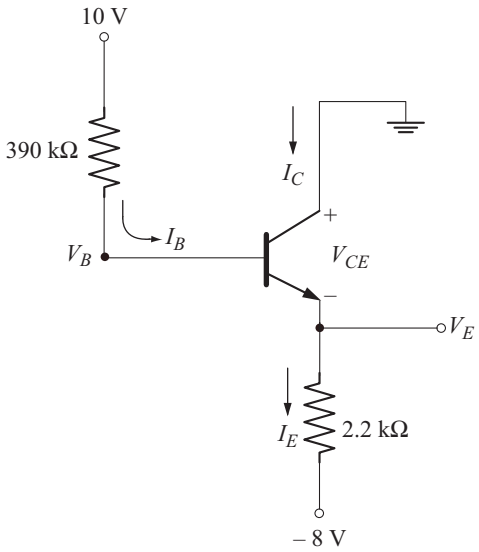
For the circuit shown determine

(a) I_B, I_C and I_E

(b) V_B and V_E

(c) V_C and V_{CE}

Assume silicon transistor with $\beta = 100$.



Solution

(a) I_B, I_C and I_E

Applying KVL to base-emitter circuit, we have

$$10\text{ V} - I_B\,(390\text{ k}\Omega) - V_{BE} - I_E\,(2.2\text{ k}\Omega) + 8\text{ V} = 0$$

Using $I_E = (1+\beta)\,I_B = 101\,I_B$, we have

$$I_B\,[390\text{ k}\Omega + (101)\,(2.2\text{ k}\Omega)] = 17.3\text{ V}$$

$$I_B = \frac{17.3\text{ V}}{612.2\text{ k}\Omega} = 28.25\ \mu\text{A}$$

$$I_C = \beta\,I_B = (100)\,(28.25\ \mu\text{A}) = 2.82\text{ mA}$$

$$I_E = 101\,I_B = (101)\,(28.25\ \mu\text{A}) = 2.85\text{ mA}$$

(b) V_E and V_B

$$I_E = \frac{V_E - (-8\text{ V})}{2.2\text{ k}\Omega}$$

$$\Rightarrow \quad V_E = I_E\,(2.2\text{ k}\Omega) - 8\text{ V}$$

$$= (2.85\text{ mA})\,(2.2\text{ k}\Omega) - 8\text{ V} = -1.73\text{ V}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} - 1.73\text{ V} = -1.03\text{ V}$$

Alternatively

$$I_B = \frac{10\text{ V} - V_B}{390\text{ k}\Omega}$$

$$\Rightarrow \quad V_B = 10\text{ V} - I_B\,(390\text{ k}\Omega)$$

$$= 10\text{ V} - (28.25\ \mu\text{A})\,(390\text{ k}\Omega) = -1.02\text{ V}$$

(c) V_C and V_{CE}

Since the collector terminal is grounded

$$V_C = 0\text{ V}$$

$$V_{CE} = V_C - V_E = 0\text{ V} - (-1.73\text{ V}) = 1.73\text{ V}$$

Example 2.23

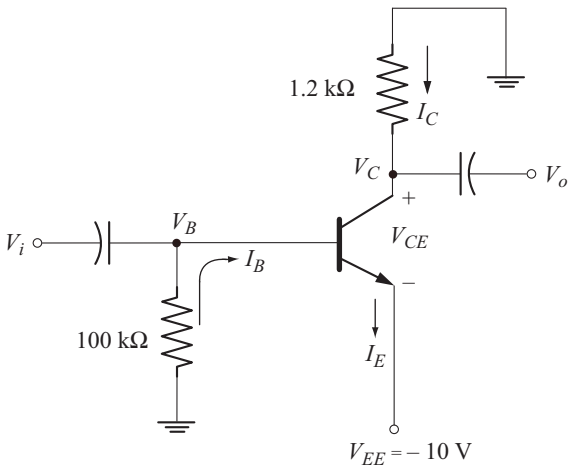
For the circuit shown below determine

(a) I_B, I_C and I_E

(b) V_E and V_B

(c) V_C and V_{CE}

Assume silicon transistor with $\beta = 60$.



Solution

For dc analysis, all capacitors can be treated as open circuits.

(a) I_B, I_C and I_E

Applying KVL to base-emitter circuit, we have

$$-I_B(100\ \text{k}\Omega) - V_{BE} + 10\ \text{V} = 0$$

$$I_B = \frac{10\ \text{V} - 0.7\ \text{V}}{100\ \text{k}\Omega} = 93\ \mu\text{A}$$

$$I_C = \beta I_B = (60)(93\ \mu\text{A}) = 5.58\ \text{mA}$$

$$I_E = I_B + I_C = 93\ \mu\text{A} + 5.58\ \text{mA} = 5.67\ \text{mA}$$

(b) V_E and V_B

Since emitter terminal is connected to V_{EE},

$$V_E = V_{EE} = -10\ \text{V}$$

$$V_B = V_{BE} + V_E = 0.7\ \text{V} - 10\ \text{V} = -9.3\ \text{V}$$

Alternatively, $$V_B = -I_B(100\ \text{k}\Omega) = -(93\ \mu\text{A})(100\ \text{k}\Omega) = -9.3\ \text{V}$$

(c) V_C and V_{CE}

$$I_C = \frac{0\ \text{V} - V_C}{1.2\ \text{k}\Omega}$$

$$\Rightarrow \quad V_C = I_C(1.2\ \text{k}\Omega) = (5.58\ \text{mA})(1.2\ \text{k}\Omega) = 6.69\ \text{V}$$

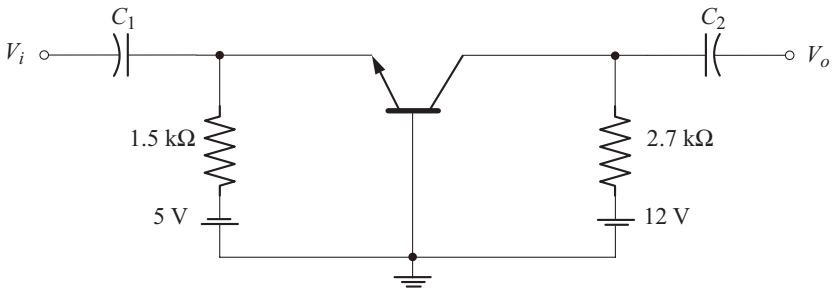
$$V_{CE} = V_C - V_E = 6.69\ \text{V} - (-10\ \text{V}) = 16.69\ \text{V}$$

Example 2.24

For the circuit shown below determine

(a) I_B, I_C and I_E
(b) V_B and V_E
(c) V_C and V_{CE}
(d) V_{CB}

Assume silicon transistor with $\alpha = 0.98$.

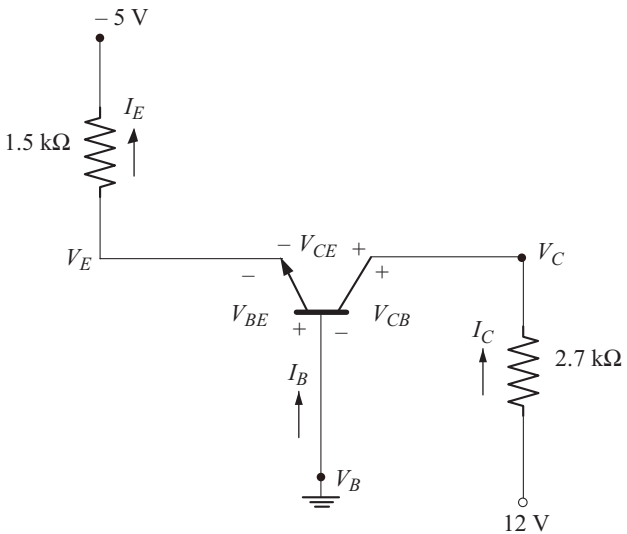


Solution

In the given circuit, the transistor is in CB configuration.

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49.$$

Let us rewrite the given circuit in the convenient form as shown below.



(a) I_B, I_C and I_E

Applying KVL to base-emitter circuit, we have

$$-V_{BE} - I_E (1.5\ \text{k}\Omega) + 5\ \text{V} = 0$$

$$I_E = \frac{5\ \text{V} - 0.7\ \text{V}}{1.5\ \text{k}\Omega} = 2.86\ \text{mA}$$

$$I_B = \frac{I_E}{1+\beta} = \frac{2.86\ \text{mA}}{50} = 57.2\ \mu\text{A}$$

$$I_C = \beta I_B = (49)\ (57.2\ \mu\text{A}) = 2.8\ \text{mA}$$

(b) V_B and V_E

Since the base terminal is grounded

$$V_B = 0\ \text{V}$$

$$I_E = \frac{V_E - (-5\ \text{V})}{1.5\ \text{k}\Omega}$$

$$V_E = I_E (1.5\ \text{k}\Omega) - 5\ \text{V}$$

$$= (2.86\ \text{mA})\ (1.5\ \text{k}\Omega) - 5\ \text{V} = -0.71\ \text{V}$$

It should be noted that, $V_E = -V_{BE}$

(c) V_C and V_{CE}

$$I_C = \frac{12\ \text{V} - V_C}{2.7\ \text{k}\Omega}$$

$\Rightarrow$

$$V_C = 12\ \text{V} - I_C (2.7\ \text{k}\Omega)$$

$$= 12\ \text{V} - (2.8\ \text{mA})\ (2.7\ \text{k}\Omega) = 4.44\ \text{V}$$

$$V_{CE} = V_C - V_E = 4.44\ \text{V} - (-0.71\ \text{V}) = 5.15\ \text{V}$$

(d) V_{CB}

$$V_{CB} = V_C - V_B = 4.44\ \text{V} - 0\ \text{V} = 4.44\ \text{V}$$

Example 2.25

For the circuit shown below calculate

(a) I_B, I_C and I_E

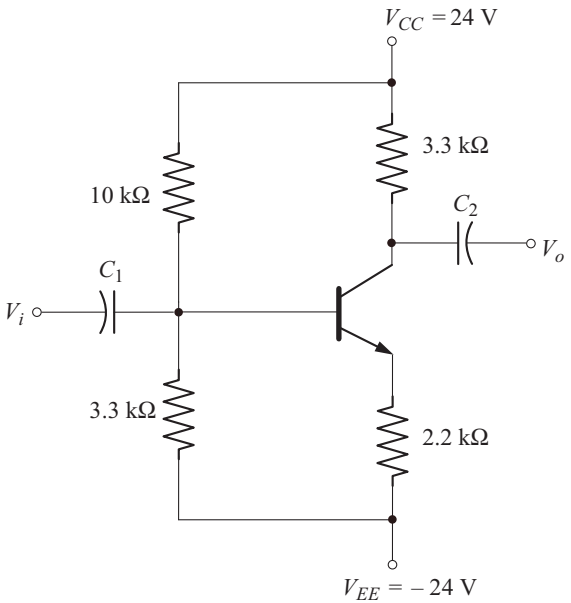
(b) V_E and V_B

(c) V_C and V_{CE}

(d) V_{CB} and $I_{C\,(\text{sat})}$

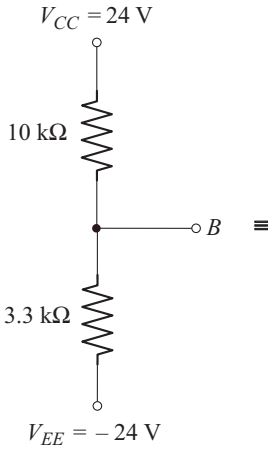
(e) Draw the dc load line and indicate the Q point.

Assume silicon transistor with $\beta = 110$.



Solution

First let us obtain the Thevenin equivalent of the voltage divider network.



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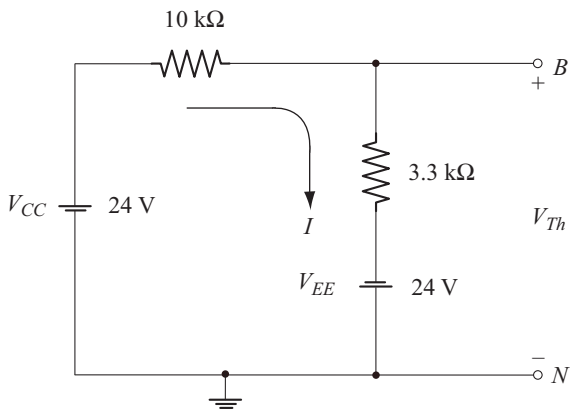


Fig. A Voltage divider network **Fig. B** Circuit to find V_{Th}

Applying KVL to the circuit of Fig. B we have

$$24 \text{ V} - I\,[10 \text{ k}\Omega + 3.3 \text{ k}\Omega] + 24 \text{ V} = 0$$

$$I = \frac{48 \text{ V}}{13.3 \text{ kW}} = 3.61 \text{ mA}$$

also, $$V_{Th} - I\,(3.3 \text{ k}\Omega) + 24 \text{ V} = 0$$

$$V_{Th} = I\,(3.3\ \text{k}\Omega) - 24\ \text{V}$$
$$= (3.61\ \text{mA})\,(3.3\ \text{k}\Omega) - 24\ \text{V} = -12\ \text{V}$$

Negative sign implies that, base terminal is negative with respect to ground.

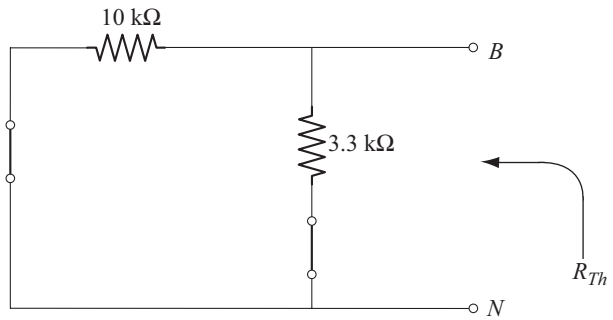


Fig. C Circuit to find R_{Th}

From the circuit of Fig. C.

$$R_{Th} = 10\ \text{k}\Omega \parallel 3.3\ \text{k}\Omega = 2.48\ \text{k}\Omega$$

The given circuit is redrawn in Fig. D with Thevenin equivalent inserted.

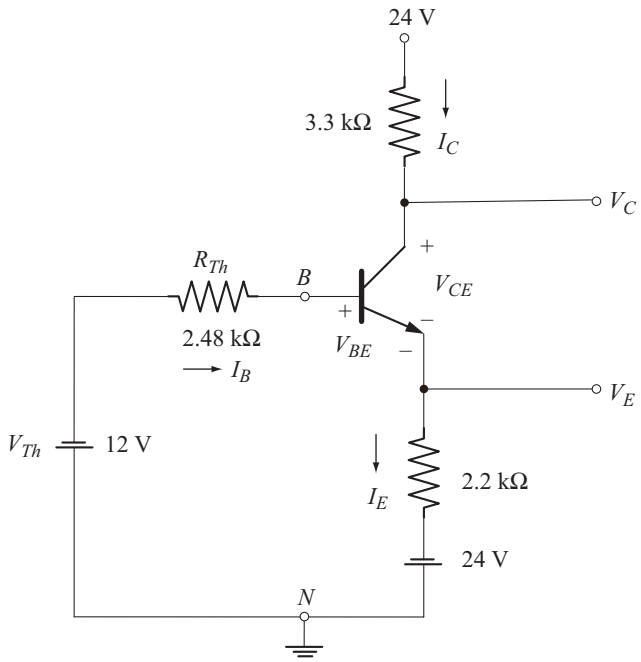


Fig. D

(a) I_B, I_C and I_E

Applying KVL to the base emitter circuit of Fig. D we have

$$-12\text{ V} - I_B(2.48\text{ k}\Omega) - V_{BE} - I_E(2.2\text{ k}\Omega) + 24\text{ V} = 0 \qquad \text{(A)}$$

But $I_E = (1+\beta)\, I_B = 111\, I_B$.

Using this in Equation (A), we have

$$I_B\,[2.48\text{ k}\Omega + (111)(2.2\text{ k}\Omega)] = 12\text{ V} - V_{BE}$$

$$I_B = \frac{12\text{ V} - 0.7\text{ V}}{2.48\text{ k}\Omega + (111)(2.2\text{ k}\Omega)} = 45.8\ \mu\text{A}$$

$$I_C = \beta\, I_B = (110)(45.8\ \mu\text{A}) = 5.03\text{ mA}$$

$$I_E = I_B + I_C = 45.8\ \mu\text{A} + 5.03\text{ mA} = 5.07\text{ mA}$$

(b) V_E and V_B

$$I_E = \frac{V_E - (-24\text{ V})}{2.2\text{ k}\Omega}$$

$$\Rightarrow \quad V_E = I_E(2.2\text{ k}\Omega) - 24\text{ V}$$

$$= (5.07\text{ mA})(2.2\text{ k}\Omega) - 24\text{ V} = -12.84\text{ V}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} - 12.84\text{ V} = -12.14\text{ V}$$

Alternatively, from the circuit of Fig. B

$$V_B = V_{BN} = V_{Th} = -12\text{ V}$$

(c) V_C and V_{CE}

$$I_C = \frac{24\text{ V} - V_C}{3.3\text{ k}\Omega}$$

$$\Rightarrow \quad V_C = 24\text{ V} - I_C(3.3\text{ k}\Omega)$$

$$= 24\text{ V} - (5.03\text{ mA})(3.3\text{ k}\Omega) = 7.4\text{ V}$$

$$V_{CE} = V_C - V_E = 7.4\text{ V} - [-12.84\text{ V}] = 20.24\text{ V}$$

(d) V_{CB} and $I_{C\,(\text{sat})}$

$$V_{CB} = V_C - V_B = 7.4\text{ V} - (-12.14\text{ V}) = 19.54\text{ V}$$

Applying KVL to collector circuit of Fig. D we have

$$24\text{ V} - I_C(3.3\text{ k}\Omega) - V_{CE} - I_E(2.2\text{ k}\Omega) + 24\text{ V} = 0 \qquad \text{(B)}$$

When transistor is in saturation

$$V_{CE\,(\text{sat})} \approx 0\text{ V}$$

taking $I_E \approx I_C$ we have

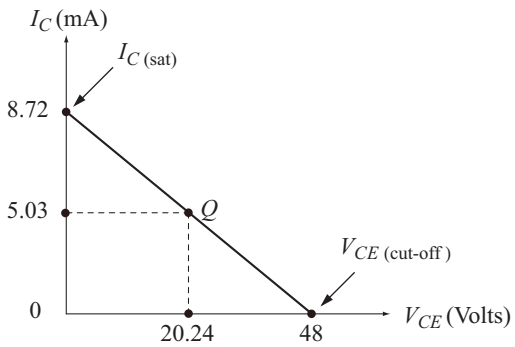
$$I_{C\,(sat)} = \frac{48\text{ V}}{3.3\text{ k}\Omega + 2.2\text{ k}\Omega} = 8.72\text{ mA}$$

(e) DC load line

When transistor is at cut-off, $I_C \approx 0$

From Equation (B) we have

$$V_{CE\,(cut\text{-}off)} = 48\text{ V}$$



Example 2.26

Determine R_C and R_B for a fixed bias configuration using the following data

$V_{CC} = 12\text{ V}$ $I_{CQ} = 2.5\text{ mA}$

$V_{CEQ} = 6\text{ V}$ $\beta = 80$

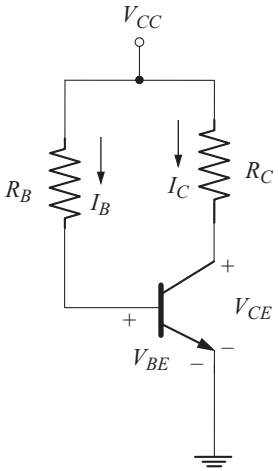
Solution

Calculation of R_C

From the KVL equation of collector emitter circuit we have

$$V_{CC} = I_C R_C + V_{CE}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12\text{ V} - 6\text{ V}}{2.5\text{ mA}} = 2.4\text{ k}\Omega$$



Calculation of R_B

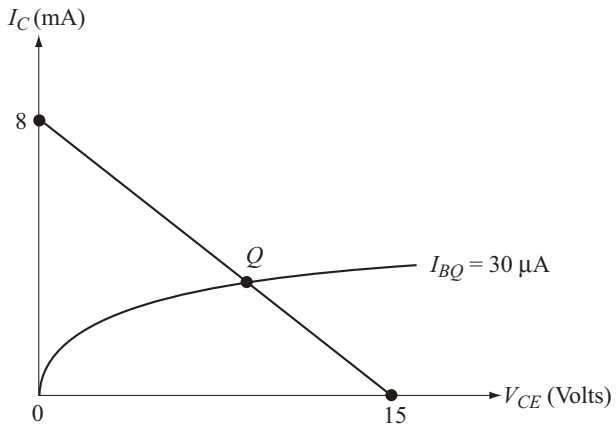
$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$I_B = \frac{I_C}{\beta} = \frac{2.5\text{ mA}}{80} = 31.25\ \mu\text{A}$$

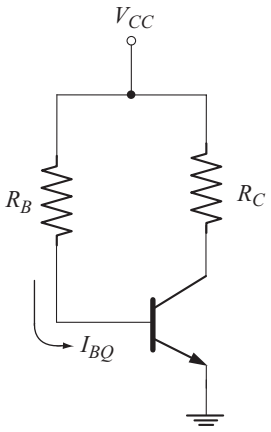
$$R_B = \frac{12\text{ V} - 0.7\text{ V}}{31.25\ \mu\text{A}} = 361.6\text{ k}\Omega$$

Example 2.27

Using the transistor output characteristics of Fig. (a), find the values of V_{CC}, R_B and R_C for the fixed bias configuration of Fig. (b).



(a)



(b)

Solution

From the characteristics of Fig. (a) we get the following data

$V_{CC} = 15$ V $\quad I_{BQ} = I_B = 30$ μA $\quad I_{C\,(sat)} = 8$ mA

$$I_{C\,(sat)} = \frac{V_{CC}}{R_C}$$

$$\therefore \quad R_C = \frac{V_{CC}}{I_{C(sat)}}$$

$$= \frac{15\text{ V}}{8\text{ mA}} = 1.875\text{ k}\Omega$$

From the KVL equation of base-emitter circuit, we have

$$V_{CC} = I_B R_B + V_{BE}$$

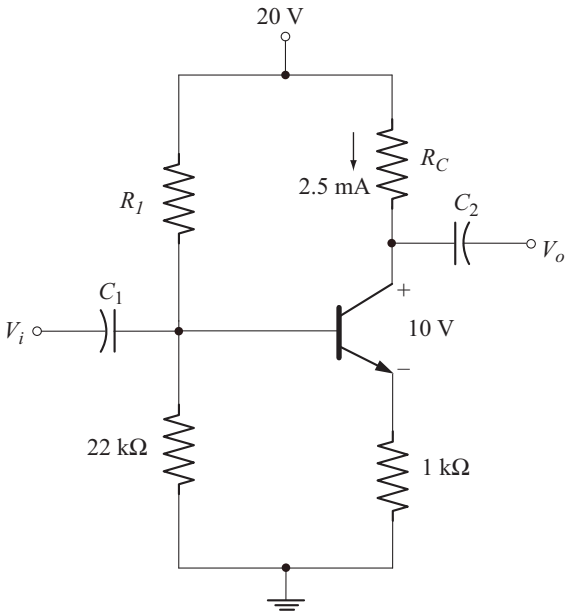
$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{20\text{ V} - 0.7\text{ V}}{30\text{ μA}}$$

$$= 643.33\text{ k}\Omega$$

Example 2.28

For the circuit shown below determine the values of R_1 and R_C.



Solution

Given

$I_{CQ} = I_C = 2.5$ mA $\quad V_{CEQ} = V_{CE} = 10$ V

Calculation of R_1

$$V_B = V_{BE} + V_E$$

$$V_E = I_E R_E \approx I_C R_E = (2.5 \text{ mA})\,(1 \text{ k}\Omega) = 2.5 \text{ V}$$

$$\therefore \quad V_B = 0.7 \text{ V} + 2.5 \text{ V} = 3.2 \text{ V}$$

But

$$V_B = V_{Th} = \frac{V_{CC}\, R_2}{R_1 + R_2}$$

$$3.2 \text{ V} = \frac{(20 \text{ V})(22 \text{ k}\Omega)}{R_1 + 22 \text{ k}\Omega}$$

$$R_1 + 22 \text{ k}\Omega = 137.5 \text{ k}\Omega$$

$$R_1 = 115.5 \text{ k}\Omega$$

Calculation of R_C

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$$\Rightarrow \quad R_C = \frac{V_{CC} - V_C}{I_C} \qquad \text{(A)}$$

$$V_C = V_{CE} + V_E = 10\text{ V} + 2.5\text{ V} = 12.5\text{ V}$$

Now from Equation (A)

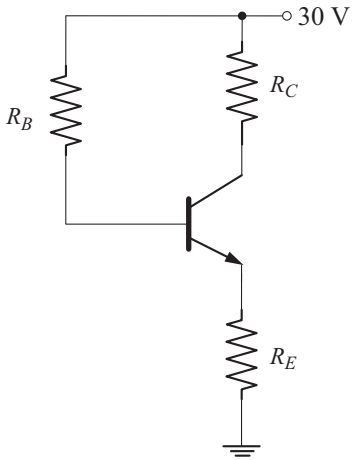
$$R_C = \frac{20\text{ V} - 12.5\text{ V}}{2.5\text{ mA}} = 3\text{ k}\Omega$$

Example 2.29

For the emitter bias circuit shown below find the values of R_C, R_E and R_B using the following specifications.

$$I_{C\,(\text{sat})} = 10\text{ mA}$$
$$I_{CQ} = \frac{1}{2} I_{C\,(\text{sat})}$$
$$V_C = 20\text{ V}$$

Assume silicon transistor with $\beta = 100$.



Solution

Calculation of R_C

$$I_{CQ} = I_C = \frac{1}{2} I_{C\,(\text{sat})} = 5\text{ mA}$$

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{30\text{ V} - 20\text{ V}}{5\text{ mA}} = 2\text{ k}\Omega$$

Calculation of R_E

$$I_{C\,(\text{sat})} = \frac{V_{CC}}{R_C + R_E}$$

$$R_C + R_E = \frac{V_{CC}}{I_{C(\text{sat})}} = \frac{30\text{ V}}{10\text{ mA}} = 3\text{ k}\Omega$$

$$R_E = 3\text{ k}\Omega - R_C = 1\text{ k}\Omega$$

Calculation of R_B

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E} \qquad \text{(A)}$$

$$I_B = \frac{I_C}{\beta} = \frac{5\text{ mA}}{100} = 50\ \mu\text{A}$$

Using this value in Equation (A) we have,

$$50\ \mu\text{A} = \frac{30\ \text{V} - 0.7\ \text{V}}{R_B + (101)(1\ \text{k}\Omega)}$$

$$R_B + 101\ \text{k}\Omega = 586\ \text{k}\Omega$$

$$R_B = 586\ \text{k}\Omega - 101\ \text{k}\Omega = 485\ \text{k}\Omega$$

Example 2.30

Design an emitter stabilized network shown using the following data

$$I_{CQ} = \frac{1}{2} I_{C\ (\text{sat})}$$

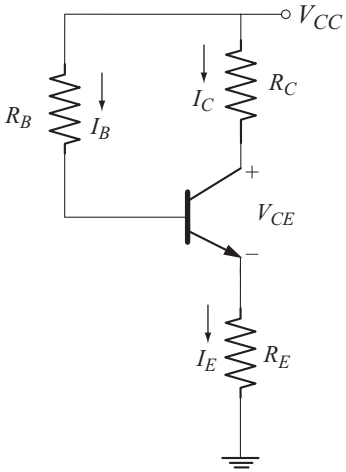
$$V_{CEQ} = \frac{1}{2} V_{CC}$$

$$V_{CC} = 20\ \text{V}$$

$$I_{C\ (\text{sat})} = 10\ \text{mA}$$

$$\beta = 120$$

$$R_C = 4\ R_E$$



Solution

$$I_C = I_{CQ} = \frac{1}{2} I_{C\ (\text{sat})} = \frac{1}{2}(10\ \text{mA}) = 5\ \text{mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{5\ \text{mA}}{120} = 41.66\ \mu\text{A}$$

$$V_{CEQ} = V_{CE} = \frac{1}{2} V_{CC} = \frac{1}{2}(20\ \text{V}) = 10\ \text{V}$$

Calculation of R_C and R_E

From the KVL equation of collector-emitter circuit we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Given $R_C = 4\ R_E$ and taking $I_C \approx I_E$ we have

$$V_{CC} - V_{CE} = I_C\,[5R_E]$$

$$R_E = \frac{V_{CC} - V_{CE}}{5I_C} = \frac{20\text{ V} - 10\text{ V}}{5(5\text{ mA})} = 400\ \Omega$$

$$R_C = 4\,R_E = 1.6\ \text{k}\Omega$$

Calculation of R_B

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$41.66\ \mu\text{A} = \frac{20\text{ V} - 0.7\text{ V}}{R_B + 121(0.4\ \text{k}\Omega)}$$

$$R_B + 48.4\ \text{k}\Omega = \frac{19.3\text{ V}}{41.66\ \mu\text{A}} = 463.27\ \text{k}\Omega$$

$$R_B = 463.27\ \text{k}\Omega - 48.4\ \text{k}\Omega = 414.87\ \text{k}\Omega$$

◆ 2.10 DESIGN RULE

To design the values of biasing circuit elements R_1, R_2 and R_E, the following thumb rules are normally used.

- In emitter stabilized and voltage divider configurations the emitter to ground voltage V_E is taken equal to one-tenth of the dc supply voltage V_{CC}

  i.e., $$V_E = \frac{1}{10}\,V_{CC} \tag{2.54}$$

  R_E is calculated using the relation

  $$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} \tag{2.55}$$

  This rule ensures that, R_E will neither be too large nor be too small. Too large value of R_E reduces the swing of V_{CE} (i.e., output voltage swing) and too small value of R_E degrades the stability of Q point.
- In voltage divider configuration, the resistors R_1 and R_2 are calculated assuming that the current through R_1 and R_2 is at least 10 times greater than the base current. This leads to the condition

  $$R_2 \le \frac{1}{10}\,\beta\,R_E \tag{2.56}$$

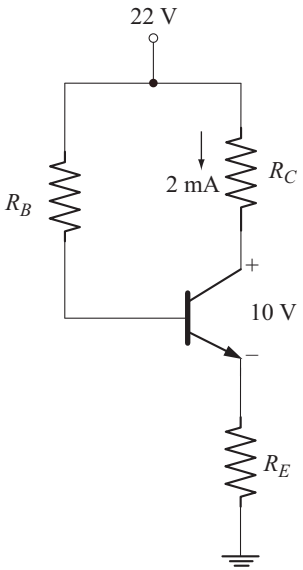
  R_1 is calculated from the relation

  $$V_B = V_{Th} = \frac{V_{CC}\,R_2}{R_1 + R_2} \tag{2.57}$$

Design of biasing networks is considered in the following examples.

Example 2.31

Design the values of R_B, R_E and R_C for the emitter-stabilized bias circuit shown below. Assume silicon transistor with $\beta = 140$.



Solution

Given

$I_{CQ} = I_C = 2$ mA
$V_{CEQ} = V_{CE} = 10$ V $\quad \beta = 140$

There are three unknowns, R_B, R_E and R_C. But we have only the following two equations.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E} \tag{A}$$

$$V_{CC} = I_C R_C + V_{CE} + \underbrace{I_E R_E}_{V_E} \tag{B}$$

To start with the design, we assume V_E. Typically V_E is taken equal to one-tenth of V_{CC}.

$$V_E = \frac{V_{CC}}{10} = \frac{22 \text{ V}}{10} = 2.2 \text{ V}$$

$$V_E = I_E R_E \approx I_C R_E$$

$$\therefore \quad R_E = \frac{V_E}{I_C} = \frac{2.2 \text{ V}}{2 \text{ mA}} = 1.1 \text{ k}\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{140} = 14.28 \ \mu\text{A}$$

From Equation (A)

$$14.26\ \mu A = \frac{22\ V - 0.7\ V}{R_B + (141)(1.1\ k\Omega)}$$

$$R_B + 155.1\ k\Omega = 1493.68\ k\Omega$$

$$R_B = 1.33\ M\Omega$$

From Equation (B)

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{22\ V - 10\ V - 2.2\ V}{2\ mA} = 4.9\ k\Omega$$

Example 2.32

Determine the values of R_C, R_E, R_1 and R_2 for the current-gain stabilized (Beta-independent) circuit with $I_C = 10$ mA, $V_{CE} = 12$V and $V_{CC} = 24$ V. Assume silicon transistor with $\beta_{(min)} = 100$.

Solution

Current-gain stabilized (Beta-independent) circuit is nothing but voltage divider bias circuit.

Given

$I_{CQ} = I_C = 10$ mA $\quad V_{CEQ} = V_{CE} = 12$ V $\quad \beta_{(min)} = \beta = 100$

Calculation of R_E

Let $\quad V_E = \frac{V_{CC}}{10}$

$\therefore \quad V_E = \frac{24\ V}{10} = 2.4\ V$

$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} = \frac{2.4\ V}{10\ mA} = 240\ \Omega$$

Calculation of R_C

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$\Rightarrow \quad R_C = \frac{V_{CC} - V_C}{I_C}$

$$V_C = V_{CE} + V_E = 12\ V + 2.4\ V = 14.4\ V$$

$$R_C = \frac{24\ V - 14.4\ V}{10\ mA} = 960\ \Omega$$

Calculation R_1 and R_2

$$V_B = \frac{V_{CC}\ R_2}{R_1 + R_2} \quad (A)$$

$$V_B = V_{BE} + V_E = 0.7\ V + 2.4\ V = 3.1\ V$$

In Equation (A), we have two unknowns R_1 and R_2.
Let us assume that the current through R_1 and R_2 is 10 times more than I_B. This implies that

$$R_2 \leq \frac{\beta R_E}{10}$$

$$R_2 \leq \frac{(100)(240\ \Omega)}{10}$$

$$R_2 \leq 2.4\ \text{k}\Omega$$

Let $R_2 = 2.4\ \text{k}\Omega$

From Equation (A)

$$3.1\ \text{V} = \frac{(24\ \text{V})(2.4\ \text{k}\Omega)}{R_1 + 2.4\ \text{k}\Omega}$$

$$R_1 + 2.4\ \text{k}\Omega = 18.58\ \text{k}\Omega$$

$$R_1 = 16.18\ \text{k}\Omega$$

◆ 2.11 CIRCUITS WITH PNP TRANSISTORS

So for we have analysed biasing configurations using *npn* transistors. Now let us consider the circuits with *pnp* transistor.

2.11.1 Emitter-stabilized Configuration using pnp Transistor

Figure 2.21 shows emitter-stabilized configuration with *pnp* transistor.

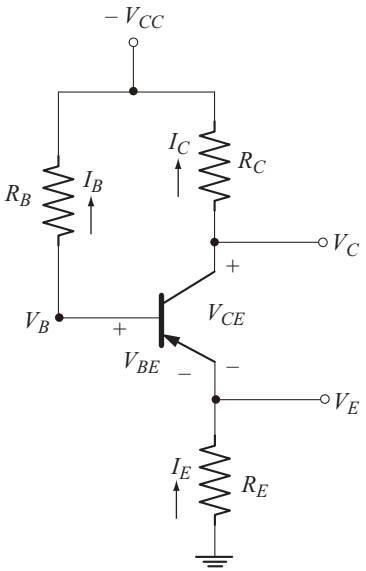


Fig. 2.21 Emitter-stabilized configuration using pnp transistor

It is necessary to make the following observations regarding the current directions and voltage polarities employed for *pnp* transistor in contrast with those of *npn* transistor.

- The directions of I_B, I_C and I_E in *pnp* transistor are exactly opposite to that of *npn* transistor. Since the correct directions of currents are taken in Fig. 2.21, numerical values of these currents will be positive.
- The polarities of V_{CE}, V_{BE}, V_C, V_E etc are retained as in the case of *npn* transistor. Since the actual polarities are the other way, numerical values of these voltages will be negative.
- *pnp* transistor requires negative dc supply $-V_{CC}$ in the collector circuit.

Circuit Analysis

Applying KVL to base-emitter circuit, we have

$$-I_E R_E + V_{BE} - I_B R_B + V_{CC} = 0$$

Using $I_E = (1+\beta)\, I_B$, we obtain

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (1+\beta) R_E} \tag{2.58}$$

It should be note that, V_{CC} is positive and V_{BE} is – 0.7 V for *pnp* silicon transistor. This results in positive value for I_B.

Applying KVL to collector, emitter circuit we have

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

$$V_{CE} = -V_{CC} + I_C R_C + I_E R_E \tag{2.59}$$

Since the direction of I_E is reversed but the polarity of V_E is retained

$$V_E = -I_E R_E \tag{2.60}$$

As in case of *npn* transistor

$$V_B = V_{BE} + V_E \tag{2.61}$$

$$V_C = V_{CE} + V_E \tag{2.62}$$

and

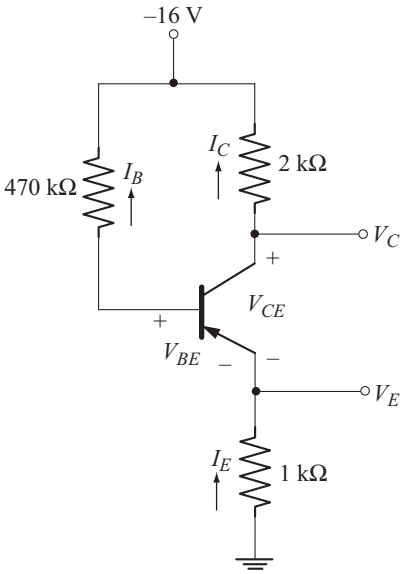
$$V_{CB} = V_C - V_B \tag{2.63}$$

Example 2.33

For the emitter-stabilized bias configuration shown below determine

(a) I_B, I_C and I_E
(b) V_E and V_B
(c) V_{CE} and V_C
(d) V_{CB} and $I_{C\,(sat)}$

Assume silicon transistor with $\beta = 75$.



Solution

The circuit uses *pnp* silicon transistor

$$\therefore \qquad V_{BE} = -0.7 \text{ V}$$

$$\text{also} \qquad -V_{CC} = -16 \text{ V} \quad \Rightarrow \quad V_{CC} = 16 \text{ V}$$

(a) I_B, I_C and I_E

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (1+\beta)R_E}$$

$$= \frac{16 \text{ V} - 0.7 \text{ V}}{470 \text{ k}\Omega + (76)(1 \text{ k}\Omega)} = 28.02 \ \mu\text{A}$$

$$I_C = \beta I_B = (75)\ (28.02 \ \mu\text{A}) = 2.1 \text{ mA}$$

$$I_E = I_C + I_B = 2.1 \text{ mA} + 28.02 \ \mu\text{A} = 2.12 \text{ mA}$$

(b) V_E and V_B

$$V_E = -I_E R_E = -(2.12 \text{ mA})\ (1 \text{ k}\Omega) = -2.12 \text{ V}$$

$$V_B = V_{BE} + V_E = -0.7 \text{ V} - 2.12 \text{ V} = -2.82 \text{ V}$$

(c) V_{CE} and V_C

$$V_{CE} = -V_{CC} + I_C R_C + I_E R_E$$

$$= -16 \text{ V} + (2.1 \text{ mA})\ (2 \text{ k}\Omega) + (2.12 \text{ mA})\ (1 \text{ k}\Omega)$$

$$= -9.68 \text{ V}$$

$$V_C = V_{CE} + V_E = -9.68 \text{ V} - 2.12 \text{ V} = -11.8 \text{ V}$$

(d) V_{CB} and $I_{C\,(sat)}$

$$V_{CB} = V_C - V_B = -11.8\text{ V} - (-2.82\text{ V}) = -8.98\text{ V}$$

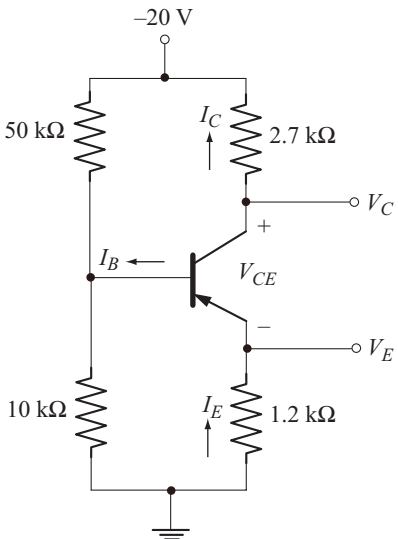
$$I_{C\,(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{16\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = 5.33\text{ mA}$$

Example 2.34

For the voltage divider configuration shown below calculate

(a) $I_B, I_C,$ and I_E
(b) V_E and V_B
(c) V_{CE} and V_C
(d) V_{CB} and $I_{C\,(sat)}$

Assume silicon transistor with $\beta = 110$.



Solution

$$-V_{CC} = -20\text{ V} \Rightarrow V_{CC} = 20\text{ V}$$

$$V_{BE} = -0.7\text{ V} \quad (pnp \text{ Si transistor})$$

(a) $I_B, I_C,$ and I_E

$$I_B = \frac{V_{Th} + V_{BE}}{R_{Th} + (1+\beta)R_E} \tag{A}$$

$$V_{Th} = \frac{V_{CC}\,R_2}{R_1 + R_2} = \frac{(20\text{ V})(10\text{ k}\Omega)}{50\text{ k}\Omega + 10\text{ k}\Omega} = 3.33\text{ V}$$

$$R_{Th} = R_1 \,||\, R_2 = 50\text{ k}\Omega \,||\, 10\text{ k}\Omega = 8.33\text{ k}\Omega$$

$$I_B = \frac{3.33\text{ V} - 0.7\text{ V}}{8.33\text{ k}\Omega + (111)(1.2\text{ k}\Omega)} = 18.58\ \mu\text{A}$$

$$I_C = \beta I_B = (110)\ (18.58\ \mu\text{A}) = 2.04\text{ mA}$$

$$I_E = I_C + I_B = 2.05\text{ mA}$$

(b) V_E and V_B

$$V_E = -I_E R_E = -(2.05\text{ mA})\ (1.2\text{ k}\Omega) = -2.46\text{ V}$$

$$V_B = V_{BE} + V_E = -0.7\text{ V} - 2.46\text{ V} = -3.16\text{ V}$$

(c) V_{CE} and V_C

$$V_{CE} = -V_{CC} + I_C R_C + I_E R_E$$

$$= -20\text{ V} + (2.04\text{ mA})\ (2.7\text{ k}\Omega) + (2.05\text{ mA})\ (1.2\text{ k}\Omega)$$

$$= -12.03\text{ V}$$

$$V_C = V_{CE} + V_E = -12.03\text{ V} - 2.46\text{ V} = -14.49\text{ V}$$

(d) V_{CB} and $I_{C\,(\text{sat})}$

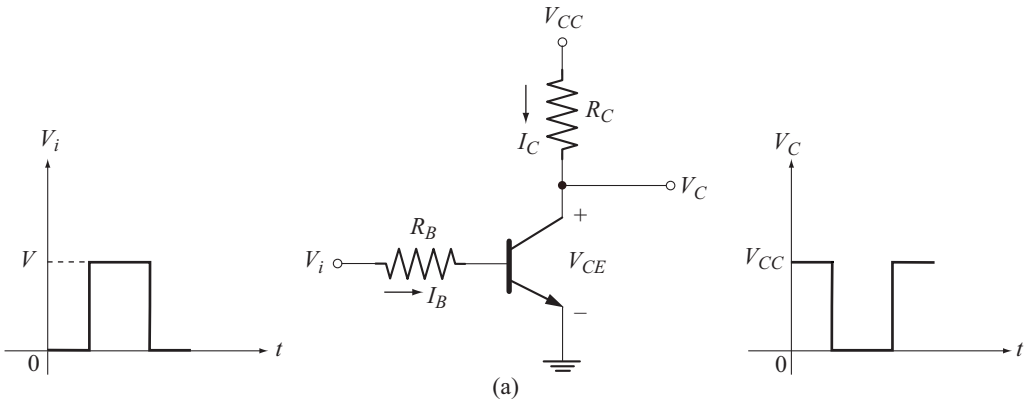
$$V_{CB} = V_C - V_B = -14.49\text{ V} - (-3.16\text{ V}) = -11.33\text{ V}$$

$$I_{C\,(\text{sat})} = \frac{V_{CC}}{R_C + R_E} = \frac{20\text{ V}}{2.7\text{ k}\Omega + 1.2\text{ k}\Omega} = 5.13\text{ mA}$$

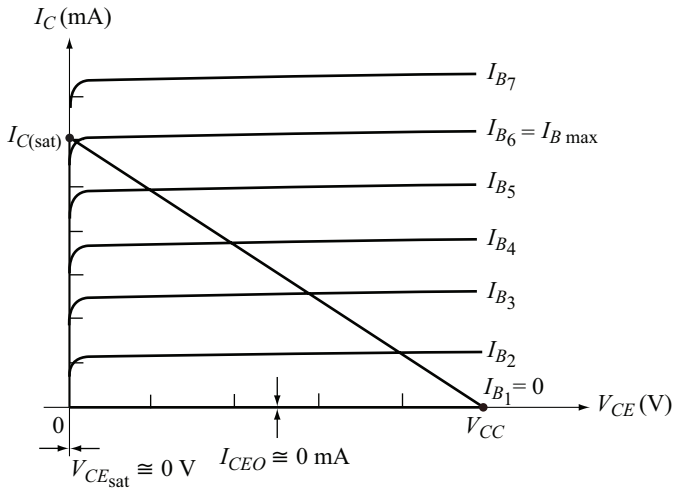
◆ 2.12 TRANSISTOR SWITCHING NETWORKS

When biased in the middle of active region, transistor works as a faith full amplifier. So far we have studied biasing configurations which biases the transistor in the active region. When operated between cut-off and saturation, transistor works as a switch or an inverter. Such a switching circuit is useful in computers and control applications

Fig. 2.22(a) shows the transistor switch and the output characteristics of the transistor is shown in Fig. 2.22(b).



(a)



(b)

Fig. 2.22 (a) Transistor switch (b) Output characteristics

Applying KVL to the base-emitter circuit, we have

$$V_i = I_B R_B + V_{BE}$$

$$I_B = \frac{V_I - V_{BE}}{R_B} \tag{2.64}$$

For the collector, emitter circuit

$$V_{CC} = I_C R_C + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \tag{2.65}$$

The output voltage is

$$V_C = V_{CE} \tag{2.66}$$

Now let us consider the following cases.

Case (i) **:** When $V_i = $ V

This high input voltage will turn on the transistor. Let us assume that, R_B is properly selected so as to produce heavy base current which drives the transistor in to saturation.

In saturation, $V_{CE} = V_{CE\,(sat)}$

and $I_C = I_{C\,(sat)}$

For silicon transistor $V_{CE\,(sat)}$ is typically 0.1 V – 0.3 V.

From Equation (2.65), the collector current at saturation is given by

$$I_{C\,(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \tag{2.67}$$

and from Equation (2.66), the output voltage is

$$V_C = V_{CE\ (\text{sat})} \tag{2.68}$$

From Equation (2.64), the base current is

$$I_B = \frac{V - V_{BE}}{R_B} \tag{2.69}$$

Just before saturation, the transistor is in the active region. The base current in the active region just before saturation is approximately given by

$$I_{B\,(\text{max})} \approx \frac{I_{C(\text{sat})}}{\beta_{dc}} \tag{2.70}$$

Some times β_{dc} is also denoted by h_{FE}.

To ensure saturation, the level of I_B given by Equation (2.69) must be greater than $I_{B\,(\text{max})}$ given in Equation (2.70).

i.e., $$I_B > \frac{I_{C(\text{sat})}}{\beta_{dc}} \tag{2.71}$$

Typically I_B is taken equal to 120 – 150% of $I_{B\ (\text{max})}$ to ensure saturation.

The resistance between collector and emitter terminals, at saturation is

$$R_{(\text{sat})} = \frac{V_{CE(\text{sat})}}{I_{C(\text{sat})}} \tag{2.72}$$

Under ideal conditions, $V_{CE(\text{sat})} \approx 0$ V

From Equation (2.67),

$$I_{C(\text{sat})} \approx \frac{V_{CC}}{R_C} \tag{2.73}$$

From Equation (2.66),

$$V_C \approx 0 \text{ V} \tag{2.74}$$

and from Equation (2.72)

$$R_{(\text{sat})} \approx 0\ \Omega \tag{2.75}$$

Note that, when transistor operates in saturation, there exists a short circuit between collector and emitter terminals.

Figure 2.23 shows the representation of saturated transistor.

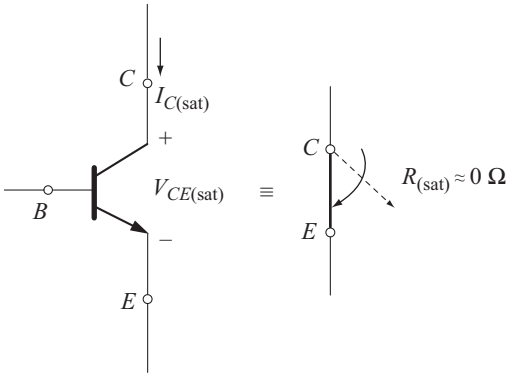


Fig. 2.23 Representation of saturated transistor

Case (ii) **:** When $V_i = 0$

When $V_i = 0$, $I_B = 0$, only leakage current I_{CEO} flows from collector to emitter and the transistor is driven into cut-off.

$$\therefore \qquad I_C = I_{CEO} \tag{2.76}$$

I_{CEO} is in the order of few microamperes.

From Equation (2.65), the output voltage is

$$V_C = V_{CE(\text{cut-off})} = V_{CC} - I_{CEO} R_C \tag{2.77}$$

The resistance between collector and emitter terminals, at cut-off is

$$R_{(\text{cut-off})} = \frac{V_{CE(\text{cut-off})}}{I_{CEO}} \tag{2.78}$$

Under ideal conditions, $I_{CEO} \approx 0$.

Now from Equation (2.77),

$$V_C = V_{CE(\text{cut-off})} = V_{CC} \tag{2.79}$$

and from Equation (2.78),

$$R_{(\text{cut-off})} = \frac{V_{CC}}{0} = \infty\ \Omega \tag{2.80}$$

Observe that, there exists an open circuit between collector and emitter terminals when the transistor operates in the cut-off region.

The representation of transistor when operates in the cut-off region is shown in Fig. 2.24.

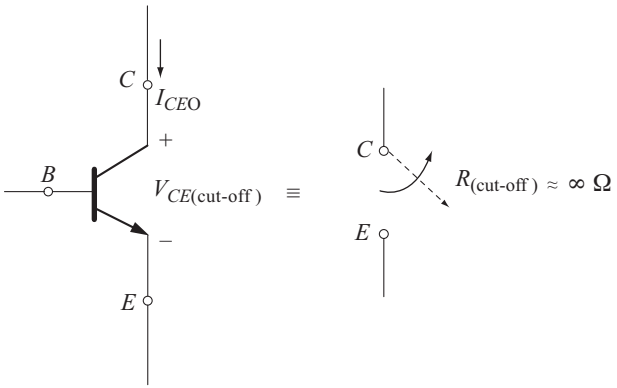


Fig. 2.24 Representation of transistor when operating at cut-off

Summary

A high input voltage drives the transistor into saturation. When in saturation, the transistor

- Conducts heavy collector current, $I_{C(\text{sat})} \approx \dfrac{V_{CC}}{R_C}$
- Has low voltage between collector and emitter terminals

$$V_C = V_{CE(\text{sat})} \approx 0\ \text{V}$$

- Has zero resistance (short circuit) from collector to emitter
- Acts as a closed switch

A low input voltage (0 V) drives the transistor into cut-off. When at cut-off the transistor

- Does not conduct, $I_C = I_{CEO} \approx 0$
- has high voltage between collector and emitter terminals

$$V_E = V_{CE} \approx V_{CC}$$

- has infinite resistance (open circuit) from collector to emitter
- acts as an opened switch

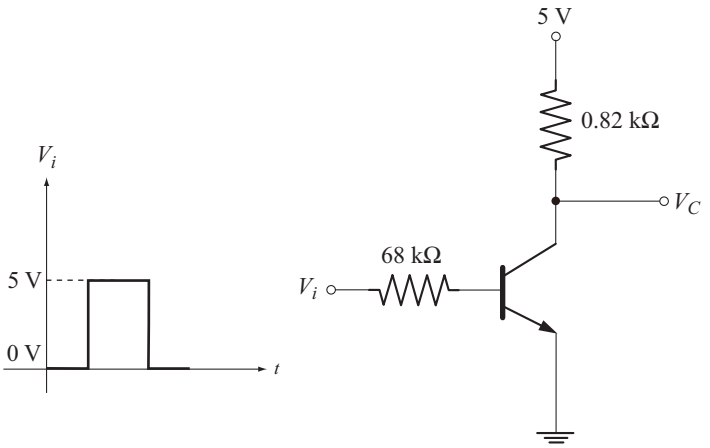
Observe that a high input voltage results in low output voltage and vice-versa. Hence the transistor switch is nothing but an inverter.

Example 2.35

Figure given below shows the transistor switch

(a) Check whether the circuit works properly
(b) Determine the output voltage levels at cut-off and saturation
(c) Calculate $R_{(\text{sat})}$ and $R_{(\text{cut-off})}$

Take $V_{BE} = 0.7$ V $\quad V_{CE(\text{sat})} = 0.15$ V
$I_{CEO} = 10\ \mu\text{A} \quad \beta_{dc} = h_{FE} = 125$



Solution

(a)
$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{5\text{ V} - 0.15\text{ V}}{0.82\text{ k}\Omega} = 5.91\text{ mA}$$

$$I_{B(\text{max})} = \frac{I_{C(\text{sat})}}{\beta_{dc}} = \frac{5.9\text{ mA}}{125} = 47.2\ \mu\text{A}$$

When $V_i = 5$V, the actual base current is

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = 63.23\text{mA}$$

Observe that, $I_B > I_{B(\text{max})}$. Hence the circuit works properly.

(b) When $V_i = 5$V

$$V_C = V_{CE(\text{sat})} = 0.15\text{ V}$$

When $V_i = 0$ V

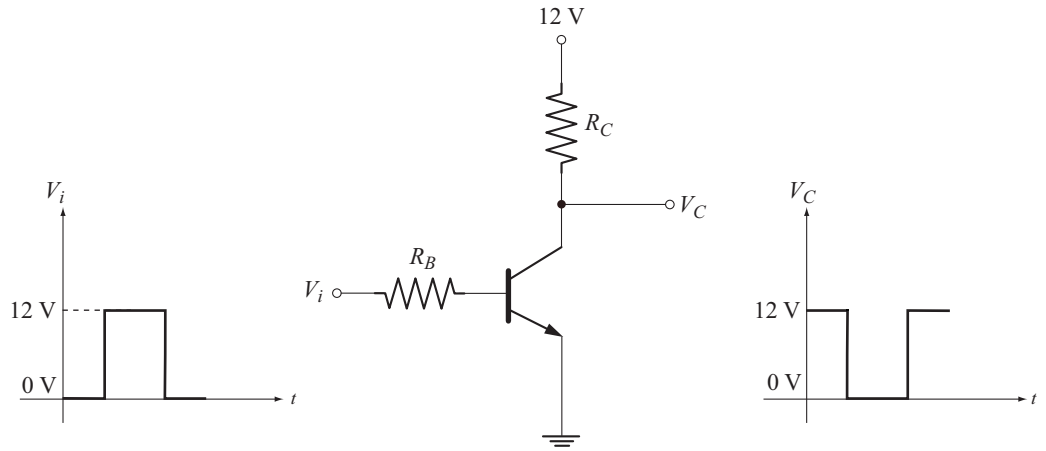
$$V_C = V_{CE(\text{cut-off})} = V_{CC} - I_{CEO}R_C$$
$$= 5\text{ V} - (10\ \mu\text{A})\ (0.82\text{ k}\Omega) \approx 5\text{ V}$$

(c)
$$R_{(\text{sat})} = \frac{V_{CE(\text{sat})}}{I_{C(\text{sat})}} = \frac{0.15\text{ V}}{5.9\text{ mA}} = 25.42\ \Omega\text{ (low)}$$

$$R_{(\text{cut-off})} = \frac{V_{CE(\text{cut-off})}}{I_{CEO}} = \frac{5\text{ V}}{10\ \mu\text{A}} = 500\text{ k}\Omega\text{ (very high)}$$

Example 2.36

For the transistor inverter shown below, determine the values of R_B and R_C. Take $I_{C\,(\text{sat})} = 12$ mA and $h_{FE} = 200$.



Solution

Calculation of R_C

$$I_{C\,(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C}$$

From the output waveform, $V_{CE\,(\text{sat})} = 0$ V

$$\therefore \quad R_C = \frac{V_{CC}}{I_{C(\text{sat})}} = \frac{12\text{ V}}{12\text{ mA}} = 1\text{ k}\Omega$$

Calculation of R_B

$$I_{B(\max)} = \frac{I_{C(\text{sat})}}{\beta_{\text{dc}}} = \frac{12\text{ mA}}{200} = 60\ \mu\text{A}$$

Let I_B = 150 % of $I_{B(\max)}$ [To ensure saturation]

$= (1.5)\ (60\ \mu\text{A}) = 90\ \mu\text{A}$

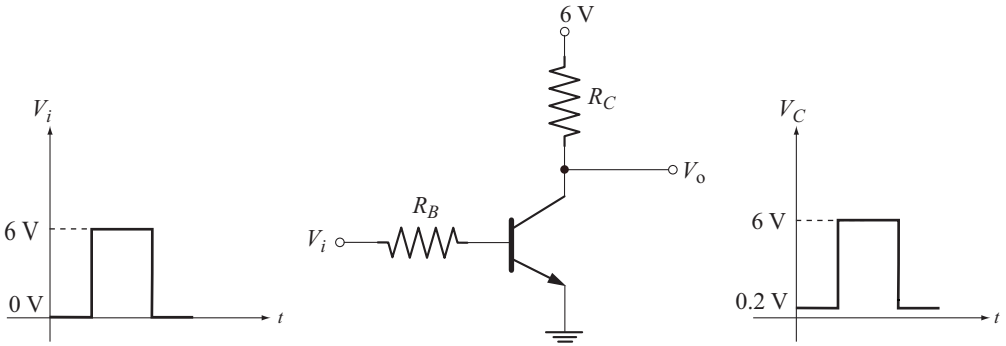
$$R_B = \frac{V_i - V_{BE}}{I_B}$$

$$= \frac{12\text{ V} - 0.7\text{ V}}{90\ \mu\text{A}}$$

$$= 125.55\text{ k}\Omega$$

Example 2.37

Design the transistor inverter shown below with a saturation current of 10 mA. Take I_B equal to 120 % of $I_{B(\max)}$. For the transistor used $\beta_{dc} = 100$ and $V_{BE} = 0.7$ V.



Solution

Calculation of R_C

$$I_{C\,(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C}$$

From the output voltage waveform, $V_{CE(\text{sat})} = 0.2$ V

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C(\text{sat})}} = \frac{6\text{ V} - 0.2\text{ V}}{10\text{ mA}} = 580\ \Omega$$

Calculation of R_B

$$I_{B(\max)} = \frac{I_{C(\text{sat})}}{\beta_{\text{dc}}} = \frac{10\text{ mA}}{100} = 100\ \mu\text{A}$$

Given

$$I_B = 120\ \%\ \text{of}\ I_{B(\max)}$$
$$= (1.2)\,(100\ \mu\text{A}) = 120\ \mu\text{A}$$
$$R_B = \frac{V_i - V_{BE}}{I_B} = \frac{6\text{ V} - 0.7\text{ V}}{120\ \mu\text{A}} = 44.16\ \text{k}\Omega$$

Example 2.38

For the transistor switch shown below

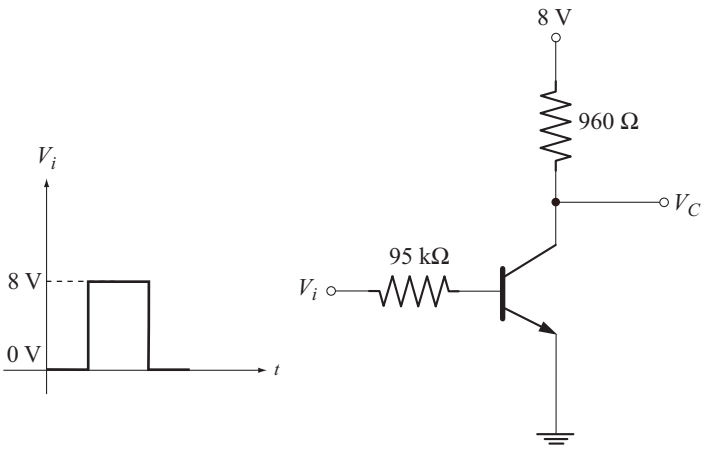
$V_{BE} = 0.7$ V, $V_{CE\,(\text{sat})} = 0.3$V, $I_{CEO} = 5\ \mu$A and $h_{FE} = 125$

(a) Calculate $I_{C\,(\text{sat})}$ and $I_{B\,(\max)}$

(b) Find I_B and check whether the transistor goes to saturation when $V_i = 8$ V

(c) Determine $R_{(\text{sat})}$ and $R_{(\text{cut-off})}$

(d) Sketch the output voltage waveform.



Solution

(a) $I_{C\,(\text{sat})}$ and $I_{B\,(\text{max})}$

$$I_{C\,(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{8\text{ V} - 0.3\text{ V}}{960\ \Omega} = 8.02\text{ mA}$$

$$I_{B\,(\text{max})} = \frac{I_{C(\text{sat})}}{\beta_{\text{dc}}} = \frac{8.02\text{ mA}}{125} = 64.16\ \mu\text{A}$$

(b) I_B when $V_i = 8$ V

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{8\text{ V} - 0.7\text{ V}}{95\text{ k}\Omega} = 76.84\ \mu\text{A}$$

Since $I_B > I_{B\,(\text{max})}$, the transistor definitely goes to saturation when $V_i = 8$ V.

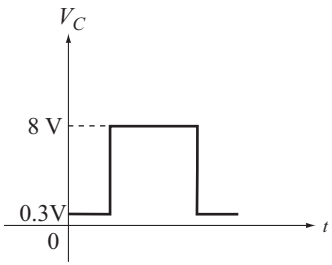
(c) $R_{(\text{sat})}$ and $R_{(\text{cut-off})}$

$$R_{(\text{sat})} = \frac{V_{CE(\text{sat})}}{I_{C(\text{sat})}} = \frac{0.3\text{ V}}{8.02\text{ mA}} = 37.4\ \Omega$$

$$R_{(\text{cut-off})} = \frac{V_{CE(\text{cut-off})}}{I_{CEO}} = \frac{8\text{ V}}{5\ \mu\text{A}} = 1.6\ \text{M}\Omega$$

(d) ***Output Voltage***

The output voltage switches between $V_{CE(\text{sat})}$ and V_{CC} as shown below.



2.13 TRANSISTOR SWITCHING TIMES

Transistors which are designed to operate at high speed between cut-off and saturation are called switching transistors. Figure 2.25 shows the timing characteristics of switching transistor.

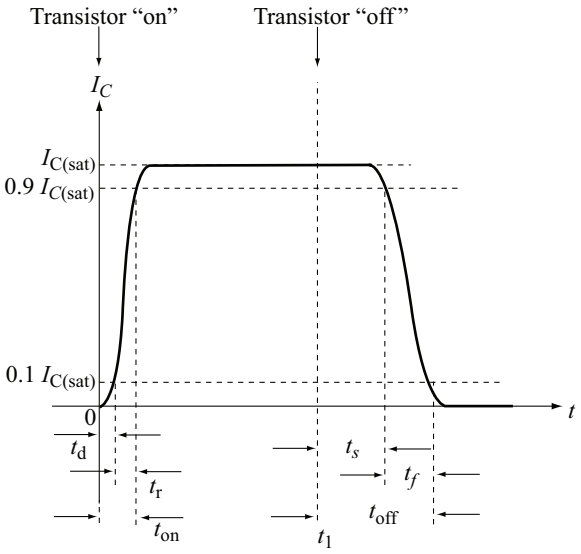


Fig. 2.25 Transistor switching times

At $t = 0$ the transistor switch is turned on by applying a high voltage at the input. The collector current does not rise immediately to $I_{C\,(sat)}$. Instead it takes a finite turn on time t_{on} to reach the steady state value of $I_{C\,(sat)}$.

$$t_{on} = t_d + t_r \tag{2.81}$$

t_d = delay time

t_r = rise time

Delay time is the time taken by the collector current to rise from zero to 10% of $I_{C\,(sat)}$.

Rise time is the time taken by the collector current to rise from 10% to 90% of $I_{C\,(sat)}$.

At $t = t_1$, the switch is turned off by reducing the input voltage to zero. The transistor does not turn-off immediately. Instead, it takes a finite time t_{off} to turn-off.

$$t_{off} = t_s + t_f \tag{2.82}$$

t_s = storage time

t_f = fall time

Due to stored charges in the base, the collector current remains at $I_{C\,(sat)}$ over the interval t_s and later it starts decreasing towards zero.

The time taken by the collector current to decrease from 90% to 10% of $I_{C(sat)}$ during turn-off is called the fall time.

Switching transistors are designed with small values of t_{on} and t_{off} in order to operate at higher speeds.

For general purpose transistor 2N4123 the following switching times are available on data sheet at $I_C = 10$ mA.

$$t_s = 120 \text{ ns}$$
$$t_d = 25 \text{ ns}$$
$$t_r = 13 \text{ ns}$$
$$t_f = 12 \text{ ns}$$
$$\therefore \quad t_{on} = t_r + t_d = 13 \text{ ns} + 25 \text{ ns} = 38 \text{ ns}$$
$$t_{off} = t_s + t_f = 120 \text{ ns} + 12 \text{ ns} = 132 \text{ ns}$$

where as for the switching transistor BSV52L the data sheet provides:

$$t_{on} = 12 \text{ ns} \quad \text{and} \quad t_{off} = 18 \text{ ns}$$

Note that switching transistors have very small values of t_{on} and t_{off}.

◆ 2.14 BIAS STABILISATION

The collector current in a transistor is sensitive to each of the following parameters

- I_{CO} doubles for every 10 ˚C rise in temperature.
- V_{BE} decreases about 2.5 mV per degree celcius increase in temperature
- β increases with increase in temperature

The three stability factors $S(I_{CO})$, $S(\beta)$ and $S(V_{BE})$ which have been already defined Section 2.4, indicates how I_C changes when I_{CO}, β and V_{BE} changes with temperature. Biasing networks should be designed with low stability factors inorder to obtain higher degree of stability of the operating point. Now let us study the bias stability of various bias configurations.

◆ 2.15 GENERAL EXPRESSION FOR STABILITY FACTOR $S(I_{CO})$

The expression for collector current in terms of β and I_{CO} is given by

$$I_C = (1 + \beta) I_{CO} + \beta I_B \tag{2.83}$$

The stability factors $S(I_{CO})$ is defined as

$$S(I_{CO}) = \left. \frac{\partial I_C}{\partial I_{CO}} \right|_{\beta, V_{BE} \text{ constant}} \tag{2.84}$$

Differentiating Equation (2.83) partially with respect to I_C, treating β constant, we get

$$1 = (1 + \beta) \frac{\partial I_{CO}}{\partial I_C} + \beta \frac{\partial I_B}{\partial I_C}$$

$$(1+\beta)\frac{\partial I_{CO}}{\partial I_C} = 1-\beta\frac{\partial I_B}{\partial I_C}$$

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}} \tag{2.85}$$

Stability factor $S(I_{CO})$ against variation in I_{CO} for any configuration can be found by computing $\dfrac{\partial I_B}{\partial I_C}$.

Recall that, lower the stability factors, the lower is the variation of I_C with respect to I_{CO}, β and V_{BE}. An observation of Equation (2.85) shows that for $S(I_{CO})$ to be small

$$1-\beta\frac{\partial I_B}{\partial I_C} \gg 1+\beta$$

or

$$\frac{\partial I_B}{\partial I_C} \ll -1 \Rightarrow \left|\frac{\partial I_B}{\partial I_C}\right| \gg 1$$

This implies that the variation of $\dfrac{\partial I_B}{\partial I_C}$ must be negative as well as substantial.

An increase in collector current due to any reason should result in a decrease in the base current.

◆ 2.16 STABILITY FACTORS FOR FIXED-BIAS CIRCUIT

The three stability factors to be determined are $S(I_{CO})$, S(V_{BE}) and $S(\beta)$. Other nomenclatures for these stability factors are shown in Table 2.3.

Table 2.3 Other nomenclatures for stability factors

Stability factors		
$S(I_{CO})$	$S(V_{BE})$	$S(\beta)$
S	S'	S''
$S_{I_{CO}}$	$S_{V_{BE}}$	S_β

Stability Factor $S(I_{CO})$

$$S(I_{CO}) \equiv \frac{\partial I_C}{\partial I_{CO}} \tag{2.86}$$

From Equation (2.9)

$$I_B = \frac{V_{CC}-V_{BE}}{R_B}$$

But $V_{CC} \gg V_{BE}$

$\therefore$ $I_B \simeq \dfrac{V_{CC}}{R_B}$ which is constant

The analysis of the fixed-bias circuit can be found in Section 2.5.
Differentiating with respect to I_C,

$$\frac{\partial I_B}{\partial I_C} = 0$$

Substituting in Equation (2.85)

$$S(I_{CO}) = 1 + \beta \tag{2.87}$$

$S(I_{CO})$ is very large because β is usually very large, say, typically that $\beta = 100$ for a transistor. Equation (2.87) implies that $S(I_{CO}) = 101$. This means that $\dfrac{\Delta I_C}{\Delta I_{CO}} = 101$ or $\Delta I_C = 101\ \Delta I_{CO}$. This implies that I_C changes by nearly hundred times the change in I_{CO}, indicating very poor stability of the operating point. This basically happens because in this configuration I_B is independent of I_C.

Stability Factor S(V_{BE})

$$S(V_{BE}) \equiv \frac{\partial I_C}{\partial V_{BE}} \tag{2.88}$$

From Equation (2.9)

$$V_{CC} = I_B R_B + V_{BE} \tag{2.89}$$

$\therefore$
$$V_{BE} = V_{CC} - I_B R_B \tag{2.90}$$

But $I_B \simeq \dfrac{I_C}{\beta}$

Substituting in Equation (2.90)

$$V_{BE} = V_{CC} - \frac{I_C}{\beta} R_B \tag{2.91}$$

Differentiating with respect to V_{BE}, keeping β constant, we get

$$1 = 0 - \frac{R_B}{\beta} \frac{\partial I_C}{\partial V_{BE}} \tag{2.92}$$

From Equation (2.88) and Equation (2.92)

$$S(V_{BE}) = -\frac{\beta}{R_B} \tag{2.93}$$

The negative sign implies that if V_{BE} decreases, due to, say an increase in temperature, I_C will increase. In order to minimize variation of I_C with V_{BE}, the ratio $\frac{\beta}{R_B}$ needs to be kept low either by the choice of a large R_B or by using transistor with small β.

Stability Factor S(β)

$$S(\beta) \equiv \frac{\partial I_C}{\partial \beta}$$

Since the variation of I_C with β cannot be obtained in analytical form, $S(\beta)$ is computed as

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} \tag{2.94}$$

From Equation (2.91)

$$I_C = \frac{\beta}{R_B} [V_{CC} - V_{BE}] \tag{2.95}$$

Let $I_C = I_{C_1}$ and $\beta = \beta_1$ at temperature T_1 and
$I_C = I_{C_2}$ and $\beta = \beta_2$ at temperature T_2

$$I_{C_1} = \frac{\beta_1}{R_B} (V_{CC} - V_{BE}) \tag{2.96}$$

$$I_{C_2} = \frac{\beta_2}{R_B} (V_{CC} - V_{BE}) \tag{2.97}$$

Dividing Equation (2.97) by Equation (2.96)

$$\frac{I_{C_2}}{I_{C_1}} = \frac{\beta_2}{\beta_1} \tag{2.98}$$

Subtracting 1 on both sides,

$$\frac{I_{C_2}}{I_{C_1}} - 1 = \frac{\beta_2}{\beta_1} - 1$$

$$\frac{I_{C_2} - I_{C_1}}{I_{C_1}} = \frac{\beta_2 - \beta_1}{\beta_1}$$

$$\frac{\Delta I_C}{I_{C_1}} = \frac{\Delta \beta}{\beta_1}$$

$$\therefore \quad S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}}{\beta_1} \tag{2.99}$$

From Equation (2.99) it is clear that to keep $S(\beta)$ low, the β of the transistor must be large. This is in contrast to $S(I_{CO})$ and $S(V_{BE})$ which require small values of β to remain low.

◆ 2.17 STABILITY FACTORS FOR EMITTER-BIAS CIRCUIT

Let us now obtain expression $S(I_{CO})$, $S(V_{BE})$ and $S(\beta)$ for the emitter-bias circuit.

Stability Factor $S(I_{CO})$

Refer Fig 2.11

From Equation (2.85), we have

$$S(I_{CO}) = \frac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}} \tag{2.100}$$

From Equation (2.15)

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

But $$I_E = I_B + I_C$$

$\therefore$ $$V_{CC} = I_B R_B + V_{BE} + I_B R_E + I_C R_E \tag{2.101}$$

Differentiating Equation (2.101) with respect to I_C keeping V_{BE} constant, we get

$$0 = \frac{\partial I_B}{\partial I_C} R_B + \frac{\partial I_B}{\partial I_C} R_E + R_E = \frac{\partial I_B}{\partial I_C}(R_B + R_E) + R_E$$

$\therefore$ $$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_B + R_E} \tag{2.102}$$

Substituting Equation (2.102) in Equation (2.100)

$$S(I_{CO}) = \frac{1+\beta}{1-\beta\left(\dfrac{-R_E}{R_B+R_E}\right)} = \frac{1+\beta}{1+\beta\left(\dfrac{R_E}{R_B+R_E}\right)}$$

$$= \frac{(\beta+1)(R_E+R_B)}{R_B+R_E+\beta R_E} = \frac{(\beta+1)(R_E+R_B)}{(\beta+1)R_E+R_B}$$

$\therefore$ $$S(I_{CO}) = \frac{(\beta+1)\left(1+\dfrac{R_B}{R_E}\right)}{(\beta+1)+\dfrac{R_B}{R_E}} \tag{2.103}$$

Design Considerations

If $$\frac{R_B}{R_E} \ll (1+\beta)$$

or $$(1+\beta)\,R_E \gg R_B$$

From Equation (2.103), we get

$$S(I_{CO}) \approx 1 + \frac{(1+\beta)\left[1+\frac{R_B}{R_E}\right]}{(1+\beta)}$$

or $$S(I_{CO}) \approx 1 + \frac{R_B}{R_E}$$

The smallest achievable value of $S(I_{CO})$ is therefore 1 under the condition $\frac{R_B}{R_E} \ll 1$.

Variation of $S(I_{CO})$ of emitter bias circuit with $\frac{R_B}{R_E}$

For $\frac{R_B}{R_E} \ll 1$, $S(I_{CO}) \approx 1$ as shown in the previous section.

For $\frac{R_B}{R_E} > (1+\beta)$, from Equation (2.103) we have

$$S(I_{CO}) \approx \frac{(1+\beta)\left[1+\frac{R_B}{R_E}\right]}{\frac{R_B}{R_E}} \approx (1+\beta)$$

For $1 < \frac{R_B}{R_E} < (1+\beta)$ $\quad S(I_{CO}) \approx 1 + \frac{R_B}{R_E} \approx \frac{R_B}{R_E}$

Figure 2.26 shows the variation of $S(I_{CO})$ with $\frac{R_B}{R_E}$.

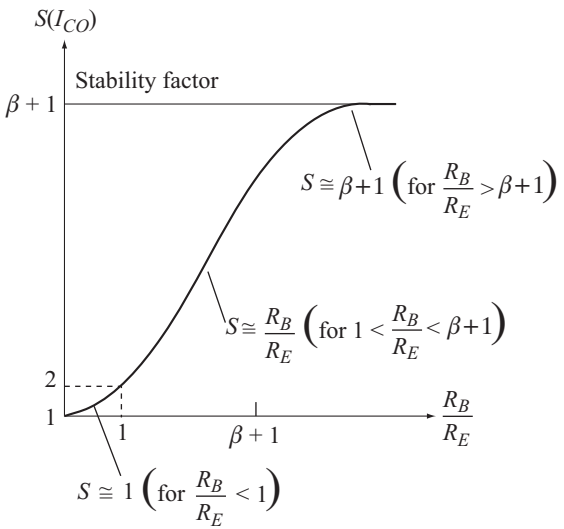


Fig. 2.26 Variation of $S(I_{CO})$ with $\frac{R_B}{R_E}$

(ii) Stability Factor S(V_{BE})

By definition

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}}$$

From Equation (2.101)

$$V_{CC} = I_B R_B + V_{BE} + I_B R_E + I_C R_E$$

Substuiting $I_B = \frac{I_C}{\beta}$

$$V_{CC} = \frac{I_C}{\beta} R_B + V_{BE} + \frac{I_C}{\beta} R_E + I_C R_E$$

$$= \left[\frac{R_B}{\beta} + \frac{R_E}{\beta} + R_E \right] I_C + V_{BE}$$

$$= \left[\frac{R_B + R_E + \beta R_E}{\beta} \right] I_C + V_{BE}$$

$$V_{CC} = \left[\frac{R_B + (1+\beta) R_E}{\beta} \right] I_C + V_{BE} \qquad (2.104)$$

Differentiating Equation (2.104) with respect to I_C, keeping β constant, we get

$$0 = \frac{R_B + (1+\beta) R_E}{\beta} + \frac{\partial V_{BE}}{\partial I_C}$$

$$\therefore \quad S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta) R_E} \qquad (2.105)$$

Design Considerations

If $(1+\beta) R_E \gg R_B$

From Equation (2.105) we have

$$S(V_{BE}) \approx \frac{-\beta}{(1+\beta) R_E}$$

For large β, $(1+\beta) \approx \beta$

$$S(V_{BE}) \approx \frac{-1}{R_E}$$

Note that $S(V_{BE})$ can be made small by increasing the value of R_E.

(iii) Stability Factor S(β)

By definition

$$S(\beta) = \frac{\partial I_C}{\partial \beta}$$

But to find $S(\beta)$ we use

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

From Equation (2.104)

$$V_{CC} = \left[\frac{R_B + (1+\beta)R_E}{\beta}\right] I_C + V_{BE}$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}\beta \tag{2.106}$$

Let $I_C = I_{C_1}$ and $\beta = \beta_1$ at temperature T_1 and $I_C = I_{C_2}$ and $\beta = \beta_2$ at temperature T_2. Substituting in Equation (2.106) we obtain

$$I_{C_1} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta_1)R_E}\beta_1 \tag{2.107}$$

$$I_{C_2} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta_2)R_E}\beta_2 \tag{2.108}$$

Dividing Equation (2.108) by Equation (2.107)

$$\frac{I_{C_2}}{I_{C_1}} = \frac{R_B + (\beta_1 + 1)R_E}{R_B + (\beta_2 + 1)R_E}\frac{\beta_2}{\beta_1}$$

$$\frac{I_{C_2}}{I_{C_1}} = \frac{1 + \beta_1 + \dfrac{R_B}{R_E}}{1 + \beta_2 + \dfrac{R_B}{R_E}}\frac{\beta_2}{\beta_1} \tag{2.109}$$

Subtracting 1 from both sides of Equation (2.109)

$$\frac{I_{C_2}}{I_{C_1}} - 1 = \frac{1 + \beta_1 + \dfrac{R_B}{R_E}}{1 + \beta_2 + \dfrac{R_B}{R_E}}\frac{\beta_2}{\beta_1} - 1$$

$$\frac{I_{C_2} - I_{C_1}}{I_{C_1}} = \frac{\left(1 + \beta_1 + \dfrac{R_B}{R_E}\right)\beta_2 - \left(1 + \beta_2 + \dfrac{R_B}{R_E}\right)\beta_1}{\beta_1\left(1 + \beta_2 + \dfrac{R_B}{R_E}\right)}$$

$$\therefore \quad \frac{\Delta I_C}{I_{C_1}} = \frac{\beta_2 + \beta_1\beta_2 + \dfrac{R_B}{R_E}\beta_2 - \beta_1 - \beta_1\beta_2 - \dfrac{R_B}{R_E}\beta_1}{\beta_1\left(1 + \beta_2 + \dfrac{R_B}{R_E}\right)}$$

$$\frac{\Delta I_C}{I_{C_1}} = \frac{(\beta_2 - \beta_1) + \frac{R_B}{R_E}(\beta_2 - \beta_1)}{\beta_1\left(1 + \beta_2 + \frac{R_B}{R_E}\right)} = \frac{(\beta_2 - \beta_1)\left(1 + \frac{R_B}{R_E}\right)}{\beta_1\left(1 + \beta_2 + \frac{R_B}{R_E}\right)}$$

$$\therefore \quad S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}\left(1 + \frac{R_B}{R_E}\right)}{\beta_1\left(1 + \beta_2 + \frac{R_B}{R_E}\right)} \tag{2.110}$$

Design Considerations

$$(1 + \beta_2) \approx \beta_2$$

From Equation (2.110) we have

$$S(\beta) \approx \frac{I_{C_1}\left[1 + \frac{R_B}{R_E}\right]}{\beta_1\left[\beta_2 + \frac{R_B}{R_E}\right]} \approx \frac{I_{C_1}\left[1 + \frac{R_B}{R_E}\right]}{\beta_1\beta_2\left[1 + \frac{R_B}{\beta_2 R_E}\right]}$$

For large β, $\frac{R_B}{\beta_2 R_E} \ll 1$

$$\therefore \quad 1 + \frac{R_B}{\beta_2 R_E} \approx 1$$

$$\therefore \quad S(\beta) \approx \frac{I_{C_1}}{\beta_1\beta_2}\left[1 + \frac{R_B}{R_E}\right] = \frac{I_{C_1}}{\beta_1\beta_2} S(I_{CO})$$

Thus $S(\beta)$ can be minimized by selecting a transistor with large β as well as by keeping $\frac{R_B}{R_E} \ll 1$.

◆ 2.18 STABILITY FACTORS FOR VOLTAGE DIVIDER BIAS CIRCUIT

Let us proceed on the same lines as in the case of other configurations.

Refer Fig. 2.16.

(i) ***Stability Factor S(I_{CO})***

$$S(I_{CO}) = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

From Equation (2.29)

$$V_{Th} = R_{Th} I_B + V_{BE} + I_E R_E$$

But
$$I_E = I_C + I_B$$
$$V_{Th} = R_{Th} I_B + V_{BE} + I_C R_E + I_B R_E \quad (2.111)$$

Differentiating the above equation partially with respect to I_C, keeping V_{BE} constant, we get

$$0 = (R_E + R_{Th}) \frac{\partial I_B}{\partial I_C} + R_E$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_{Th}}$$

Substituting in the expression for $S(I_{CO})$, we get

$$S(I_{CO}) = \frac{1+\beta}{1+\beta \dfrac{R_E}{R_E + R_{Th}}} = \frac{1+\beta}{R_E + R_{Th} + \beta R_E} (R_E + R_{Th})$$

$$\therefore \quad S(I_{CO}) = (\beta + 1) \frac{R_E + R_{Th}}{(\beta+1)R_E + R_{Th}} \quad (2.112)$$

$$\therefore \quad S(I_{CO}) = (\beta + 1) \frac{\left[1 + \dfrac{R_{Th}}{R_E}\right]}{(\beta+1) + \dfrac{R_{Th}}{R_E}} \quad (2.113)$$

Design Considerations

Consider the denominator of Equation (2.112). Generally $(\beta + 1) R_E \gg R_{Th}$

Hence,
$$S(I_{CO}) \simeq \frac{(\beta+1)(R_E + R_{Th})}{(\beta+1)R_E} = 1 + \frac{R_{Th}}{R_E}$$

The smallest achievable value of $S(I_{CO})$ is therefore 1 under the condition $R_{Th} \ll R_E$.

(ii) Stability Factor $S(V_{BE})$

By definition

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}}$$

From Equation (2.111)

$$V_{Th} = R_{Th} I_B + V_{BE} + I_C R_E + I_B R_E$$

Substituting
$$I_B = \frac{I_C}{\beta}$$

$$\therefore \quad V_{Th} = \left(\frac{R_{Th}}{\beta} + \frac{R_E}{\beta} + R_E\right) I_C + V_{BE}$$

$$= \left(\frac{R_{Th} + R_E + \beta R_E}{\beta}\right) I_C + V_{BE}$$

$$V_{Th} = \left(\frac{\left(R_{Th} + (\beta+1)R_E\right)}{\beta}\right) I_C + V_{BE} \tag{2.114}$$

Differentiating partially with respect to V_{BE}, keeping β constant

$$0 = \frac{R_{Th} + (\beta+1)R_E}{\beta} \frac{\partial I_C}{\partial V_{BE}} + 1$$

$$\therefore \quad S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_{Th} + (\beta+1)R_E} \tag{2.115}$$

Design Considerations

Again from Equation (2.115)

If $(\beta + 1)\ R_E \gg R_{Th}$,

$$S(V_{BE}) \simeq \frac{-\beta}{(\beta+1)R_E}$$

For large β, $\beta + 1 \simeq \beta$

$$\therefore \quad S(V_{BE}) = -\frac{1}{R_E}$$

Thus, $S(V_{BE})$ can be made small by increasing the value of emitter resistance R_E.

(iii) Stability Factor S(β)

By definition

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

From Equation (2.114)

$$V_{th} = \left(\frac{R_{Th} + (\beta+1)R_E}{\beta}\right) I_C + V_{BE}$$

$$\therefore \quad \left(\frac{R_{Th} + (\beta+1)R_E}{\beta}\right) I_C = V_{th} - V_{BE}$$

$$I_C = \frac{(V_{Th} - V_{BE})\beta}{R_{Th} + (1+\beta)R_E}$$

Let $I_C = I_{C_1}$ and $\beta = \beta_1$ at temperature T_1 and
Let $I_C = I_{C_2}$ and $\beta = \beta_2$ at temperature T_2

$$\therefore \quad I_{C_1} = \frac{(V_{Th} - V_{BE})\beta_1}{R_{Th} + (1+\beta_1)R_E} \tag{2.116}$$

$$\text{and} \quad I_{C_2} = \frac{(V_{Th} - V_{BE})\beta_2}{R_{Th} + (1+\beta_2)R_E} \tag{2.117}$$

Dividing Equation (2.117) by Equation (2.116)

$$\frac{I_{C_2}}{I_{C_1}} = \frac{R_{Th} + (1+\beta_1)R_E}{R_{Th} + (1+\beta_2)R_E} \cdot \frac{\beta_2}{\beta_1} \tag{2.118}$$

Subtracting 1 from both sides of Equation (2.118)

$$\frac{I_{C_2}}{I_{C_1}} - 1 = \frac{R_{Th} + (1+\beta_1)R_E}{R_{Th} + (1+\beta_2)R_E} \cdot \frac{\beta_2}{\beta_1} - 1$$

$$\frac{\Delta I_C}{I_{C_1}} = \frac{\left[R_{Th} + (1+\beta_1)R_E\right]\beta_2 - \left[R_{Th} + (1+\beta_2)R_E\right]\beta_1}{\left[R_{Th} + (1+\beta_2)R_E\right]\beta_1}$$

$$= \frac{R_{Th}\beta_2 + \beta_2 R_E + \beta_1\beta_2 R_E - R_{Th}\beta_1 - \beta_1 R_E - \beta_1\beta_2 R_E}{\left[R_{Th} + (1+\beta_2)R_E\right]\beta_1}$$

$$= \frac{R_{Th}(\beta_2 - \beta_1) + R_E(\beta_2 - \beta_1)}{\left[R_{Th} + (1+\beta_2)R_E\right]\beta_1}$$

$$\therefore \quad \frac{\Delta I_C}{\Delta\beta} = \frac{I_{C_1}}{\beta_1}\,\frac{R_{Th} + R_E}{R_{Th} + (1+\beta_2)R_E} \tag{2.119}$$

$$\therefore \quad S(\beta) = \frac{\Delta I_C}{\Delta\beta} = \frac{I_{C_1}\left(1 + \dfrac{R_{Th}}{R_E}\right)}{\beta_1\left(1 + \beta_2 + \dfrac{R_{Th}}{R_E}\right)} \tag{2.120}$$

Design Considerations

From Equation (2.120)

$$S(\beta) = \frac{I_{C_1}\left(1 + \dfrac{R_{Th}}{R_E}\right)}{\beta_1(\beta_2+1)\left(1 + \dfrac{R_{Th}}{(\beta_2+1)R_E}\right)}$$

Now $\beta_2 + 1 \simeq \beta_2$

$$\therefore \quad S(\beta) = \frac{I_{C_1}\left(1+\frac{R_{Th}}{R_E}\right)}{\beta_1\beta_2\left(1+\frac{R_{Th}}{\beta_2 R_E}\right)} \tag{2.121}$$

For large β $\quad \frac{R_{Th}}{\beta_2 R_E} \ll 1$

$$\therefore \quad 1+\frac{R_{Th}}{\beta_2 R_E} \simeq 1$$

From Equation (2.121)

$$\therefore \quad S(\beta) = \frac{I_{C_1}}{\beta_1\beta_2}\left(1+\frac{R_{Th}}{R_E}\right) = \frac{I_{C_1}}{\beta_1\beta_2} S(I_{CO})$$

Thus, $S(\beta)$ can be minimized by selecting a transistor with large β as well as by keeping $\frac{R_{Th}}{R_E} \ll 1$.

◆ 2.19 STABILITY FACTORS FOR COLLECTOR FEEDBACK BIAS CIRCUIT

Let us proceed on the same lines as in the case of other configurations. Refer Fig. 2.19.

(i) Stability factor $S(I_{CO})$

$$S(I_{CO}) = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_B}}$$

From Equation (2.47)

$$\begin{aligned} V_{CC} &= (I_C + I_B) R_C + I_B R_B + V_{BE} + I_E R_E \\ &= (I_C + I_B) R_C + I_B R_B + V_{BE} + (I_B + I_C) R_E \\ V_{CC} &= (R_C + R_E) I_C + (R_C + R_E + R_B) I_B + V_{BE} \end{aligned} \tag{2.122}$$

Differentiating Equation (2.122) partially with respect to I_C,

$$0 = (R_C + R_E) + (R_C + R_E + R_B)\frac{\partial I_B}{\partial I_C}$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C} = -\frac{R_C + R_E}{R_C + R_E + R_B}$$

Now $$S(I_{CO}) = -\frac{1+\beta}{1-\beta\left(\frac{-(R_C+R_E)}{R_C+R_E+R_B}\right)}$$

$$S(I_{CO}) = \frac{(\beta+1)(R_C + R_E + R_B)}{R_B + (1+\beta)(R_C + R_E)} \tag{2.123}$$

$$\therefore \quad S(I_{CO}) = \frac{(\beta+1)\left(1 + \frac{R_B}{R_C + R_E}\right)}{(1+\beta) + \frac{R_B}{R_C + R_E}} \tag{2.124}$$

(ii) Stability Factor S(V_{BE})

By definition $S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}}$

From Equation (2.122)

$$V_{CC} = (R_C + R_E) I_C + (R_C + R_E + R_B) I_B + V_{BE}$$

$$V_{CC} = (R_C + R_E) I_C + (R_C + R_E + R_B) \frac{I_C}{\beta} + V_{BE} \tag{2.125}$$

Differentiating Equation (2.125) partially with respect to I_C

$$0 = (R_C + R_E) + \frac{(R_C + R_E + R_B)}{\beta} + \frac{\partial V_{BE}}{\partial I_C}$$

$$0 = \frac{\beta(R_C + R_E) + (R_C + R_E + R_B)}{\beta} + \frac{\partial V_{BE}}{\partial I_C}$$

$$\therefore \quad S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{\beta(R_C + R_E) + (R_C + R_E + R_B)}$$

$$S(V_{BE}) = \frac{-\beta}{(\beta+1)(R_C + R_E) + R_B} \tag{2.126}$$

(ii) Stability Factor S(β)

By definition $S(\beta) = \frac{\Delta I_C}{\Delta \beta}$

From Equation (2.125)

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (1+\beta)(R_C + R_E)}$$

Let $I_C = I_{C_1}$ and $\beta = \beta_1$ at temperature T_1 and
$I_C = I_{C_2}$ and $\beta = \beta_2$ at temperature T_2

$$\therefore \quad I_{C_1} = \frac{\beta_1(V_{CC} - V_{BE})}{R_B + (1+\beta_1)(R_C + R_E)} \tag{2.127}$$

$$I_{C_2} = \frac{\beta_2 (V_{CC} - V_{BE})}{R_B + (1+\beta_2)(R_C + R_E)} \tag{2.128}$$

Dividing Equation (2.128) by Equation (2.127), we get

$$\frac{I_{C_2}}{I_{C_1}} = \frac{R_B + (1+\beta_1)(R_C + R_E)}{R_B + (1+\beta_2)(R_C + R_E)} \cdot \frac{\beta_2}{\beta_1} \tag{2.129}$$

Subtracting 1 from both sides of Equation (2.129)

$$\frac{I_{C_2}}{I_{C_1}} - 1 = \frac{R_B + (1+\beta_1)(R_C + R_E)}{R_B + (1+\beta_2)(R_C + R_E)} \cdot \frac{\beta_2}{\beta_1} - 1$$

$$\frac{\Delta I_C}{I_{C_1}} = \frac{\left[R_B + (1+\beta_1)(R_C + R_E)\right]\beta_2 - \left[R_B + (1+\beta_2)(R_C + R_E)\right]\beta_1}{\left[R_B + (1+\beta_2)(R_C + R_E)\right]\beta_1}$$

$$= \frac{R_B\beta_2 + (1+\beta_1)\beta_2(R_C + R_E) - R_B\beta_1 + \beta_1(1+\beta_2)(R_C + R_E)}{\left[R_B + (1+\beta_2)(R_C + R_E)\right]\beta_1}$$

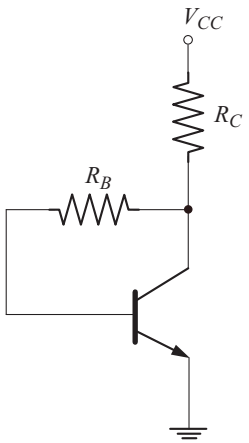
$$= \frac{R_B(\beta_2 - \beta_1) + (R_C + R_E)(\beta_2 - \beta_1)}{\left[R_B + (1+\beta_2)(R_C + R_E)\right]\beta_1}$$

$$\frac{\Delta I_C}{I_{C_1}} = \frac{\left[R_B + (R_C + R_E)\right](\beta_2 - \beta_1)}{\left[R_B + (1+\beta_2)(R_C + R_E)\right]\beta_1}$$

$$\therefore \quad S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C1}\left[R_B + (R_C + R_E)\right]}{\beta_1\left[R_B + (1+\beta_2)(R_C + R_E)\right]} \tag{2.130}$$

Example 2.39

For the circuit shown below derive the expressions for $S(I_{CO})$, $S(V_{BE})$ and $S(\beta)$.



Solution

The given circuit is nothing but the collector feedback configuration with $R_E = 0\ \Omega$.

The required results can be obtained by substituting $R_E = 0\ \Omega$ in the results of section 2.19.

From Equation (2.124)

$$S(I_{CO}) = \frac{(1+\beta)\left[1+\frac{R_B}{R_C}\right]}{(1+\beta)+\frac{R_B}{R_C}}$$

From Equation (2.126)

$$S(V_{BE}) = \frac{-\beta}{R_B+(1+\beta)R_C}$$

From Equation (2.130)

$$S(\beta) = \frac{I_{C_1}[R_B+R_C]}{\beta_1[R_B+(1+\beta_2)R_C]}$$

Example 2.40

Calculate the stability factor $S(I_{CO})$ and the change in I_C from 25° C to 100° C for the transistor which has $I_{CO}(25°\text{ C}) = 0.1$ nA and $I_{CO}(100°\text{ C}) = 20$ nA, for the following emitter bias arrangements. Take $\beta = 50$.

(a) $\frac{R_B}{R_E} = 100$ (b) $\frac{R_B}{R_E} = 0.1$

Also calculate I_{CQ} at 100° C for each case if I_{CQ} at 25° C is 2 mA.

Solution

For the emitter bias configuration

$$S(I_{CO}) = (1+\beta)\frac{1+\frac{R_B}{R_E}}{(1+\beta)+\frac{R_B}{R_E}}$$

(a) $\frac{R_B}{R_E} = 100$

$$S(I_{CO}) = \frac{(51)(1+100)}{51+100} = 34.11$$

$$\Delta I_C = S(I_{CO})\,\Delta I_{CO}$$

$$\Delta I_{CO} = I_{CO}(100°\text{ C}) - I_{CO}(25°\text{ C})$$

$$= 20\text{ nA} - 0.1\text{ nA} = 19.9\text{ nA}$$

$$\begin{aligned}\Delta I_C &= (34.11)\,(19.9\text{ nA})\\ &= 0.67\ \mu\text{A}\\ I_{C_2} &= I_{CQ} \text{ at } 100^\circ \text{ C}\\ I_{C_1} &= I_{CQ} \text{ at } 25^\circ \text{ C} = 2\text{ mA}\\ I_{C_2} &= I_{C_1} + \Delta I_C\\ &= 2\text{ mA} + 0.67\ \mu\text{A}\\ &\approx 2\text{ mA}\end{aligned}$$

(b) $\dfrac{R_B}{R_E} = 0.1$

$$\begin{aligned}S(I_{CO}) &= \frac{(51)(1.1)}{51+0.1} = 1.09\\ \Delta I_C &= S(I_{CO})\,\Delta I_{CO}\\ &= (1.09)\,(19.9\text{ nA}) = 21.69\text{ nA}\\ I_{C_2} &= I_{C_1} + \Delta I_C\\ &= 2\text{ mA} + 21.69\text{ nA}\\ &\approx 2\text{ mA}\end{aligned}$$

Observe that changes I_C is minimal when $\dfrac{R_B}{R_E} \ll 1$.

Example 2.41

Determine the stability factor $S(V_{BE})$ and the change in I_C from 25° C to 100° C for the transistor with V_{BE} (25° C) = 0.65 V and V_{BE} (100° C) = 0.48 V for the following bias arrangements

(a) Fixed bias with $R_B = 270\ \text{k}\Omega$ and $\beta = 120$.

(b) Emitter bias with $R_B = 39\ \text{k}\Omega$, $R_E = 1.2\ \text{k}\Omega$ and $\beta = 120$.

(c) Voltage divider bias with $R_1 = 39\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_E = 1\ \text{k}\Omega$ and $\beta = 120$.

Solution

$$\begin{aligned}\Delta V_{BE} &= V_{BE}(100^\circ\text{ C}) - V_{BE}(25^\circ\text{ C})\\ &= 0.48\text{ V} - 0.65\text{ V} = -0.17\text{ V}\end{aligned}$$

(a) ***Fixed Bias***

$R_B = 270\ \text{k}\Omega \quad \beta = 120$

$$\begin{aligned}S(V_{BE}) &= \frac{-\beta}{R_B} = -\frac{120}{270\text{ kW}} = -0.44 \times 10^{-3}\\ \Delta I_C &= S(V_{BE})\,\Delta V_{BE}\\ &= (-0.44 \times 10^{-3})\,(-0.17) = 74.8\ \mu\text{A}\end{aligned}$$

(b) ***Emitter Bias***

$R_B = 39\ \text{k}\Omega \quad R_E = 1.2\ \text{k}\Omega \quad \beta = 120.$

$$S(V_{BE}) = \frac{-\beta}{R_B + (1+\beta)R_E}$$

$$= \frac{-120}{39\ \text{kW} + (121)(1.2\ \text{kW})} = -0.65 \times 10^{-3}$$

$$\Delta I_C = S(V_{BE})\,\Delta V_{BE} = (-0.65 \times 10^{-3})\,(-0.17) = 110.5\ \mu\text{A}$$

(c) ***Voltage Divider Bias***

$R_1 = 39\ \text{k}\Omega \quad R_2 = 10\ \text{k}\Omega \quad R_E = 1\text{k}\Omega \quad \beta = 120$

$$S(V_{BE}) = \frac{-\beta}{R_{Th} + (1+\beta)R_E}$$

$$R_{th} = R_1 \,||\, R_2 = 39\ \text{k}\Omega \,||\, 10\ \text{k}\Omega = 7.95\ \text{k}\Omega$$

$$S(V_{BE}) = \frac{-120}{7.95\ \text{k}\Omega + (121)(1\ \text{k}\Omega)} = -0.93 \times 10^{-3}$$

$$\Delta I_C = S(V_{BE})\,\Delta V_{BE} = (-0.93 \times 10^{-3})\,(-0.17) = 158.1\ \mu\text{A}$$

Example 2.42

Determine the stability factor $S(\beta)$ and the change in I_C from 25° C to 100° C for the transistor with β (25° C) = 50 and β (100° C) = 100 for the following bias arrangement.

(a) Fixed bias with $R_B = 330\ \text{k}\Omega$

(b) Emitter bias with $\frac{R_B}{R_E} = 5$

(c) Voltage divider bias with $\frac{R_{Th}}{R_E} = 1.5$.

Also calculate I_{CQ} at the 100° C in each case if I_{CQ} at 25° C is 3 mA.

Solution

$$\beta_1 = \beta\ (25°\ \text{C}) = 50$$

$$\beta_2 = \beta\ (100°\text{C}) = 100$$

$$\Delta\beta = \beta_2 - \beta_1 = 50$$

$$I_{C_1} = I_{CQ}\ (25°\ \text{C}) = 3\ \text{mA}$$

$$I_{C_2} = I_{CQ}\ (100°\ \text{C})$$

(a) ***Fixed bias***

$$S(\beta) = \frac{I_{C_1}}{\beta_1} = \frac{3 \times 10^{-3}}{50} = 0.06 \times 10^{-3}$$

$$\Delta I_C = S(\beta)\,\Delta\beta = (0.06 \times 10^{-3})\,(50) = 3 \text{ mA}$$
$$I_{C_2} = I_{C_1} + \Delta I_C = 3 \text{ mA} + 3 \text{ mA} = 6 \text{ mA}$$

Observe the doubling of I_C value when β is doubled.

(b) ***Emitter Bias***

$$\frac{R_B}{R_E} = 5$$

$$S(\beta) = \frac{I_{C_1}\left[1+\frac{R_B}{R_E}\right]}{\beta_1\left[1+\beta_2+\frac{R_B}{R_E}\right]} = \frac{(3 \text{ mA})[1+5]}{50[101+5]} = 3.39 \times 10^{-6}$$

$$\Delta I_C = S(\beta)\,\Delta\beta = (3.39 \times 10^{-6})\,(50) = 0.17 \text{ mA}$$
$$I_{C_2} = I_{C_1} + \Delta I_C = 3 \text{ mA} + 0.17 \text{ mA} = 3.17 \text{ mA}$$

(c) ***Voltage Divider Bias***

$$\frac{R_{Th}}{R_E} = 1.5$$

$$S(\beta) = \frac{I_{C_1}\left[1+\frac{R_{Th}}{R_E}\right]}{\beta_1\left[1+\beta_2+\frac{R_{Th}}{R_E}\right]} = \frac{(3 \text{ mA})[1+1.5]}{50[101+1.5]} = 1.46 \times 10^{-6}$$

$$\Delta I_C = S(\beta)\,\Delta\beta = (1.46 \times 10^{-6})\,(50) = 73\ \mu\text{A}$$
$$I_{C_2} = I_{C_1} + \Delta I_C = 3 \text{ mA} + 73\ \mu\text{A} = 3.07 \text{ mA}$$

Example 2.43

For a voltage divider bias circuit, the following values are given:

$R_1 = 62\ \text{k}\Omega$ $R_2 = 9.1\ \text{k}\Omega$ $R_C = 3.9\ \text{k}\Omega$ $R_E = 680\ \Omega$ $V_{BE} = 0.7$ V $\beta = 80$ $V_{CC} = 16$ V

Calculate

(a) $S(I_{CO})$

(b) $S(V_{BE})$

(c) $S(\beta)$ with $\beta(T_1) = 80$ and $\beta(T_2) = 25\%$ more than $\beta(T_1)$

(d) Net change in I_C if I_{CO} increases from 0.2 to 10 μA, V_{BE} drops from 0.7 to 0.5 V and β increases by 25%.

Solution

(a) $S(I_{CO})$

$$S(I_{CO}) = (\beta+1)\frac{R_E + R_{Th}}{(\beta+1)R_E + R_{Th}}$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{62\ \text{kW} \times 9.1\ \text{kW}}{62\ \text{kW} + 9.1\ \text{kW}} = 7.94\ \text{k}\Omega$$

$$\therefore \quad S(I_{CO}) = \frac{(80+1)(0.68\ \text{kW} + 7.94\ \text{kW})}{(80+1)(0.68\ \text{kW}) + 7.94\ \text{kW}} = 11.08$$

(b) $S(V_{BE})$

$$S(V_{BE}) = \frac{-\beta}{R_{Th} + (\beta+1) R_E}$$

$$= \frac{-80}{7.94 \times 10^3 + (80+1)680} = 1.27 \times 10^{-3}$$

(c) $S(\beta)$

$$S(\beta) = \frac{I_{C_1}\left(1 + \frac{R_{Th}}{R_E}\right)}{\beta_1\left(1 + \beta_2 + \frac{R_{Th}}{R_E}\right)}$$

$$I_{C_1} = \frac{(V_{Th} - V_{BE})\,\beta_1}{R_{Th} + (1+\beta_1) R_E}$$

$$V_{th} = V_{CC} \frac{R_2}{R_1 + R_2} = (16\ \text{V}) \frac{9.1\ \text{kW}}{62\ \text{kW} + 9.1\ \text{kW}} = 2.05\ \text{V}$$

$$I_{C_1} = \frac{(2.05\ \text{V} - 0.7\ \text{V}) \times 80}{7.94\ \text{k}\Omega + (1+80) 0.68\ \text{k}\Omega} = 1.71\ \text{mA}$$

$$\beta_2 = 25\%\ \text{more than}\ \beta_1 = 1.25 \times 80 = 100$$

$$S(\beta) = \frac{\left[1.71 \times 10^{-3}\right]\left[1 + \frac{7.94\ \text{k}\Omega}{0.68\ \text{k}\Omega}\right]}{80\left[1 + 100 + \frac{7.94\ \text{k}\Omega}{0.68\ \text{k}\Omega}\right]} = 2.41 \times 10^{-6}$$

(d) Net change in collector current, ΔI_C

$$\Delta I_C = S(I_{CO})\,\Delta I_{CO} + S(V_{BE})\,\Delta V_{BE} + S(\beta)\,\Delta\beta$$

$$\Delta I_{CO} = 10\ \mu\text{A} - 0.2\ \mu\text{A} = 9.8\ \mu\text{A}$$

$$\Delta V_{BE} = 0.5\ \text{V} - 0.7\ \text{V} = -0.2\ \text{V}$$

$$\Delta\beta = \beta_2 - \beta_1 = 100 - 80 = 20$$

$$\Delta I_C = [11.08]\,[9.8 \times 10^{-6}] + [-1.27 \times 10^{-3}]\,[-0.2] + [2.141 \times 10^{-6}]\,[20]$$

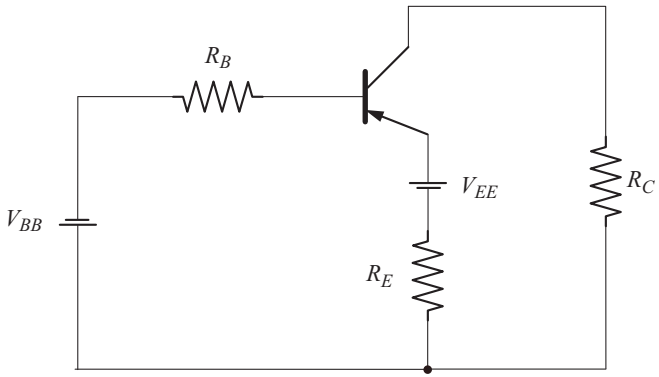
$$= 0.41 \text{ mA}$$

$$I_{C_2} = I_{C_1} + \Delta I_C = 1.71 \text{ mA} + 0.41 \text{ mA} = 2.12 \text{ mA}$$

Note: Similarly we can calculate the net change in collector current for the other biasing configurations.

Example 2.44

Find an expression for $S(I_{CO})$ for the circuit shown below.



Solution

The given circuit with actual current directions voltage polarities is redrawn in Fig. A.

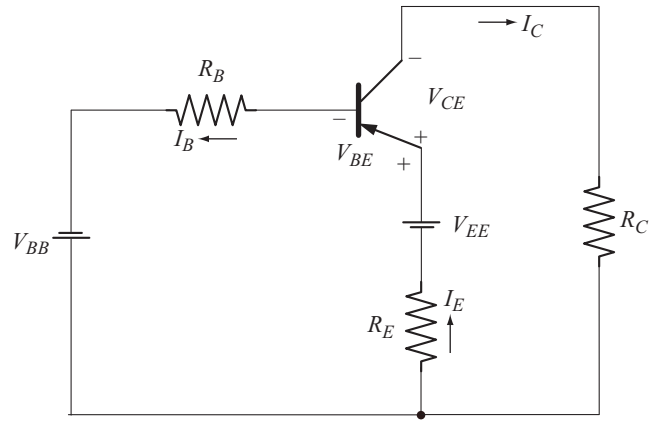


Fig. A

$$S(I_{CO}) = \frac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}}$$

Writing the KVL equation to the base-emitter circuit,

$$-V_{BB} + I_B R_B + V_{BE} - V_{EE} + I_E R_E = 0$$

$$\therefore \quad I_B R_B + I_E R_E = V_{BB} + V_{EE} - V_{BE}$$

$$\text{But} \quad I_E = I_B + I_C$$

$$\therefore \quad I_B(R_B + R_E) + I_C R_E = V_{BB} + V_{EE} - V_{BE}$$

Differentiating partially with respect to I_C

$$\frac{\partial I_B}{\partial I_C}(R_B + R_E) + R_E = 0$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{(R_B + R_E)}$$

$$\therefore \quad S(I_{CO}) = \frac{1+\beta}{1+\beta\left(\dfrac{R_E}{R_B + R_E}\right)}$$

$$S(I_{CO}) = \frac{1+\beta}{\dfrac{R_B + R_E + \beta R_E}{R_B + R_E}}$$

$$= \frac{(1+\beta)(R_B + R_E)}{R_B + (1+\beta)R_E}$$

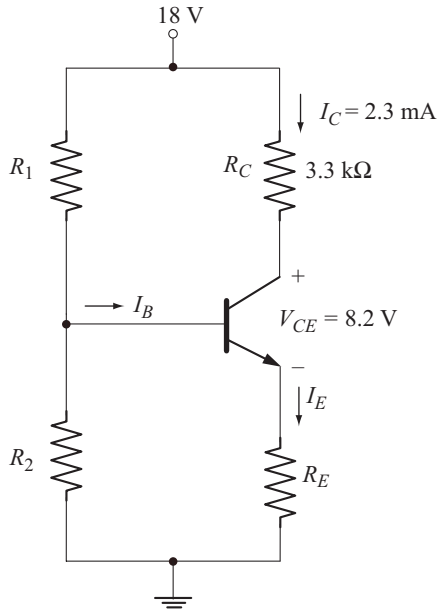
$$S(I_{CO}) = \frac{(1+\beta)\left(1 + \dfrac{R_B}{R_E}\right)}{(1+\beta) + \dfrac{R_B}{R_E}}$$

Example 2.45

Design a voltage divider bias circuit using a silicon transistor with V_{CC} = 18 V, I_C = 2.3 mA, V_{CE} = 8.2 V, R_C = 3.3 kΩ, β = 100 and $S(I_{CO}) \leq 5$.

Solution

The circuit is shown below.



Given $I_C = 2.3$ mA,

$$I_B = \frac{I_C}{\beta} = \frac{2.3 \text{ mA}}{100} = 0.023 \text{ mA}$$

$$I_E = I_B + I_C = 2.3 + 0.023 = 2.32 \text{ mA}$$

$$V_{BE} = 0.7 \text{ V} \quad \text{for a silicon transistor}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$\therefore \quad R_C + R_E = \frac{V_{CC} - V_{CE}}{I_C}$$

and

$$R_E = \frac{18 \text{ V} - 8.2 \text{ V}}{2.3 \text{ mA}} - 3.3 \text{ k}\Omega = 0.96 \text{ k}\Omega$$

$$S(I_{CO}) = (\beta + 1) \frac{R_E + R_{Th}}{(\beta + 1) R_E + R_{Th}}$$

$$S(I_{CO}) \leq 5 \text{ implies}$$

$$(\beta + 1) \frac{R_E + R_{Th}}{(\beta + 1) R_E + R_{Th}} \leq 5$$

$$(\beta + 1)(R_E + R_{Th}) \leq 5 [(\beta + 1) R_E + R_{Th}]$$

$$101 R_E + 101 R_{Th} \leq 505 R_E + 5 R_{Th}$$

$$96 R_{Th} \leq 404 R_E$$

$$R_{Th} \leq \frac{404}{96} R_E$$

$$R_{Th} \leq \frac{404}{96} \times 0.96\ \text{k}\Omega$$

$$R_{Th} \leq 4.04\ \text{k}\Omega$$

Let $R_{Th} = 4\ \text{k}\Omega$

$$V_{Th} = R_{Th} I_B + I_E R_E + V_{BE}$$

$$= (4\ \text{k}\Omega \times 0.023\ \text{mA}) + 0.7\ \text{V} + (2.32\ \text{mA} \times 0.96\ \text{k}\Omega)$$

$$= 3.02\ \text{V}$$

$$V_{Th} = V_{CC} \frac{R_2}{R_1 + R_2}$$

Multiply and divide by R_1

$$\therefore \quad V_{Th} = \frac{V_{CC}}{R_1} \frac{R_1 R_2}{R_1 + R_2}$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{Th} = \frac{V_{CC}}{R_1} R_{Th}$$

$$\therefore \quad R_1 = \frac{V_{CC}}{V_{Th}} R_{Th}$$

$$= \frac{18\ \text{V}}{3.02\ \text{V}} \times 4\ \text{k}\Omega$$

$$= 23.84\ \text{k}\Omega$$

$$R_{Th} = R_1 \parallel R_2$$

$$\therefore \quad \frac{1}{R_{Th}} = \frac{1}{R_1} + \frac{1}{R_2}$$

$$\therefore \quad \frac{1}{R_2} = \frac{1}{R_{Th}} - \frac{1}{R_1} = \frac{R_1 - R_{Th}}{R_{Th}\ R_1}$$

$$R_2 = \frac{R_1\ R_{Th}}{R_1 - R_{Th}}$$

$$= \frac{(23.84\ \text{k}\Omega)(4\ \text{k}\Omega)}{23.84\ \text{k}\Omega - 4\ \text{k}\Omega}$$

$$= 4.81\ \text{k}\Omega$$

Exercise Problems

2.1 A *npn* silicon transistor with V_{BE} = 0.7 V and β = 75 is used in a fixed bias circuit. If R_B = 330 kΩ, R_C = 1.5 kΩ and V_{CC} = 32 V. Find the coordinates of the *Q* point. Draw the dc load line and locate the *Q* point on dc load line.

2.2 A *npn* germanium transistor with V_{BE} = 0.3 V and β = 90 is used in a fixed bias circuit. V_{CC} = 15 V, R_C = 4.7 kΩ and R_B = 820 kΩ. Find the coordinates of the *Q* point and locate it on the dc load line.

2.3 In a fixed bias circuit the coordinates of the *Q* point which is located at the center of the dc load line V_{CE} = 5 V and I_C = 2 mA. Find the values of V_{CC}, R_C, and R_B. Assume a silicon transistor with β = 100.

2.4 For a voltage divider-bias circuit, V_{CC} = 18 V, R_1 = 50 kΩ, R_2 = 12 kΩ, R_C = 2.2 kΩ, R_E = 1 kΩ, V_{BE} = 0.7 V and β = 125. Find the (a) Coordinates of the *Q* point and locate it on the dc load line (b) Stability factors $S(I_{CO})$ and $S(V_{BE})$.

2.5 Find the values of R_1, R_2 and R_E for a voltage divider bias-circuit given that V_{CC} = 30 V, V_{CE} = 15 V, I_C = 3 mA, R_C = 3.3 kΩ, V_{BE} = 0.7 V, β = 100 and $S(I_{CO}) \leq 4$.

Chapter 3

TRANSISTOR AT LOW FRENQUENCIES

To analyse the ac operation of a transistor amplifier, it is necessary to develope an ac equivalent circuit for the transistor. This ac equivalent circuit is called the model of the transistor, which simulates the behavior of the transistor, when an ac signal is present. In order to develop the linear model small signal operation is assumed. At low frequencies the junction capacitance of the transistor are not considered due to their high reactance. In this chapter analysis of CE, CB and CC amplifiers with different biasing schemes has been carried out using the r_e model of the transistor. The effects of source resistance and load resistance are also considered.

3.1 NOTATIONS IN AMPLIFIER ANALYSIS

In an amplifier circuit we come across dc quantities as well as ac quantities. DC voltages and currents result from the biasing network while ac currents and voltages result from the ac input given to the amplifier circuit. To keep dc quantities distinct from ac quantities, the following notations are employed.

DC quantities are represented by upper case letter with uppercase subscripts. For instance:

I_B, I_C and I_E represent dc currents.

V_{BE}, V_{CE}, and V_{CB} represent dc voltages between terminals.

V_B, V_C, and V_E represent dc terminal voltages with respect to ground.

Instantaneous values of ac quantities are represented by lower case letter with lower case subscripts. For instance:

i_b, i_c, and i_e represent instantaneous currents.

v_{be}, v_{ce}, and v_{cb} represent instantaneous voltages between terminals.

v_b, v_c and v_e represent instantaneous terminal voltages with respect to ground.

RMS values of ac quantities are represented by upper case letter with lower case subscripts. For instance:

I_b, I_c and I_e represent rms currents.

V_{be}, V_{ce} and V_{cb} represent rms voltages between terminals.

V_b, V_c and V_e represent rms terminal voltages with respect to ground.

3.2 AC RESISTANCE OF EMITTER BASE DIODE

In order to use the transistor as an amplifying device, it must be biased properly in the active region. That is the emitter-base junction to be forward biased and collector base junction reverse biased. The forward biased emitter-base junction behaves exactly like a forward biased *p-n* junction diode.

The ac resistance of the *p-n* junction diode is given by

$$r_{ac} = \frac{26 \text{ mV}}{I_D} \tag{3.1}$$

where I_D is the dc current through the diode at the Q point. In Equation (3.1), I_D is in milli amperes.

The ac resistance r_e of emitter-base diode can be obtained by replacing I_D by I_E in Equation (3.1).

$$\therefore \qquad r_e = \frac{26 \text{mV}}{I_E} \tag{3.2}$$

I_E is the dc emitter current at the Q point and it is in mill amperes.

3.3 TWO PORT NETWORK

A two port network as the name implies has two ports: an input port and an output port as shown in Fig. 3.1. A port consists of two terminals.

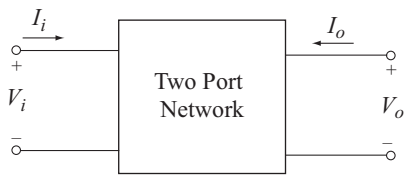


Fig. 3.1 Two port network

A port network is characterized by the two currents, I_i and I_o and the two voltages V_i and V_o.

I_i is the input current
I_o is the output current
V_i is the input voltage
V_o is the output voltage

By convention I_i and I_o are assumed to be into the network.

A BJT has three terminals. It can be modelled as a two port device by making one terminal common to the input and output ports. This leads to the following three configurations of BJT amplifier.

(a) Common emitter (CE) amplifier
(b) Common base (CB) amplifier and
(c) Common collector (CC) amplifier

3.4 MODELING OF TRANSISTOR

In order to analyze the ac operation of a transistor amplifier, it is necessary to develop an ac equivalent circuit for the transistor. This ac equivalent circuit is called the model of the transistor. The model of the transistor is a combination of circuit elements, properly chosen, the best approximates the actual behavior of the transistor under specific operating conditions.

In order to obtain linear relation between input and output variables, small signal operation is assumed in the development of transistor models. Small signal operation means that, the applied ac input signal causes a small variation in output current and voltages about the *Q* point.

At low frequencies the junction capacitances of the transistor act as open circuits due to their high reactance. Thus low frequency small signal models do not consider the effect of these junction capacitances.

At high frequencies the junction capacitances conduct appreciably due to their low reactance, providing a feedback path from output to input. Thus high frequency small signal models takes in account the effect of Junction capacitances.

The two most commonly used models of the transistor used in the analysis and design of transistor amplifiers are:

(a) The hybrid model and

(b) The r_e model

In the hybrid model, the transistor is modelled based on what is happening at its terminals without regard for the physical process taking place inside the transistor. Transistor data sheets provide the parameters of the hybrid model in their listing, and analysis is simply a matter of inserting the equivalent circuit with the listed values.

The r_e model is the more practical model. The important parameter, r_e of this model is determined by the actual operating conditions rather than using a data sheet value. The r_e model does not include feedback term, which in some cases is important.

It is important to note that the hybrid model and the r_e model are the small signal low frequency models. The hybrid π model (discussed later in the chapter) is used almost exclusively for high frequency analysis. The r_e model is infact a reduced version of the hybrid π model.

3.5 THE r_e MODEL OF TRANSISTOR IN COMMON BASE (CB) CONFIGURATION

Figure 3.2 shows an npn-transistor in CB configuration represented as a two port network. Since the base terminal is present both in input and output ports, the configuration is common base. It is important to note that, in a transistor the directions of I_b and I_c are same and always opposite to that of I_e. For an npn-transistor I_e is out of the transistor as indicated by the arrow on the emitter terminal and I_b and I_c are into the transistor.

$$\therefore \qquad I_i = -I_e \tag{3.3}$$

$$\text{and} \qquad I_o = I_c \tag{3.4}$$

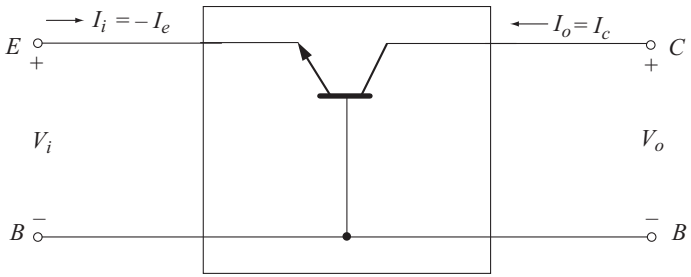


Fig. 3.2 npn-transistor in CB configuration

The emitter-base junction is equivalent to a *p-n* junction diode. Hence at the input, the common base transistor can be represented by a *p-n* diode.

In common-base configuration the current gain alpha is given by

$$\alpha = \frac{I_c}{I_e}$$

or
$$I_c = \alpha I_e \tag{3.5}$$

Note that the collector current I_c is controlled by the emitter current I_e. Hence at the output the common-base transistor can be represented by a controlled current source.

Since I_c flows through the collector-base junction, the controlled current source apperars between the collector and base terminals.

The r_e model of *npn* transistor in CB configuration is shown in Fig. 3.3.

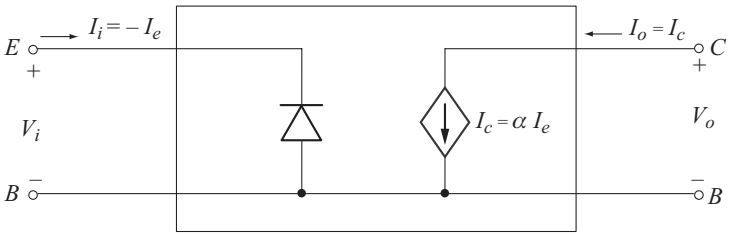


Fig. 3.3 r_e model of transistor in CB configuration

For ac response, the diode can be replaced by its equivalent ac resistance, r_e. The ac resistance of emitter-base diode is given in Equation (3.2) as

$$r_e = \frac{26\,\text{mV}}{I_E} \tag{3.6}$$

The common-base r_e equivalent circuit is obtained by replacing the diode in Fig. 3.3 by its ac resistance r_e. This is shown in Fig. 3.4.

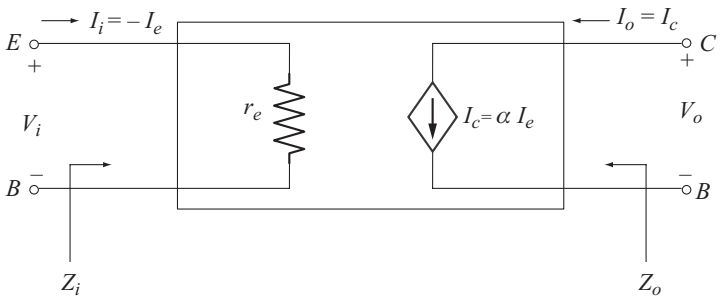


Fig. 3.4 Common base r_e equivalent circuit

From the circuit of Fig. 3.4, let us find the following performance parameters :

- Input impedance Z_i is given by

$$Z_i = \frac{V_i}{I_i} = r_e \tag{3.7}$$

  Note that the input impedance is quite low, which is in the order of few tens of ohms.
- Output impedance Z_o is $\infty\ \Omega$, since the output circuit contains an ideal current source. The output impedance is actually given by the slope of output characteristics. Typically it is in the range of $1-2\ M\Omega$ which is quite a high value.
- With R_L connected between the output terminals, the voltage gain is given by

$$A_V = \frac{V_0}{V_i} = \frac{\alpha\ R_L}{r_e} \tag{3.8}$$

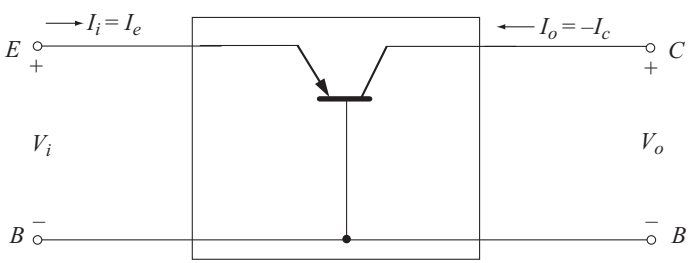
  Since A_V is positive, V_o and V_i are in phase. Also, due to low value of r_e, A_V is quite high.
- With R_L connected between the output terminals, the current gain is given by

$$A_I = \frac{I_o}{I_i} = -\alpha \approx -1 \tag{3.9}$$

  Note that the magnitude of current gain is approximately unity.

3.6 r_e MODEL OF PNP TRANSISTOR IN CB CONFIGURATION

Figure 3.5 shows the r_e model of pnp transistor in CB configuration. Note that for pnp transistor, I_e is into the transistor. Therefore I_b and I_c are out of the transistor.



(a)

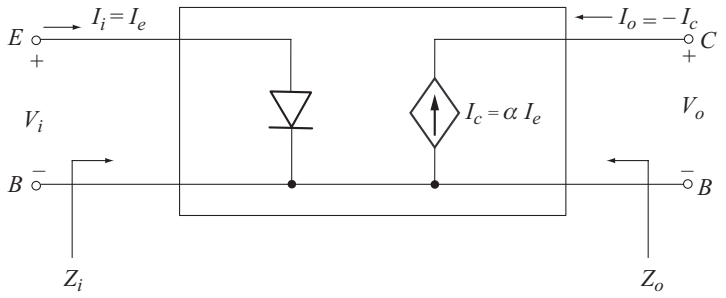


Fig. 3.5 r_e model of pnp transistor in CB configuration

It can be verified that, all results obtained for CB amplifier using npn transistor can be applied for this case also. Thus ac analysis of transistor amplifier is independent of the type of transistor (whether npn or pnp) used in the circuit.

Example 3.1

For the common base configuration of Fig. 3.2, $I_E = 4$ mA, $\alpha = 0.991$. An ac signal of 3 mV is applied between the base and emitter terminals. If $R_L = 610\ \Omega$. Calculate

(a) r_e and Z_i (b) A_V and A_I

(c) V_o, I_i and I_o (d) Z_o with $r_o = \infty$ and I_c, I_e and I_b

Solution

(a)
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{4\,\text{mA}} = 6.5\ \Omega$$
$$Z_i = r_e = 6.5\ \Omega$$

(b)
$$A_V = \frac{\alpha R_L}{r_e} = \frac{(0.991)(610\Omega)}{(6.5\Omega)} = 93$$
$$A_I = -\alpha = -0.991$$

(c)
$$V_o = A_V V_i = (93)\ (3\ \text{mV}) = 279\ \text{mV}$$
$$I_i = \frac{V_i}{Z_i} = \frac{3\ \text{mV}}{6.5\ \Omega} = 461.52\ \mu\text{A}$$
$$I_o = A_I I_i = -\ (0.991)\ (461.52\ \mu\text{A}) = -\ 457.36\ \mu\text{A}$$

(d)
$$Z_o = r_o = \infty$$
$$I_i = -I_e \quad \text{and} \quad I_o = I_c$$

To avoid confusion with signs, let us take only the magnitudes of I_c, I_b and I_e.

$$\therefore \quad I_e = 461.52\ \mu A$$

$$I_c = 457.36\ \mu A$$

Also $$I_e = I_b + I_c$$

$$\therefore \quad I_b = I_e - I_c = 461.52\ \mu A - 457.36\ \mu A = 4.16\ \mu A$$

3.7 THE r_e MODEL OF TRANSISTOR IN COMMON-EMITTER (CE) CONFIGURATION

Figure 3.6 shows an npn transistor in CE configuration represented as a two port network. The input terminals are the base and emitter terminals, and the output terminals are the collector and emitter terminals. Note that the emitter terminal is common between the input and output ports. The input current is I_b and the output current is I_c.

$$\therefore \quad I_i = I_b \tag{3.10}$$

and $$I_o = I_c \tag{3.11}$$

The emitter-base junction is equivalent to a *p-n* junction diode. Hence between the emitter and base terminals, the common-emitter transistor can be modelled as a *p-n* diode.

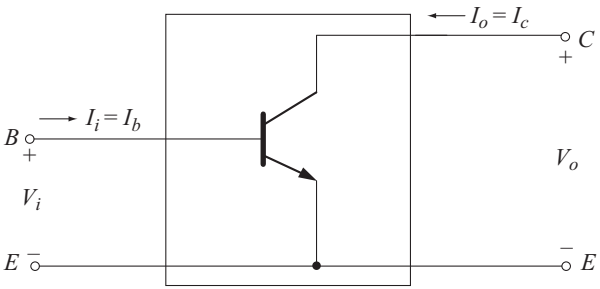


Fig. 3.6 npn transistor in CE configuration

In common-emitter configuration the current gain Beta is given by

$$\beta = \frac{I_c}{I_b}$$

or $$I_c = \beta I_b \tag{3.12}$$

Note that the collector current I_c is controlled by the base current I_b. Since I_c flows through the collector-base junction, the controlled current source is connected between the collector and base terminals. The r_e model is shown in Fig. 3.7.

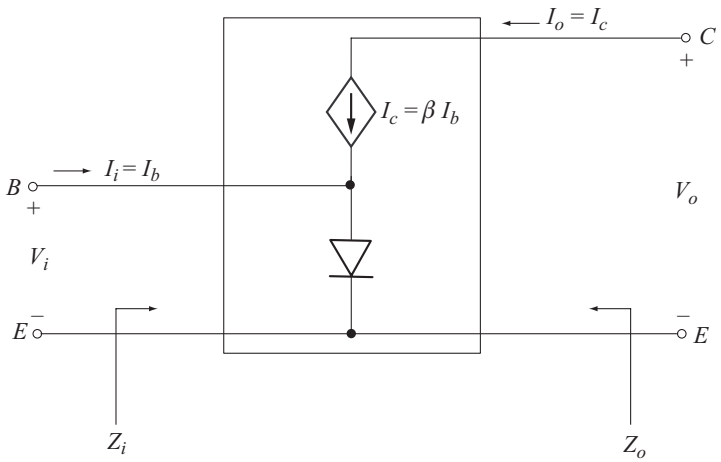


Fig. 3.7 r_e model of transistor in CE Configuration

For ac response, the diode can be replaced by its equivalent ac resistance, r_e as shown in Fig. 3.8.

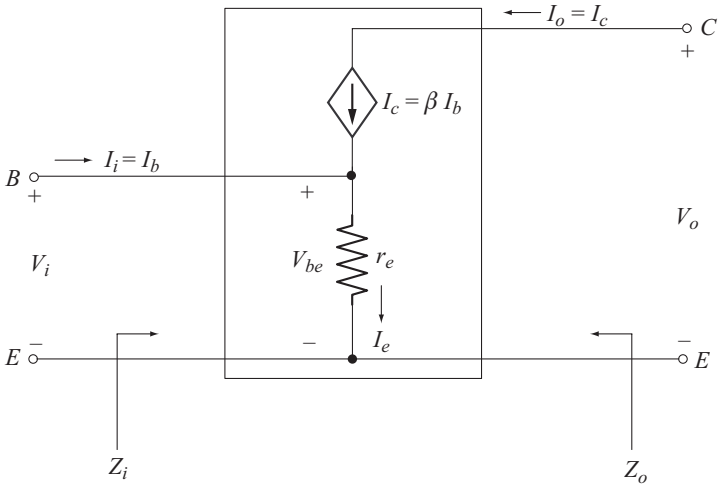


Fig. 3.8 Common emitter r_e equivalent circuit

Input Impedance (Z_i)

$$Z_i = \frac{V_i}{I_i} \tag{3.13}$$

$$V_i = V_{be} = I_e r_e = (1+\beta) I_b r_e$$
$$\approx \beta I_b r_e \quad (\text{since } 1+\beta \approx \beta) \tag{3.14}$$

Also $I_i = I_b$

$$\text{Now} \qquad Z_i = \frac{\beta I_b r_e}{I_b}$$

$$\text{or} \qquad Z_i = \beta r_e \tag{3.15}$$

Note that the input impedance of transistor in CE configuration is β times the value of r_e. Stated alternatively, **a resistive element in the emitter leg is reflected into the input circuit with a multiplying factor β**.

For instance if $r_e = 6.5\ \Omega$ and $\beta = 200$, the input impedance is

$$Z_i = \beta r_e = (200)(6.5\ \Omega) = 1.3\ \text{k}\Omega$$

For the common-emitter configuration, typical values of Z_i range from a few hundred ohms to the kilo ohms range, with a maximum of about 6 kΩ to 7 kΩ.

Output Impedance (Z_o)

The output impedance is given by the reciprocal of output characteristic. Typically it is in the range of 40 – 50 kΩ. Z_o is also denoted by r_o.

Voltage Gain (A_V) and Current Gain (A_I)

With R_L connected between the output terminals, the voltage gain is given by

$$A_V = -\frac{R_L}{r_e} \tag{3.16}$$

The negative sign implies that V_o and V_i are 180° out of phase. The magnitude of voltage gain is

$$|A_V| = \frac{R_L}{r_e} \tag{3.17}$$

Also the current gain is $$A_I = \beta \tag{3.18}$$

Observe that due to low value of r_e and large value of β, the voltage and current gains are quite high.

◆ 3.8 r_e MODEL OF TRANSISTOR IN CE CONFIGURATION INCLUDING r_o

In CE configuration:

(a) The input impedance is measured between the base and emitter terminals. Thus a resistance βr_e is connected between the base and emitter terminals.

(b) The output resistance is measured between the collector and emitter terminals. Thus a resistance r_o is connected between the collector and emitter terminals.

(c) The emitter current I_e is given by

$$I_e = I_b + I_c$$
$$= I_b + \beta I_b$$

Note that the contribution of collector current to make emitter current is βI_b.

Thus a controlled current source of current βI_b is connected between the collector and emitter terminals.

Figure 3.9 shows the r_e model of transistor in CE configuration including the effect of r_o.

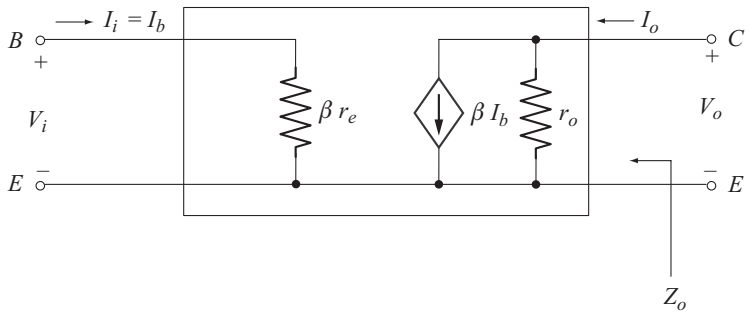


Fig. 3.9 r_e model of CE configuration including r_o

Note: For common-collector (CC) configuration, the model defined for the CE configuration of Fig. 3.8 is usually employed instead of defining a separate model for the CC configuration.

3.9 THE HYBRID EQUIVALENT MODEL

Consider the two port network shown in Fig. 3.10. To develope the hybrid equivalent model of this two port network, let us select I_i and V_o as independent variables and V_i and I_o as dependent variables.

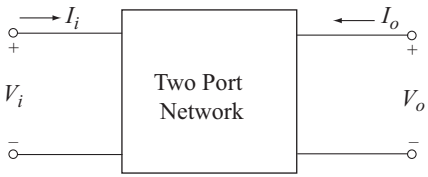


Fig. 3.10 Two port network

We can express V_i and I_o in terms of I_i and V_o as follows:

$$V_i = f_1(I_i, V_o) \tag{3.19}$$

$$I_o = f_2(I_i, V_o) \tag{3.20}$$

Note that we are developing a small signal low frequency model which is a linear model. Thus we can express V_i and I_o as a linear combinations of I_i and V_o.

$$\therefore \quad V_i = h_{11} I_i + h_{12} V_o \tag{3.21}$$

and

$$I_o = h_{21} I_i + h_{22} V_o \tag{3.22}$$

The parameters h_{11}, h_{12}, h_{21} and h_{22} are called the hybrid parameters or *h*-parameters. The name hybrid is due to the fact that they do not have the same units. Let us now, define these parameters.

Set $V_o = 0$ by short circuiting the output terminals:

From Equation (3.21),

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o = 0} \tag{3.23}$$

h_{11} is called the input impedance with output short circuited and has the unit ohms.

From Equation (3.22),

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o = 0} \tag{3.24}$$

h_{21} is the short circuit forward transfer current ratio and has no unit

Set $I_i = 0$ by open circuiting the input:

From Equation (3.21),

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i = 0} \tag{3.25}$$

h_{12} is the open circuit reverse transfer voltage ratio and has no unit

From Equation (3.22),

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i = 0} \tag{3.26}$$

h_{22} is the open circuit output admittance and has the unit mhos.

Note that:

h_{11} has the unit ohms

h_{22} has the unit mhos

h_{12} and h_{21} have no units.

Since these parameters dimensionally differ, they are called hybrid parameters. The double subscript parameter notation can further be reduced to a single subscript notation as follows:

Let i represent 11 denoting input

o represent 22 denoting output

f represent 21 denoting forward transfer

and r represent 12 denoting reverse transfer

Equations (3.21) and (3.22) now become

$$V_i = h_i I_i + h_r V_o \tag{3.27}$$

$$I_o = h_f I_i + h_o V_o \tag{3.28}$$

The circuit model based on Equation (3.27) is shown in Fig. 3.11 and Fig. 3.12 shows the circuit model of Equation (3.28). Note that Equation (3.27) is a KVL equation and Equation (3.28) is a KCL equation.

Equation (3.27) has two components:

$h_i\ I_i$ representing a voltage drop across the impedance h_i and

$h_r\ V_o$ representing a controlled voltage source.

Equation (3.28) has two components:

$h_f\ I_i$ representing a controlled current source and

$h_o\ V_o$ representing the current through admittance h_o.

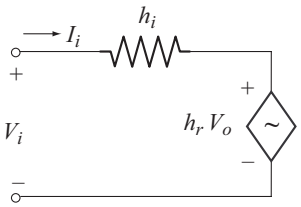


Fig. 3.11 Circuit model of $V_i = h_i I_i + h_r V_o$

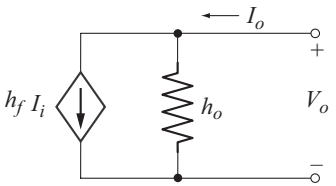


Fig. 3.12 Circuit model of $I_o = h_f I_i + h_o V_o$

Combining these two models, we obtain the hybrid model of the two-port network as shown in Fig. 3.13.

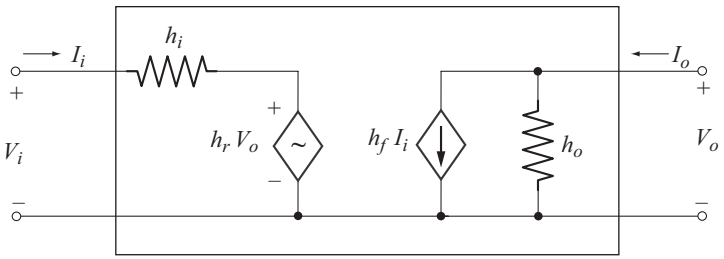


Fig. 3.13 Complete hybrid equivalent circuit

3.9.1 Hybrid Parameter Nomenclature for Transistor

In order to specify the hybrid parameters for a given transistor configuration, a second subscript is used:

e for CE Configuration

b for CB Configuration

and *c* for CC Configuration

This is illustrated in Table 3.1.

Table 3.1 Hybrid parameter nomenclature

Hybrid Parameters	*Configuration*		
	CE	*CB*	*CC*
h_i	h_{ie}	h_{ib}	h_{ic}
h_f	h_{fe}	h_{fb}	h_{fc}
h_r	h_{re}	h_{rb}	h_{rc}
h_o	h_{oe}	h_{ob}	h_{oc}

3.10 HYBRID MODEL OF CB CONFIGURATION

The two port network representation of CB configuration is shown in Fig. 3.14.

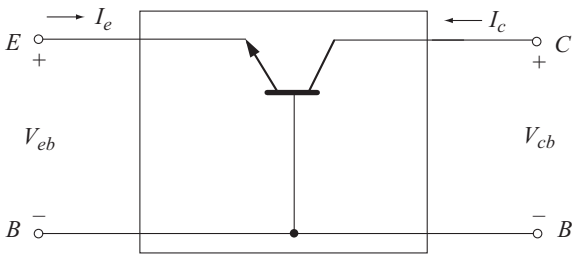


Fig. 3.14 Two port network representation of CB configuration

Comparing the network of Fig. 3.10 and Fig. 3.14, we can list the equivalent voltages and currents as given in Table 3.2.

Table 3.2 Equivalent voltages and currents for CB configuration

General two port network	*CB configuration*
V_i	V_{eb}
I_i	I_e
V_o	V_{cb}
I_o	I_c

Equations (3.21) and (3.22) now become

$$V_{eb} = h_{ib} I_e + h_{rb} V_{cb} \tag{3.29}$$

$$I_c = h_{fb} I_e + h_{ob} V_{cb} \tag{3.30}$$

The hybrid model constructed based on Equations (3.29) and (3.30) is shown in Fig. 3.15.

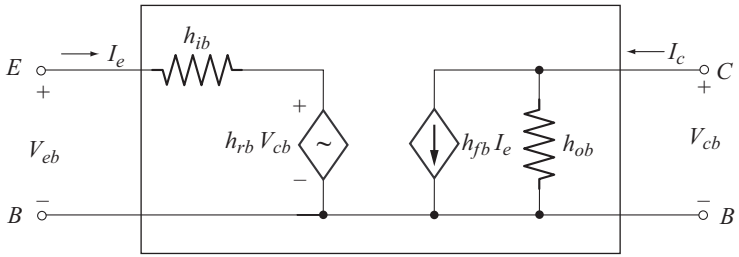


Fig. 3.15 Hybrid model of CB configuration

3.11 HYBRID MODEL OF CE CONFIGURATION

The two port network representation of CE configuration is shown in Fig. 3.16.

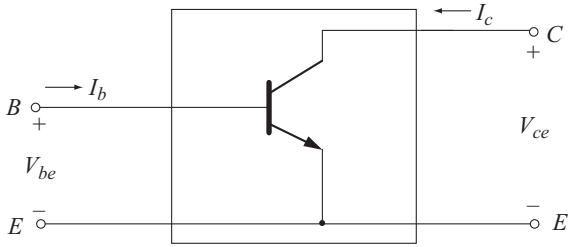


Fig. 3.16 Two port network representation of CE configuration

Comparing the network of Fig. 3.10 and Fig. 3.16 we can list the equivalent voltages and currents as given in Table.3.3.

Table 3.3 Equivalent voltages and currents for CE configuration

General two port network	*CE Configuration*
V_i	V_{be}
I_i	I_b
V_o	V_{ce}
I_o	I_c

Equations (3.21) and (3.22) now become

$$V_{be} = h_{ie}\ I_b + h_{re}\ V_{ce} \tag{3.31}$$

$$I_c = h_{fe}\ I_b + h_{oe}\ V_{ce} \tag{3.32}$$

Based on these equations, the hybrid model for the CE configuration can be developed as shown in Fig. 3.17.

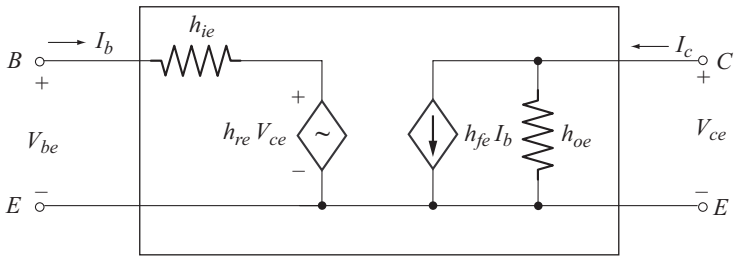


Fig. 3.17 Hybrid model of CE configuration

3.12 HYBRID MODEL OF CC CONFIGURATION

The two port network representation of CC configuration is shown in Fig. 3.18.

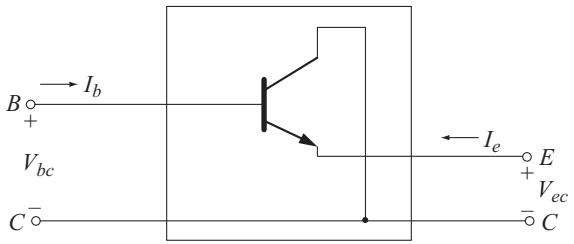


Fig. 3.18 Two port network representation of CC configuration

Comparing the networks of Fig. 3.10 and 3.18 we can list the equivalent voltages and currents as given in Table 3.4.

Table 3.4 Equivalent voltages and currents for CC configuration

General two port network	*CC configuration*
V_i	V_{bc}
I_i	I_b
V_o	V_{ec}
I_o	I_e

Equations (3.21) and (3.22) now become

$$V_{bc} = h_{ic}\ I_b + h_{rc}\ V_{ec} \tag{3.33}$$

$$I_e = h_{fc}\ I_b + h_{oc}\ V_{ec} \tag{3.34}$$

Based on these equations, the hybrid model for the CC configuration can be developed as shown in Fig. 3.19.

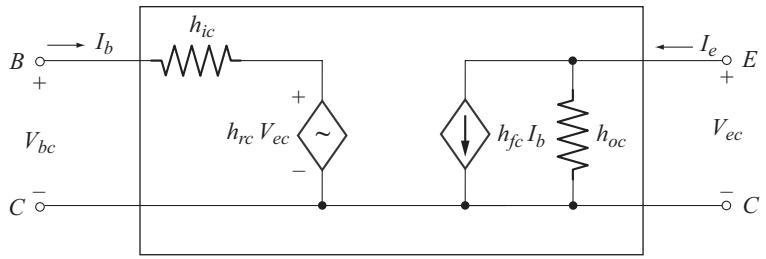


Fig. 3.19 Hybrid model of CC configuration

Typical values of hybrid parameters for all the three configurations are given in Table 3.5.

Table 3.5 Typical values of h-parameters in CE, CB and CC configurations

Parameter	*Configuration*		
	CE	*CB*	*CC*
h_i	1 kΩ	20 Ω	1 kΩ
h_r	2.5×10^{-4}	3.0×10^{-4}	1
h_f	50	– 0.98	– 50
h_o	25 μA/V	0.5 μA/V	25 μA/V
$1/h_o$	40 kΩ	2 MΩ	40 kΩ

3.13 VARIATIONS OF *h*-PARAMETERS

The *h*-parameters in general vary with changes in temperature, frequency, voltage and current. It is worthwhile to look at the variation of *h*-parameters particularly with reference to collector current, collector voltage and temperature. In order to compare the changes in various parameters with temperature, voltage and current variations, the *h*-parameters are normalized to 1. Figure 3.20 shows the variation in *h*-parameters (in CE mode) with collector current for $I_C = 1$ mA, $V_{CE} = 5$ V, $T = 25^oC$ and $f = 1$ kHz.

The axis are graduated on a logarithmic scale to accommodate wide variations. The operating point is at $V_{CE} = 5$ V and $I_C = 1$ mA and hence all the parametric curves intersect at this point. Observe from Fig. 3.20 that at $I_C = 0.1$ mA, h_{fe} is 50% of its value at $I_C = 1$ mA. Thus, if h_{fe} is 100 at $I_C = 1$mA, it would be 50 at $I_C = 0.1$ mA. At $I_C = 3$ mA, h_{fe} is 150% of its value at $I_C = 1$ mA. If h_{fe} is 100 at $I_C = 1$ mA, it would be 150 at $I_C = 3$ mA.

Further, observe the variation in h_{re}. The value of h_{re} increases to nearly 10 times its value at $I_C = 1$ mA, while h_{oe} increases to nearly 40 times its value at $I_C = 1$ mA. At such values h_{oe} may become large enough in comparison with load resistance to be ignored while approximating the model. Figure 3.21 shows the variation of *h*-parameters with collector-emitter voltage.

The variations are plotted with reference to the same operating point as in the previous figure. Observe that h_{fe} and h_{ie} do not change much in comparison with h_{re} and h_{oe}. Note that values of h_{oe} and h_{re} increase significantly on either sides of the operating point. Further, both with respect to

changes in collector current as well as collector voltage, variation in h_{fe} is minimal when compared to other parameters.

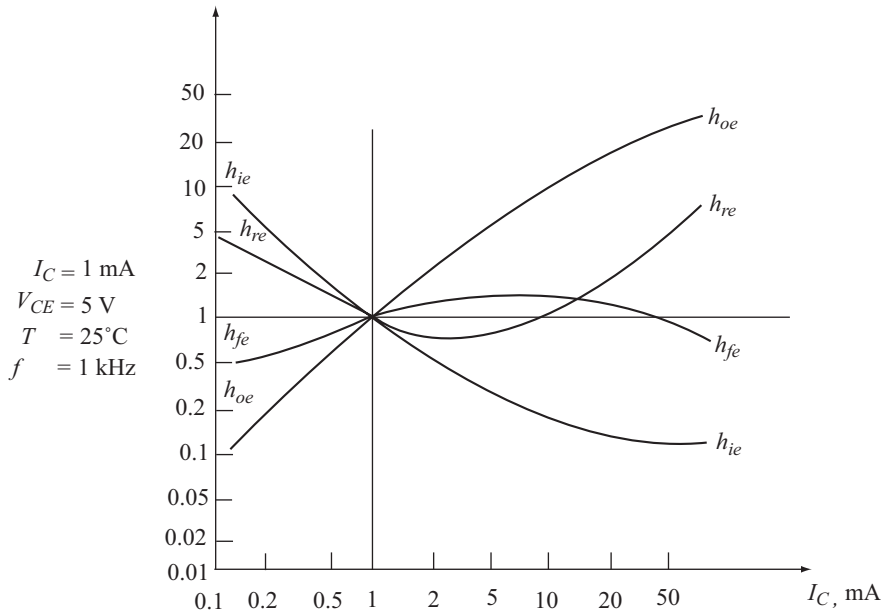


Fig. 3.20 Variation of CE h-parameters with collector current

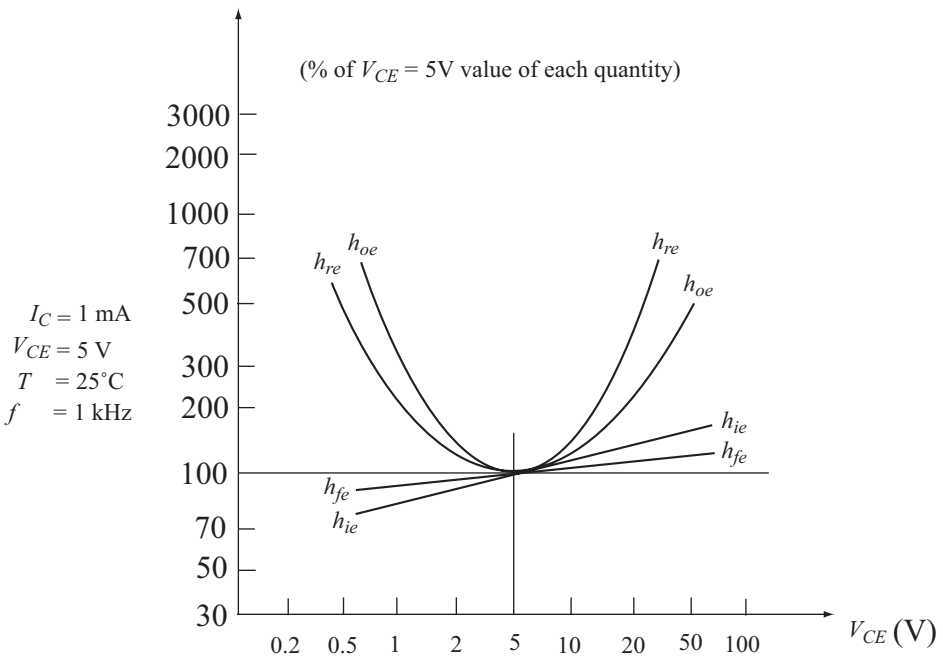


Fig. 3.21 Variation of CE h-parameters with collector-emitter voltage

Figure 3.22 shows the variation of *h*-parameters with respect to temperature. Observe that h_{oe} is least affected by the changes in temperature. However, in general, the values of all parameters increase with temperature. The value of input impedance h_{ie} varies the most with temperature. The value of h_{fe} drops to half its value at 25° C at a temperature of – 50° C and, at 150° C it increases to 150% of its value at 25° C. All these variations must be taken into consideration when designing circuits using transistors.

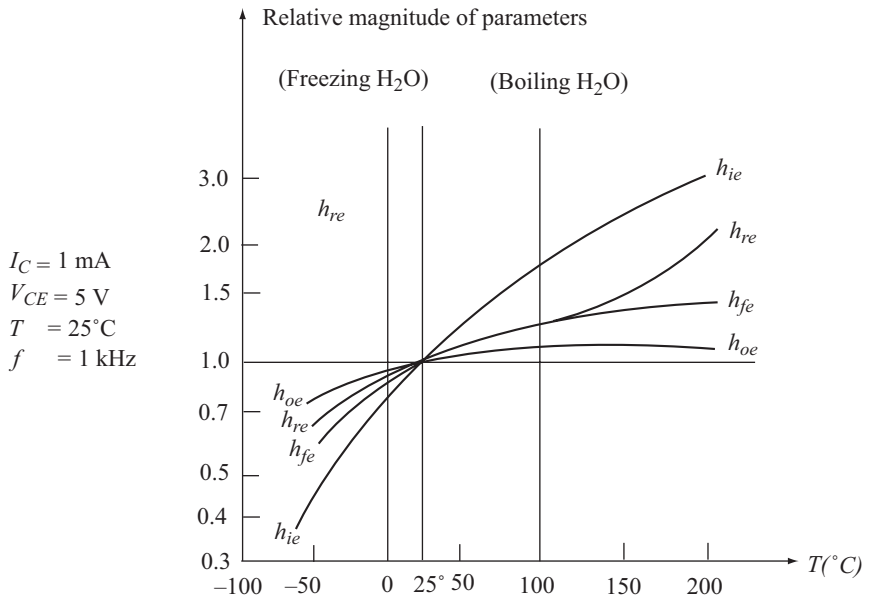


Fig. 3.22 Variation of CE h-parameters with temperature

3.14 ADVANTAGES OF *h*-PARAMETERS

The advantages of *h*-parameters are :

- The *h*-parameters are extremely useful in the analysis and design of circuits using transistors.
- At audio frequencies the *h*-parameters are real numbers which makes computations easy. This is essentially true because all capacitances have been treated as open circuits at low-frequencies.
- These parameters can be easily determined from the transistor characteristics.
- Since, we started the definition of *h*-parameters, by considering the transistor as a general two-port, four-terminal device, the models developed are independent of whether the transistors are of *npn* or *pnp* type.
- Further, once the *h*-parameters are graphically obtained for one configuration, the *h*-parameters of other configurations can be obtained by a simple conversion.

◆ 3.15 APPROXIMATE HYBRID EQUIVALENT CIRCUIT

Consider the hybrid equivalent circuit of Fig. 3.13. For the CE and CB configurations, the magnitude of h_r and h_o is such that the results obtained for the important quantities such as Z_o, Z_i A_V and A_I are only slightly affected if h_r and h_o are not included in the model.

From Table 3.5 we find that

$$h_{re} = 2.5 \times 10^{-4} \quad \text{and} \quad h_{rb} = 3.0 \times 10^{-4}$$

Due to very small values of h_{re} and h_{rb} we can take h_{re} and h_{rb} approximately equal to zero. As a result $h_r V_o = 0$. Thus the controlled voltage source $h_r V_o$ can be replaced by a short circuit as shown in Fig. 3.23.

Also from Table 3.5 we find that

$$1 / h_{oe} = 40 \text{ k}\Omega \quad \text{and} \quad 1 / h_{ob} = 2 \text{ M}\Omega$$

In practical situations, these values are quiet large when compared with the parallel load R_L which will be connected between the output terminals. Thus $1 / h_o$ can be replaced by an open circuit as shown in Fig. 3.23.

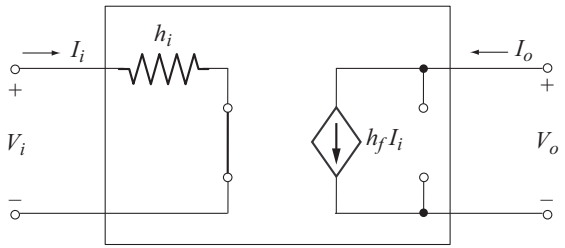


Fig. 3.23 Removing h_r and h_o from the hybrid equivalent model

Figure 3.24 shows the approximate hybrid equivalent circuit.

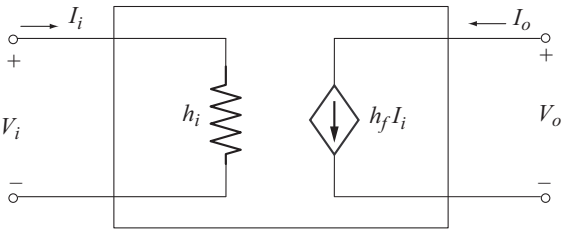


Fig. 3.24 Approximate hybrid equivalent circuit

The approximate hybrid equivalent circuit for CE configuration is shown in Fig. 3.25.

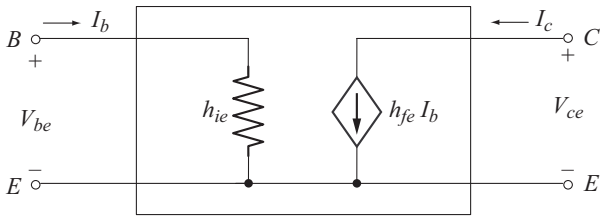


Fig. 3.25 Approximate hybrid equivalent circuit for CE configuration

Figure 3.26 shows the approximate hybrid equivalent circuit for CB configuration.

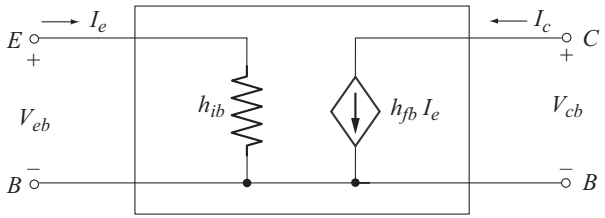


Fig. 3.26 Approximate hybrid equivalent circuit for CB configuration

3.16 RELATION BETWEEN THE PARAMETERS OF HYBRID MODEL AND THE r_e MODEL

Figure 3.27 shows the comparison between the approximate hybrid model and the r_e model of the transistor in CE configuration.

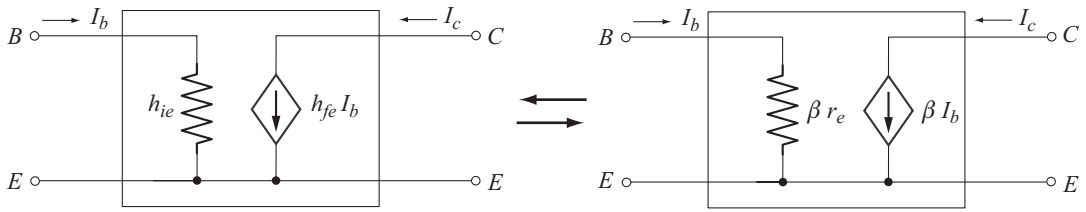


Fig. 3.27 Hybrid model versus r_e model for CE configuration

Comparing the two models we obtain the following relations:

$$h_{ie} = \beta\, r_e \tag{3.35}$$

and

$$h_{fe} = \beta \tag{3.36}$$

In Fig. 3.28 the approximate hybrid model and r_e model of the transistor in CB configuration are compared.

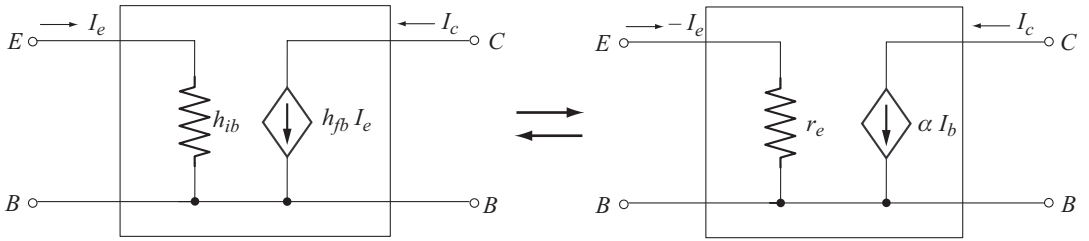


Fig. 3.28 Hybrid model versus r_e model for CB configuration

Comparing the two models we obtain the following relations:

$$h_{ib} = r_e \tag{3.37}$$
$$h_{fb} = \alpha$$

In any transistor (either pnp or npn) I_e and I_c are in opposite directions. Therefore h_{fb}, which is the ratio of I_c to I_e must have negative sign. But the value of α is given with positive sign. Hence it is appropriate to write.

$$h_{fb} = -\alpha \tag{3.38}$$

Since $\alpha \approx 1$, we can write

$$h_{fb} = -\alpha \approx -1 \tag{3.39}$$

3.16.1 Conversion between Hybrid Parameters

Having obtained the hybrid parameters for one transistor configuration, it is easy to find the parameters for other transistor configurations by a simple conversion.

Usually the CB and CC parameters are expressed in terms of the popular CE parameters as given below.

CB Hybrid Parameters in Terms of CE Hybrid Parameters

$$h_{ib} = \frac{h_{ie}}{1+h_{fe}} \tag{3.40}$$

$$h_{rb} = \frac{h_{ie}\, h_{oe}}{1+h_{fe}} - h_{re} \tag{3.41}$$

$$h_{fb} = \frac{-h_{fe}}{1+h_{fe}} \tag{3.42}$$

$$h_{ob} = \frac{h_{oe}}{1+h_{fe}} \tag{3.43}$$

CC Hybrid Parameters in Terms of CE Hybrid Parameters

$$h_{ic} = h_{ie} \tag{3.44}$$

$$h_{rc} = 1 - h_{re} \tag{3.45}$$

$$h_{fc} = -(1 + h_{fe}) \tag{3.46}$$

$$h_{oc} = h_{oe} \tag{3.47}$$

Example 3.2

Given $I_E = 3.2$ mA, $h_{fe} = 150$, $r_o = \dfrac{1}{h_{oe}} = 40$ kΩ and $h_{ob} = 0.5$ μS, determine

(a) The common-emitter hybrid equivalent circuit
(b) The common-base r_e model.

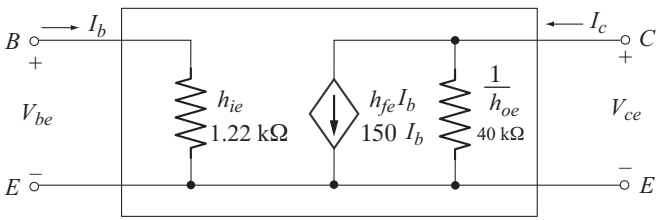
Solution

(a)

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{3.2\,\text{mA}} = 8.125\ \Omega$$

$$h_{ie} = \beta\, r_e = (150)\,(8.125\ \Omega) = 1.22\ \text{k}\Omega$$

The common-emitter hybrid equivalent circuit is shown below.

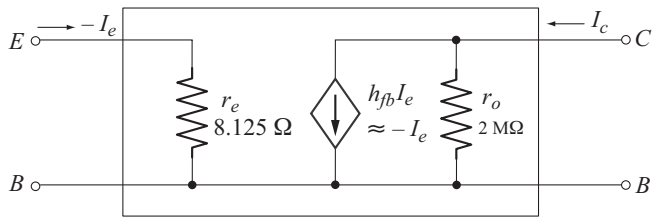


(b)

$$r_o = \frac{1}{h_{ob}} = \frac{1}{0.5\ \mu\text{S}} = 2\ \text{M}\Omega$$

$$h_{fb} = \frac{-h_{fe}}{1+h_{fe}} = \frac{-150}{151} = -0.993 \approx -1$$

The common-base r_e model is shown below.



3.17 HYBRID π MODEL

At high frequencies the effect of junction capacitances of the transistor has to be considered since they conduct appreciable amount of current due to their low reactance. The high frequency model of the transistor in CE configuration in which these capacitive effects are taken into consideration is called the hybrid π model or GIACOLETTO MODEL and is shown in Fig. 3.29.

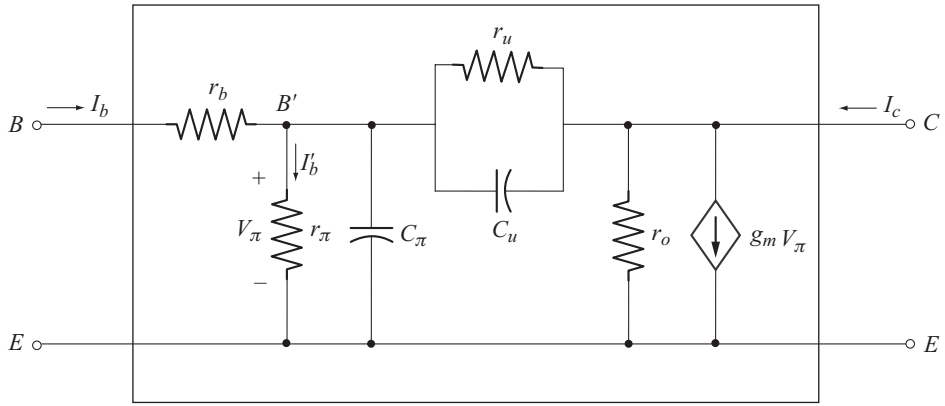


Fig. 3.29 The hybrid-π model of transistor in CE configuration

Let us discuss the significance of each component in the model shown in Fig. 3.29.

Hybrid π Capacitances

In chapter, 1, we have seen that a forward biased p-n junction exhibits diffusion capacitance and a reverse biased p-n junction exhibits transition capacitance.

In the model of Fig. 3.29, C_π represents the diffusion capacitance of forward-biased emitter-base junction. This capacitance is an indicative of excess minority carrier storage in the base. C_π is usually just a few picofarads to a few tens of picofarads.

C_u represents the transition capacitance of the reverse biased collector-base junction. C_u typically extends from less than 1 pF to a few Picofarads.

C_π and C_u are alternatively represented by C_{be} and C_{bc} respectively.

Hybrid π Resistances

The internal node B' is not physically accessible as shown in Fig. 3.30. Node B represents the external base terminal. The resistance r_b includes the following.

- the base contact resistance
- the base bulk resistance and
- the base spreading resistance.

It is typically a few ohms to tens of ohms.

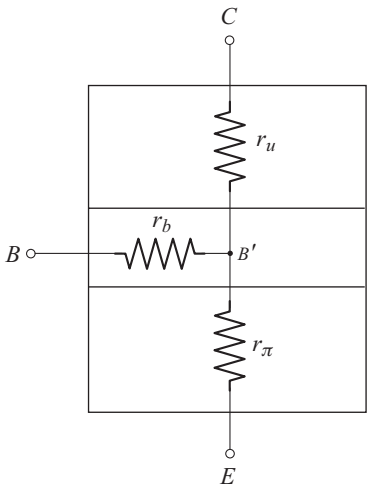


Fig. 3.30 Hybrid π resistances

The resistors r_π, r_u and r_o are the resistances between the indicated terminals of the transistor when the transistor is in the active region.

The resistance r_π is identical to $\beta\, r_e$ introduced in the common-emitter r_e model. The resistance r_u represents the feedback from collector to base. It is very large typically in the mega ohm range.

r_o is the output resistance which appears between the collector and emitter terminals. Typically it lies in the range of 5 kΩ to 40 kΩ and it is determined from the hybrid parameter h_{oe}.

Hybrid π Conductance

The small signal collector current, due to small change in the voltage V_π, with the collector shorted to emitter is accounted by the voltage controlled current source $g_m V_\pi$ connected between the collector and emitter terminals.

The subscripts π and u is associated with hybrid π parameters have the following meaning.

π : comes from the hybrid π terminology.

u : the element with this subscript provides union between collector and base terminals.

Hybrid π Parameters in Terms of r_e and h Parameters

The following relations can be used to find the parameters of hybrid π model using r_e and the h parameters.

$$r_\pi = \beta\, r_e \tag{3.48}$$

$$g_m = \frac{1}{r_e} \tag{3.49}$$

$$r_0 = \frac{1}{h_{oe}} \tag{3.50}$$

$$h_{re} = \frac{r_\pi}{r_\pi + r_u} \approx \frac{r_\pi}{r_u} \tag{3.51}$$

3.17.1 Low Frequency Hybrid Model from Hybrid π Model

For low-to-mid frequency analysis, the effect of capacitances C_π and C_u can be neglected due to the very high reactance associatd with each of them.

The resistance r_b is usually so small, it can be replaced by a short-circuit. The resistance r_u usually so large, it can be treated as an open circuit.

The simplified low frequency hybrid π model is shown in Fig. 3.31.

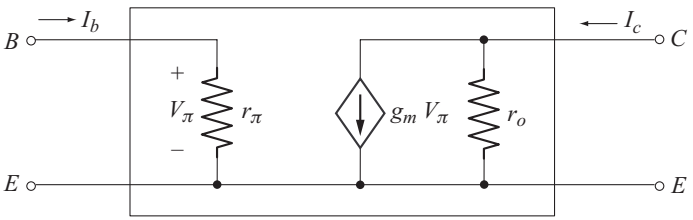


Fig. 3.31 Simplified low frequency hybrid π model

$$r_\pi = \beta r_e = h_{ie}$$
$$r_0 = 1 / h_{oe}$$
$$V_\pi = I_b r_\pi = I_b \beta r_e$$
$$g_m V_\pi = \frac{1}{r_e}(I_b \beta r_e) = \beta I_b = h_{fe} I_b \quad (\because \beta = h_{fe})$$

The resulting model is shown in Fig. 3.32 which is same as the low frequency hybrid model with h_{re} taken equal to zero.

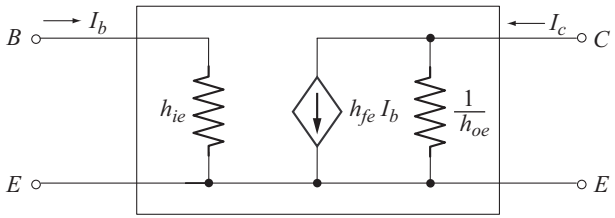


Fig. 3.32 Low frequency hybrid model with h_{re} removed

Example 3.3

(a) Sketch the Giacoletto (hybrid π) model for a common-emitter transistor given that:

$r_b = 4\ \Omega$ $\quad C_\pi = 5$ pF $\quad C_u = 1.5$ pF
$h_{oe} = 18\ \mu$S $\quad \beta = 120$ $\quad r_e = 14\ \Omega$

(b) If the applied load is 1.2 kΩ and the source resistance is 250 Ω, draw the approximate hybrid π model for low and mid frequency range.

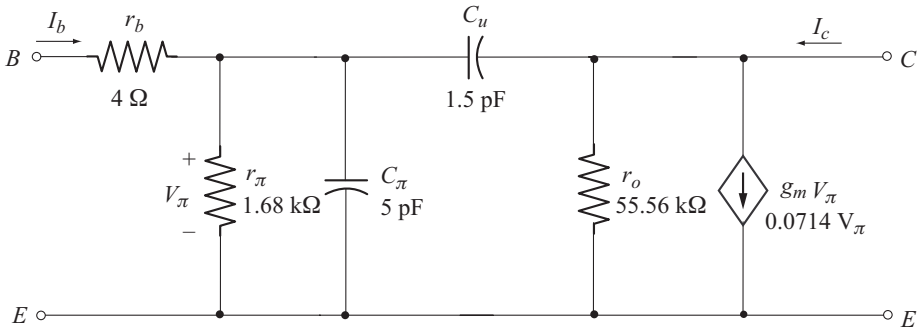
Solution

(a)
$$r_\pi = \beta r_e = (120)\,(14\ \Omega) = 1.68\ \text{k}\Omega$$
$$g_m = \frac{1}{r_e} = \frac{1}{14\ \Omega} = 0.0714\ \text{℧}$$
$$r_o = \frac{1}{h_{oe}} = \frac{1}{18 \times 10^{-6}} = 55.56\ \text{k}\Omega$$
$$h_{re} \approx \frac{r_\pi}{r_u} \quad \Rightarrow \quad r_u = \frac{r_\pi}{h_{re}}$$

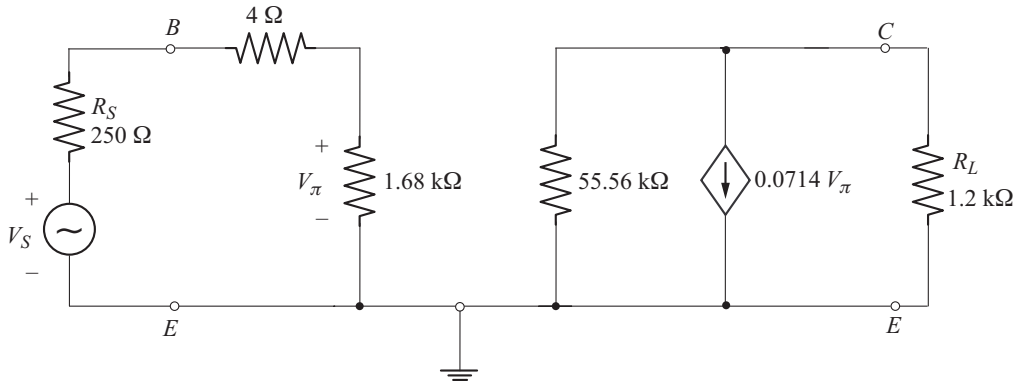
Since h_{re} is not given, let us take $h_{re} = 0$

$\therefore$ $r_u = \infty \Rightarrow$ open circuit.

The hybrid π model is shown below.



(b) For low and mid frequency range of operation, the capacitors C_u and C_π can be replaced by open circuit equivalent due their high reactance. The simplified hybrid π model is shown below.



3.18 COMMON-EMITTER FIXED-BIAS CONFIGURATION

Figure 3.33 shows the common-emitter amplifier using fixed bias. The ac input signal V_i is applied to the base of transistor through the input coupling capacitor C_1. The amplified signal V_o is taken at the collector through the output coupling capacitor C_2.

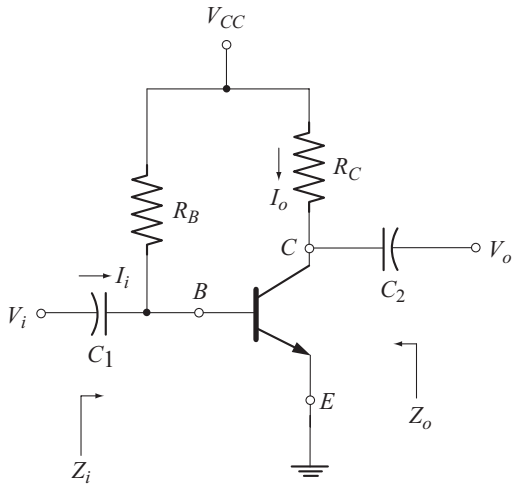


Fig. 3.33 Common-emitter fixed bias configuration

In order to perform the small-signal ac analysis let us obtain the ac equivalent circuit by reducing the dc source V_{CC} to zero and short circuiting the coupling capacitors C_1 and C_2 as shown in Fig. 3.34.

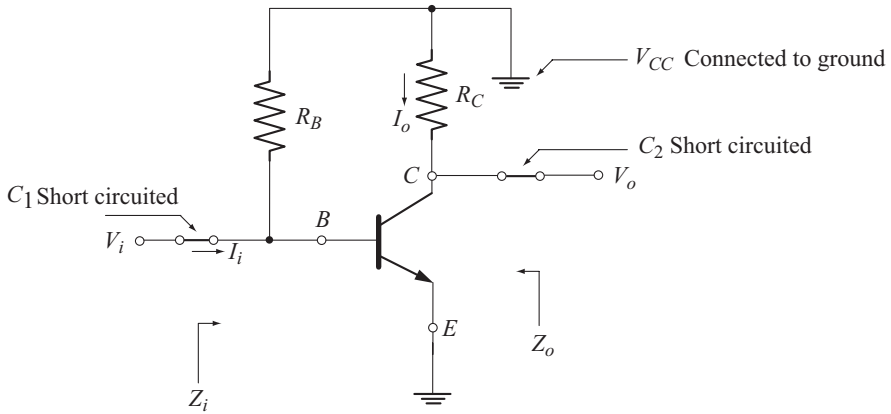


Fig. 3.34 AC equivalent circuit

Note that R_B appears between base and ground and R_C between collector and ground. The ac equivalent circuit is redrawn in Fig. 3.35.

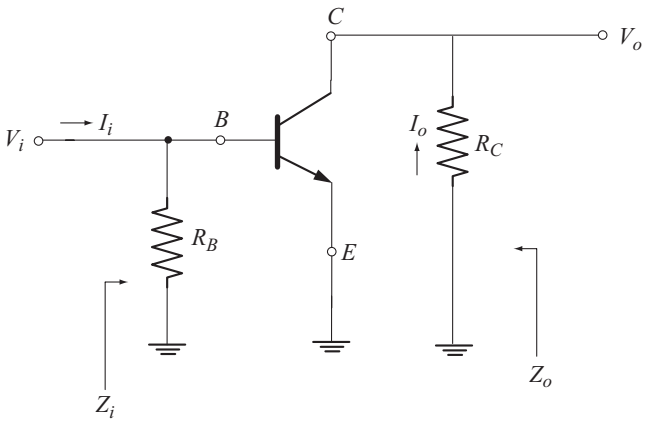


Fig. 3.35 AC equivalent circuit redrawn

Note that the emitter terminal is common to input and output circuits. Hence the configuration is common-emitter. Let us replace the transistor by its common emitter r_e model as shown in Fig. 3.36.

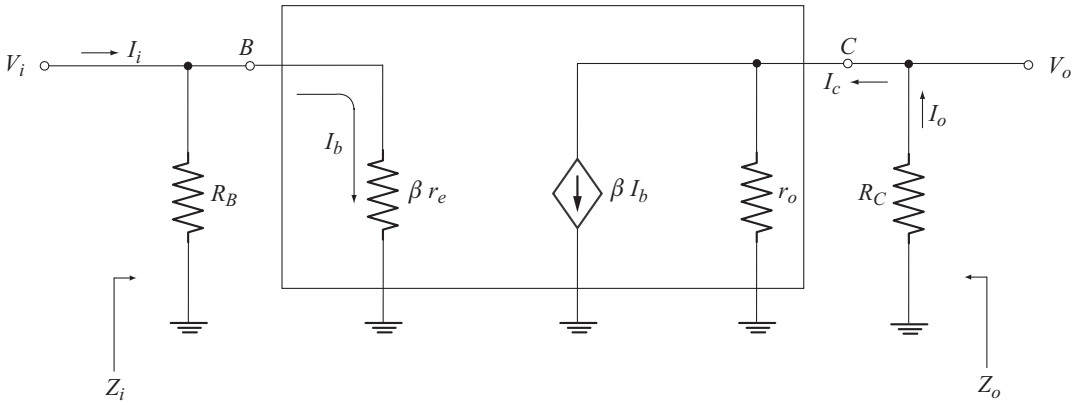


Fig. 3.36 AC equivalent circuit with r_e model

3.18.1 Input Impedance (Z_i)

The input impedance is given by

$$Z_i = \frac{V_i}{I_i} \tag{3.52}$$

From the input circuit of Fig. 3.36, we find that, Z_i is given by the parallel combination of R_B and βr_e.

$$\therefore \quad Z_i = R_B \| \beta r_e \tag{3.53}$$

3.18.2 Output Impedance (Z_o)

To find the output impedance we have to reduce V_i to zero.

With $V_i = 0, I_i = 0, \ I_b = 0$ and therefore $\beta I_b = 0$. Thus we have to open circuit the current source. The output equivalent circuit under this condition is shown in Fig. 3.37.

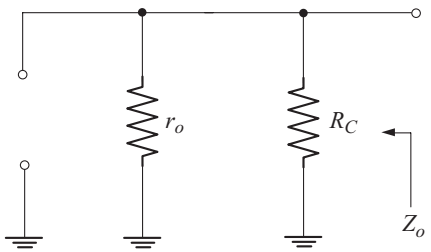


Fig. 3.37 Circuit to find Z_o

Note that Z_o is given by the parallel combination of r_o and R_C

$$\therefore \qquad Z_o = r_o \| R_C \tag{3.54}$$

3.18.3 Voltage Gain (A_v)

To find the voltage gain let us consider the output equivalent circuit shown in Fig. 3.38.

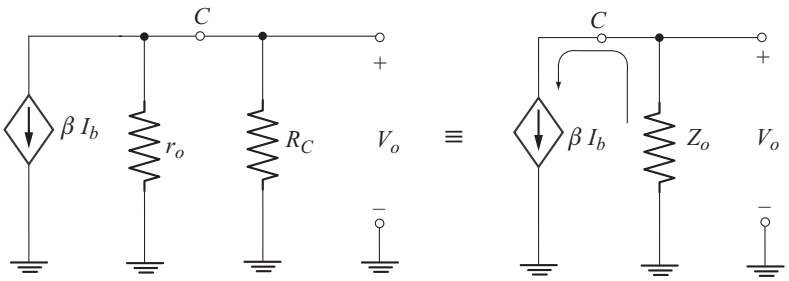


Fig. 3.38 Circuit to find V_o

$$\begin{aligned} V_o &= -\beta I_b Z_o \\ &= -\beta I_b [r_o \| R_C] \end{aligned} \tag{3.55}$$

From the input circuit of Fig. 3.36 we have

$$V_i = I_b [\beta r_e] \tag{3.56}$$

Now the voltage gain is

$$A_V = \frac{V_o}{V_i}$$

$$= \frac{-\beta\ I_b\ [r_o \parallel R_C]}{I_b\ [\beta r_e]}$$

$$A_V = -\frac{r_o \parallel R_C}{r_e} \tag{3.57}$$

If $R_B \geq 10\,\beta\, r_e$, $\quad R_B \parallel \beta\, r_e \approx \beta\, r_e$

Now Equation (3.53) become

$$Z_i \approx \beta r_e \tag{3.58}$$

For $r_o \geq 10\, R_C$

Under this situation

$$R_C \parallel r_o \approx R_C$$

From Equation (3.54)

$$Z_o \approx R_C \tag{3.59}$$

From Equation (3.57)

$$A_V \approx -\frac{R_C}{r_e} \tag{3.60}$$

3.18.4 Current Gain (A_I)

The current gain is defined by

$$A_I = \frac{I_o}{I_i} \tag{3.61}$$

$$V_0 = -I_o R_C \quad \text{(From Fig. 3.36)}$$

$$\therefore \quad I_o = \frac{-V_o}{R_C} \tag{3.62}$$

$$\text{Also} \quad I_i = \frac{V_i}{Z_i} \tag{3.63}$$

Using these relations in Equation (3.61) we have

$$A_V = \left[\frac{-V_o}{R_C}\right] \div \left[\frac{V_i}{Z_i}\right]$$

$$= -\left[\frac{V_o}{V_i}\right]\left[\frac{Z_i}{R_C}\right]$$

$$A_I = -\frac{A_V\, Z_i}{R_C} \tag{3.64}$$

Using Equations (3.60) and (3.58) for A_V and Z_i respectively, we obtain

$$A_I \approx -\left[\frac{1}{R_C}\right]\left(\frac{-R_C}{r_e}\right)(\beta\, r_e)$$

$$A_I \approx \beta \tag{3.65}$$

3.18.5 Phase Relationship

The negative sign in the equation for A_V implies that the input signal V_i and the output signal V_o are 180° out of phase as shown in Fig. 3.39.

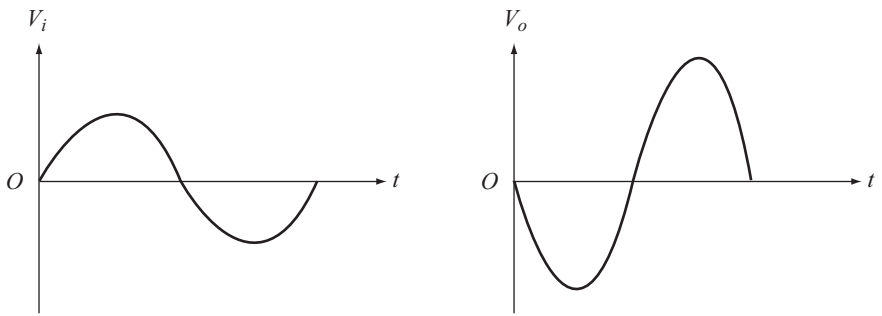


Fig. 3.39 180° Phase shift between V_i and V_0

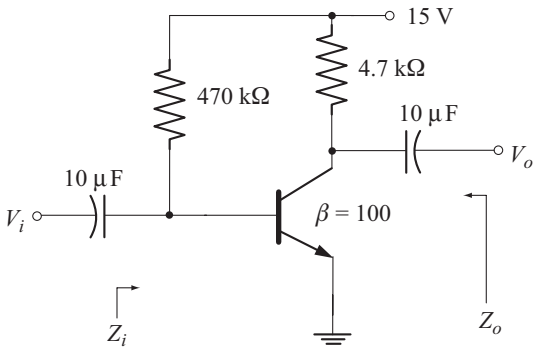
Example 3.4

For the circuit shown below:

(a) Determine r_e

(b) Find Z_i, Z_o, A_V and A_I (with $r_o = \infty\ \Omega$)

(c) Repeat part (b) taking $r_o = 50\ \text{k}\Omega$ and compare the results.



Solution

(a)

$$r_e = \frac{26\,\text{mV}}{I_E}$$

$$I_E = (1+\beta)\, I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{15\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega} = 30.43\ \mu\text{A}$$

$$I_E = (101)\,(30.43\ \mu\text{A}) = 3.073\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{3.073\text{ mA}} = 8.46\ \Omega$$

(b)

$$Z_i = R_B \parallel \beta r_e$$

$$\beta r_e = (100)\,(8.46\ \Omega) = 846\ \Omega$$

$$Z_i = 470\text{ k}\Omega \parallel 846\ \Omega = 844.47\ \Omega$$

$$Z_o = r_o \parallel R_C = \infty\ \Omega \parallel 4.7\text{ k}\Omega = 4.7\text{ k}\Omega$$

$$A_V = -\frac{r_0 \parallel R_C}{r_e} = -\frac{4.7\text{ k}\Omega}{8.46\ \Omega} = -555.55$$

$$A_I = \frac{-A_V Z_i}{R_C} = \frac{-(-555.55)\,(844.47\Omega)}{4.7\text{ k}\Omega} = 99.82$$

(c) When $r_o = 50\text{ k}\Omega$

Z_i is not affected by r_o

$\therefore$ $Z_i = 844.47\ \Omega$. (As calculated in part (b))

$$Z_o = 50\text{ k}\Omega \parallel 4.7\text{ k}\Omega = 4.3\text{ k}\Omega$$

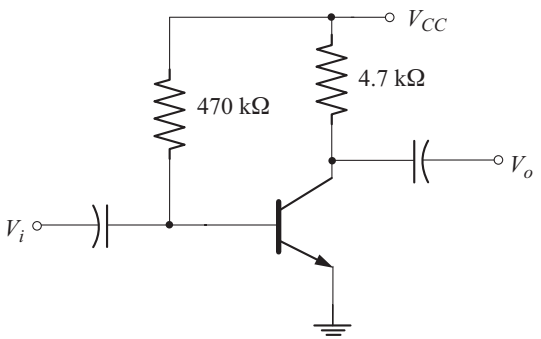
$$A_V = \frac{-4.3\text{ k}\Omega}{8.46\ \Omega} = -508.27$$

$$A_I = -\frac{(-508.27)(844.47\ \Omega)}{(4.7\text{ k}\Omega)} = 91.32$$

Note that the values of Z_o and A_V with finite r_o are less than that with $r_o = \infty$.

Example 3.5

For the amplifier circuit shown below calculate V_{CC} for a voltage gain of $A_V = -200$. Take $\beta = 90$ and $r_o = \infty\ \Omega$.



Solution

$$A_V = -\frac{r_o \parallel R_C}{r_e}$$

$$R_C \parallel r_o = 4.7\ \text{k}\Omega \parallel \infty\ \Omega$$

$$= 4.7\ \text{k}\Omega$$

$$-200 = \frac{-4.7\,\text{k}\Omega}{r_e}$$

$$r_e = 23.5\ \Omega$$

$$r_e = \frac{26\,\text{mV}}{I_E}$$

$$I_E = \frac{26\,\text{mV}}{23.5\,\Omega} = 1.106\ \text{mA}$$

$$I_E = (1+\beta)\, I_B$$

$$I_B = \frac{I_E}{1+\beta} = \frac{1.106\,\text{mA}}{91} = 12.15\ \mu\text{A}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

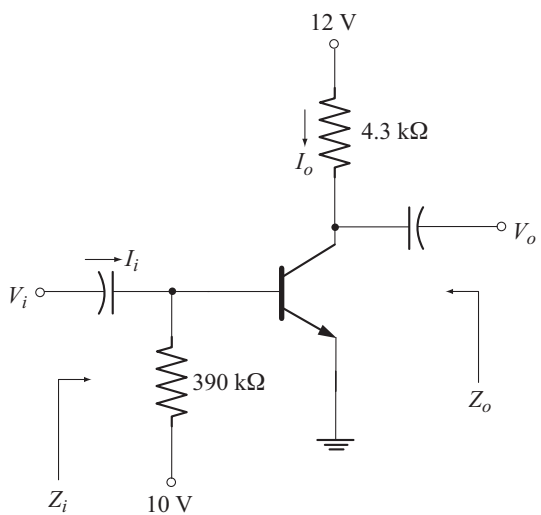
$$\Rightarrow \quad V_{CC} = I_B R_B + V_{BE} = (12.15\ \mu\text{A})\ (470\ \text{k}\Omega) + 0.7\ \text{V} = 6.4\ \text{V}$$

Example 3.6

For the circuit shown below, taking $\beta = 100$ and $r_o = 60\ \text{k}\Omega$, calculate

(a) r_e (b) Z_i and Z_o

(c) A_V (d) the effect of $r_o = 30\ \text{k}\Omega$ on A_V



(a)
$$I_B = \frac{10\text{V} - V_{BE}}{390\,\text{k}\Omega} = \frac{10\,\text{V} - 0.7\,\text{V}}{390\ \text{k}\Omega} = 23.85\ \mu\text{A}$$
$$I_E = (1+\beta)\, I_B = (101)\ (23.85\ \mu\text{A}) = 2.4\ \text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.4\,\text{mA}} = 10.83\ \Omega$$

(b) From the given figure, $R_B = 390\ \text{k}\Omega$ and $R_C = 4.3\text{k}\Omega$
$$Z_i = \beta\, r_e = (100)(10.83\ \Omega) = 1.083\ \text{k}\Omega$$
$$Z_0 = R_C \,\|\, r_o = 4.3\ \text{k}\Omega \,\|\, 60\ \text{k}\Omega = 4.012\ \text{k}\ \Omega$$

(c)
$$A_V = -\frac{R_C \,\|\, r_o}{r_e} = -\frac{4.012\ \text{k}\Omega}{10.83\ \Omega} = -370.45$$

(e) when
$$r_o = 30\ \text{k}\Omega$$
$$R_C \,\|\, r_o = 4.3\ \text{k}\Omega \,\|\, 30\ \text{k}\Omega = 3.76\ \text{k}\Omega$$
$$A_V = -\frac{3.76\ \text{k}\Omega}{10.83\ \Omega} = -347.18$$

3.19 COMMON EMITTER CONFIGURATION WITH VOLTAGE DIVIDER BIAS

Figure 3.40 shows CE configuration using voltage divider bias.

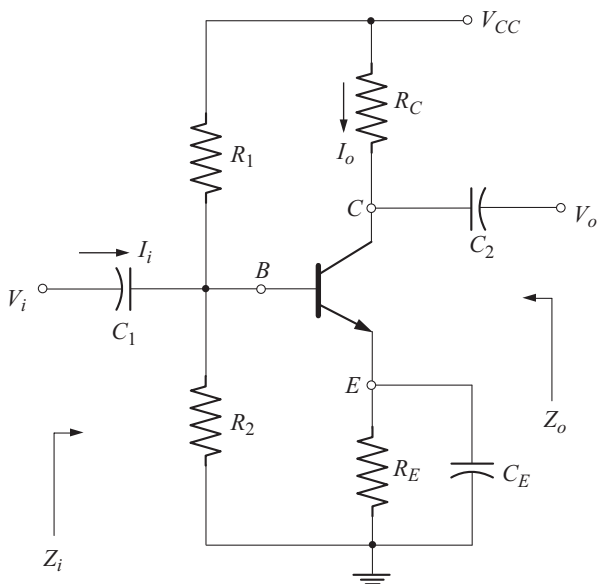


Fig. 3.40 CE configuration using voltage divider bias

The ac input signal V_i is applied to the base of the transistor through the input coupling capacitor C_1. The amplified signal V_o is taken at the collector through the output coupling capacitor C_2. The emitter bypass capacitor C_E is used to prevent the loss of voltage gain due to ac negative feedback through R_E by creating an ac ground at the emitter. C_1, C_2 and C_E are so selected that they represent short circuit even at the lowest frequency of operation.

To perform small signal ac analysis, let us obtain the ac equivalent circuit by reducing V_{CC} to zero and replacing the capacitors C_1, C_2 and C_E by short circuits as shown in Fig. 3.41.

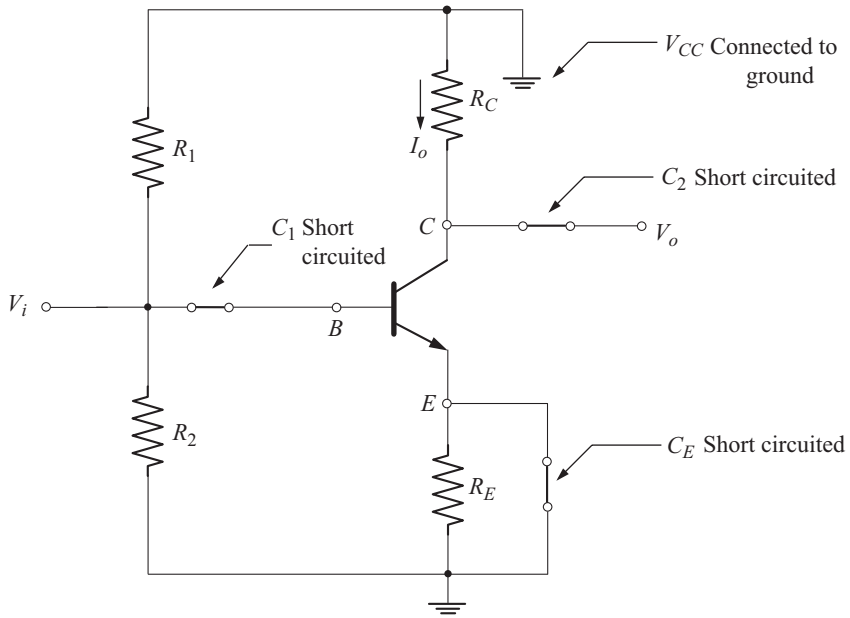


Fig. 3.41 *AC equivalent circuit*

The following observations can be made from Fig. 3.41.

(a) R_1 appears between base and ground. Thus R_1 comes in parallel with R_2.

(b) R_C appears between collector and ground

(c) R_E is in parallel with a short circuit (0 Ω)

$$\therefore \qquad R_E \,||\, 0\ \Omega \ = 0\ \Omega$$

i.e., the equivalent is a short circuit.

The ac equivalent circuit is redrawn in Fig. 3.42.

Note that the emitter terminal is common to input and output circuits. Hence the configuration is common-emitter.

$$\text{Let} \qquad R' \ = \ R_1 \,||\, R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

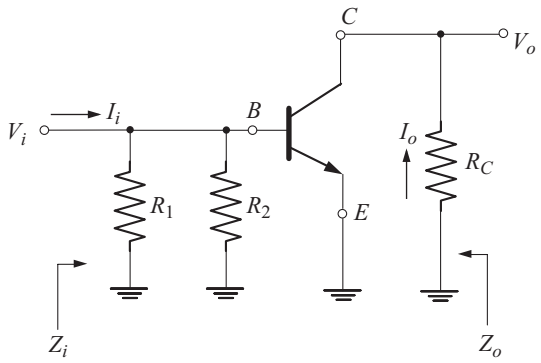


Fig. 3.42 AC equivalent circuit redrawn

The ac equivalent circuit of Fig. 3.42 is an exact duplicate of the equivalent circuit shown in Fig. 3.35 for fixed bias configuration. The only exception is that, R_B is replaced by R'. Therefore, the results derived in the previous section can be readily applied to the circuit under consideration. The results are reproduced here for convenience.

- $$Z_i = \frac{V_i}{I_i} = R' \parallel \beta r_e \tag{3.66}$$
- $$Z_o = r_o \parallel R_C \tag{3.67}$$
- $$A_V = -\frac{r_o \parallel R_C}{r_e} \tag{3.68}$$
- $$A_I = -\frac{A_V Z_i}{R_C} \tag{3.69}$$

For $r_o \geq 10 R_C$

- $$Z_o \approx R_C \tag{3.70}$$
- $$A_V \approx -\frac{R_C}{r_e} \tag{3.71}$$

Negative sign in A_V reveals that, V_i and V_o are 180° out of phase.

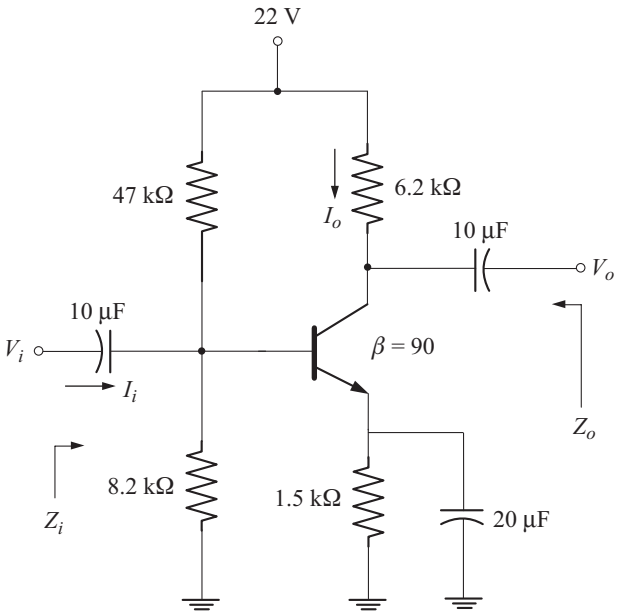
Example 3.7

For the circuit shown below, taking $r_o = \infty\ \Omega$, calculate:

(a) r_e (b) Z_i

(c) Z_o (d) A_V and A_I

(e) Repeat part (b) to (d) with $r_o = \frac{1}{h_{oe}} = 50\ \text{k}\Omega$ and compare the results.



Check for $\beta R_E \geq 10 R_2$

$$\beta R_E = (90)\,(1.5\ \text{k}\Omega) = 135\ \text{k}\Omega$$
$$10 R_2 = (10)(8.2\text{k}\Omega) = 82\ \text{k}\Omega$$

Since $\beta R_E > 10 R_2$, we can use approximate analysis

$$R_{Th} = R' = R_1 \,||\, R_2 = 47\ \text{k}\Omega \,||\, 8.2\ \text{k}\Omega = 6.98\ \text{k}\Omega$$

$$V_B = V_{Th} = \frac{V_{CC}\, R_2}{R_1 + R_2} = \frac{(22\,\text{V})\,(8.2\,\text{k}\Omega)}{47\,\text{k}\Omega + 8.2\,\text{k}\Omega} = 3.268\ \text{V}$$

$$V_{Th} = V_{BE} + V_E \Rightarrow V_E = V_{Th} - V_{BE}$$

$$V_E = 3.268\ \text{V} - 0.7\ \text{V} = 2.568\text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.568\,\text{V}}{1.5\,\text{k}\Omega} = 1.712\ \text{mA}$$

(a) $$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{1.712\,\text{mA}} = 15.18\ \Omega$$

(b) $$Z_i = R' \,||\, \beta\, r_e = (6.98\ \text{k}\Omega) \,||\, (90)\ (15.18\ \Omega) = 1.152\ \text{k}\Omega$$

(c) $$Z_o = r_o \,||\, R_C = (\infty\ \Omega) \,||\, R_C = R_C = 6.2\ \text{k}\Omega$$

(d) $$A_V = -\frac{r_o \,||\, R_C}{r_e} = -\frac{R_C}{r_e} = -\frac{6.2\ \text{k}\Omega}{15.18\ \Omega} = -408.43$$

$$A_I = -\frac{A_V Z_i}{R_C} = -\frac{(-408.43)(1.19\,\text{k}\Omega)}{(6.2\,\text{k}\Omega)} = 78.39$$

(e) When $r_o = 50\ \text{k}\Omega$

Check for $r_o \geq 10\ R_C$

$$10\ R_C = (10)\ (6.2\ \text{k}\Omega) = 62\ \text{k}\Omega$$

Since $r_o < 62\ \text{k}\Omega$, we have to use exact analysis.

$$Z_i = 1.152\ \text{k}\Omega \quad \text{(same as before)}$$

$$Z_o = 50\ \text{k}\Omega \parallel 6.2\ \text{k}\Omega = 5.52\ \text{k}\Omega$$

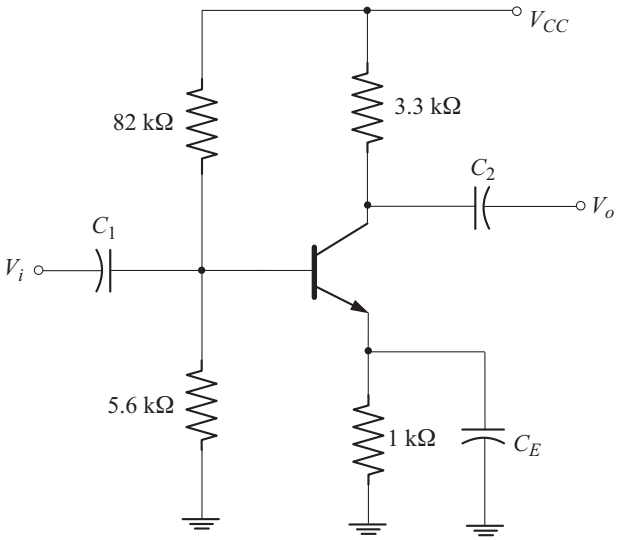
$$A_V = -\frac{5.52\ \text{k}\Omega}{15.18\ \Omega} = -363.64$$

$$A_I = -\frac{(-363.64)(1.152\ \text{k}\Omega)}{(6.2\ \text{k}\Omega)} = 67.56$$

There is a considerable difference in the values of Z_o, A_V and A_I since the condition $r_o \geq 10\ R_C$ is not satisfied.

Example 3.8

For the circuit shown below determine V_{CC} if $A_V = -160$ and $r_o = 100\ \text{k}\Omega$. Take $\beta = 100$



Solution

$$A_V = -\frac{r_o \parallel R_C}{r_e}$$

$$-160 = -\frac{100\ \text{k}\Omega \parallel 3.3\ \text{k}\Omega}{r_e}$$

$$r_e = 19.96\ \Omega$$

$$r_e = \frac{26\,\text{mV}}{I_E} \quad \Rightarrow \quad I_E = \frac{26\,\text{mV}}{r_e}$$

$$I_E = \frac{26\,\text{mV}}{19.96\,\Omega} = 1.3\ \text{mA}$$

$$V_{Th} = V_{BE} + I_E R_E = 0.7\ \text{V} + (1.3\text{mA})(1\ \text{k}\Omega) = 2\text{V}$$

$$V_{Th} = \frac{V_{CC} R_2}{R_1 + R_2} \quad \Rightarrow \quad V_{CC} = \frac{V_{Th}(R_1 + R_2)}{R_2}$$

$$V_{CC} = \frac{(2\ \text{V})(82\ \text{k}\Omega + 5.6\ \text{k}\Omega)}{5.6\ \text{k}\Omega} = 31.2\ \text{V}$$

3.20 COMMON-EMITTER CONFIGURATION USING EMITTER-BIAS WITH UNBYPASSED R_E

Figure 3.43 shows CE configuration using emitter–bias. Note that the emitter resistor R_E is unbypassed.

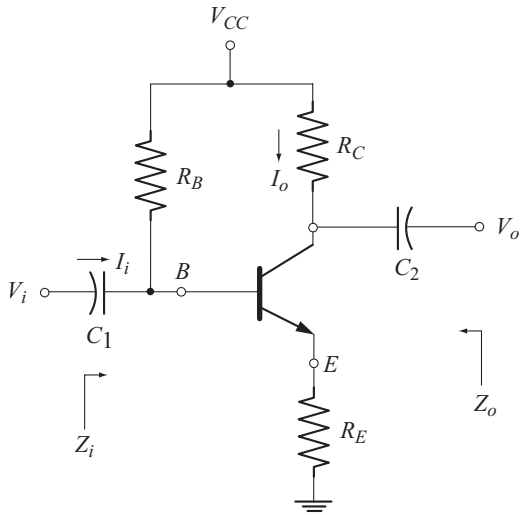


Fig. 3.43 CE configuration with emitter bias

The ac equivalent circuit is drawn by reducing V_{CC} to zero and replacing C_1 and C_2 by short circuit equivalent as shown in Fig. 3.44.

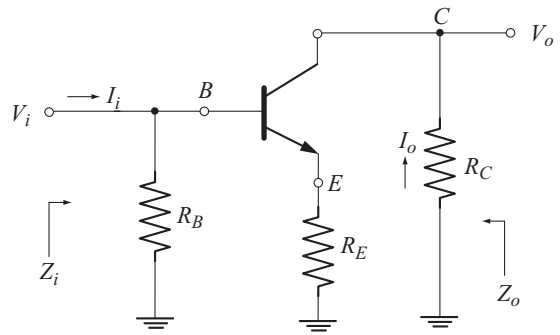


Fig. 3.44 AC equivalent circuit

Let us replace the transistor by its common-emitter r_e model as shown in Fig. 3.45. To simplify the analysis, r_o is not included in the model.

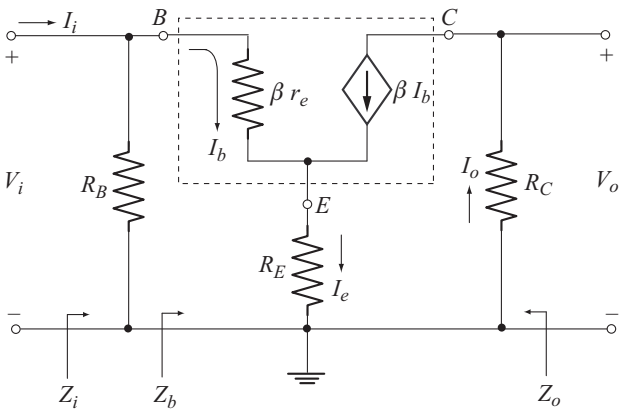


Fig. 3.45 AC equivalent circuit using r_e model

Input Impedance (Z_b)

Applying KVL to the input circuit of Fig. 3.45 we have

$$V_i = I_b \beta r_e + I_e R_E \tag{3.72}$$

using

$$I_e = (1+\beta) I_b$$

$$V_i = I_b \beta r_e + (1+\beta) I_b R_E$$

The input impedance looking into the network to the right of R_B (i.e., excluding R_B) is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (1+\beta) R_E \tag{3.73}$$

Since $\beta >> 1$, $\quad (1+\beta) \approx \beta$

$$\therefore \qquad Z_b \approx \beta r_e + \beta R_E$$

$$\text{or} \qquad Z_b = \beta (r_e + R_E) \tag{3.74}$$

Usually $r_e \ll R_E$.

Now Equation (3.74) can be further reduced to

$$Z_b \approx \beta R_E \tag{3.75}$$

Input Impedance (Z_i)

Z_i takes the effect of R_B into account. It is given by the parallel combination of R_B and Z_b as shown in Fig. 3.46.

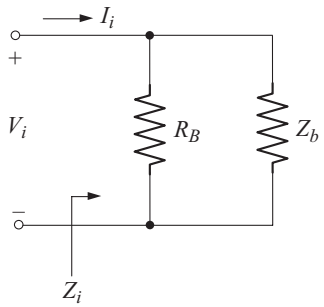


Fig. 3.46 Determining Z_i

$$Z_i = \frac{V_i}{I_i} = R_B \parallel Z_b \tag{3.76}$$

Output Impedance (Z_o)

To find Z_o, we have to set V_i to zero. With $V_i = 0$, $I_b = 0$ and therefore $\beta I_b = 0$. Thus the controlled current source can be replaced by an open circuit as shown in Fig. 3.47.

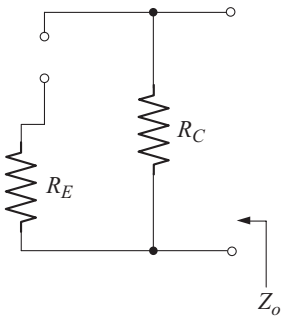


Fig. 3.47 Circuit to find Z_0

From Fig. 3.47 we find that Z_o is given by the parallel combination of R_C and ∞ ohms (open circuit).

$$Z_o = R_C \parallel \infty\ \Omega$$
$$Z_o = R_C \tag{3.77}$$

Voltage Gain (A_V)

$$V_o = -I_o R_C$$
$$= -\beta I_b R_C$$

From Equation (3.73),

$$I_b = \frac{V_i}{Z_b}$$

$$\therefore \quad V_0 = -\beta \left(\frac{V_i}{Z_b}\right) R_C$$

$$A_V = \frac{V_o}{V_i}$$

$$= -\frac{\beta R_C}{Z_b} \tag{3.78}$$

Using, $Z_b = \beta(r_e + R_E)$ we have

$$A_V = -\frac{R_C}{r_e + R_E} \tag{3.79}$$

Taking, $r_e + R_E \approx r_e$ we get

$$A_V \approx -\frac{R_C}{R_E} \tag{3.80}$$

Note that A_V is β independent. As a result the voltage gain is independent of transistor, which is a desirable feature.

Current Gain (A_I)

$$I_o = -\frac{V_o}{R_C}$$

and $$I_i = \frac{V_i}{Z_i}$$

Now $$A_I = \frac{I_o}{I_i}$$

$$= -\left[\frac{V_0}{R_C}\right] \div \left[\frac{V_i}{Z_i}\right]$$

$$= -\left[\frac{V_0}{V_i}\right]\left[\frac{Z_i}{R_C}\right]$$

$$A_I = -\frac{A_V Z_i}{R_C} \tag{3.81}$$

Effect of Unbypassed R_E

Following are the effects of unbypassed R_E on the performance parameters of the amplifier.

- The input impedance increases by βR_E
- Voltage gain decreases
- Voltage gain is independent of β. Thus voltage gain is independent of the transistor and it depends only on the external components R_C and R_E. It means that voltage gain is stabilized.

The reason for these results is that, there is an ac negative feedback through R_E.

Phase Relationship

The negative sign in equation for A_V reveals that V_i and V_o are 180° out of phase.

◆ 3.21 CE EMITTER BIAS CONFIGURATION WITH BYPASSED R_E

Figure 3.48 shows CE emitter bias configuration with R_E bypassed by an emitter bypass capacitor C_E.

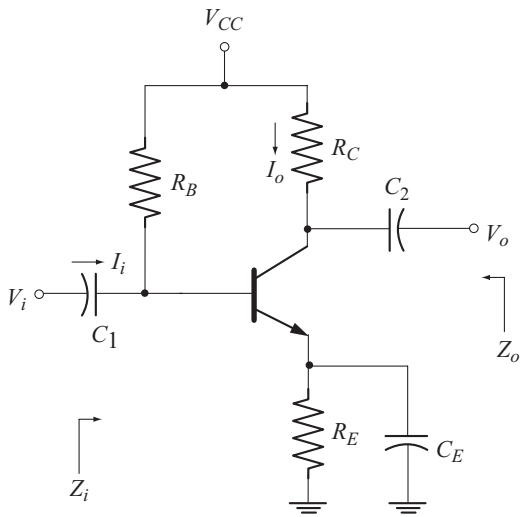


Fig. 3.48 CE emitter bias configuration with bypassed R_E

The ac equivalent circuit is shown in Fig. 3.49. Note that this ac equivalent circuit is an exact replica of that shown in Fig. 3.34, written for CE fixed bias configuration. Hence all the results derived in section 3.18 for CE fixed bias configuration can be readily applied to this circuit.

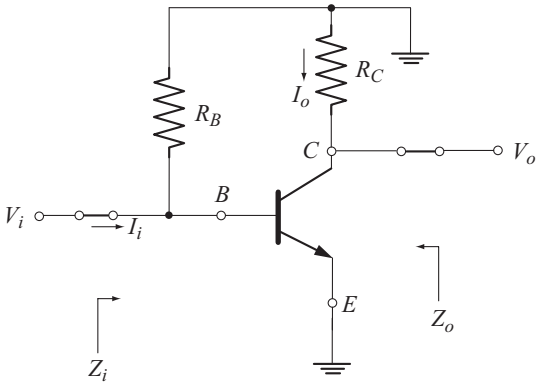


Fig. 3.49 *AC equivalent circuit*

Example 3.9

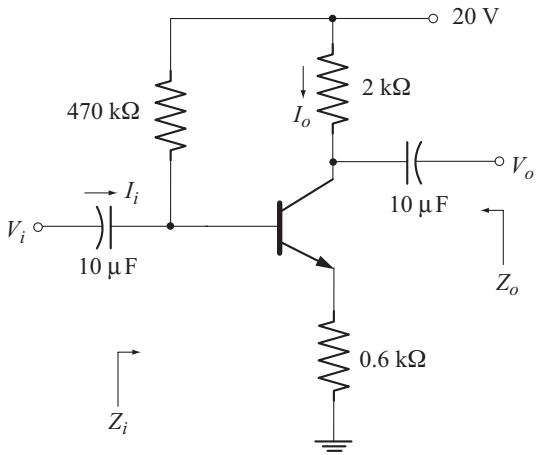
For the circuit shown below calculate

(a) r_e (b) Z_i

(c) Z_o (d) A_V

(e) A_I

Take $\beta = 120$ and $r_o = 40$ kΩ



Solution

(a)

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$= \frac{20\,\text{V} - 0.7\,\text{V}}{470\,\text{k}\Omega + (121)(0.6\,\text{k}\Omega)} = 35.57\ \mu\text{A}.$$

$$I_E = (1 + \beta)\, I_B = (121)\,(35.57\ \mu\text{A}) = 4.3\ \text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{4.3\,\text{mA}} = 6.04\ \Omega$$

(b) $$Z_b = \beta\,(R_E + r_e) = 120\,(600\ \Omega + 6.04\ \Omega) = 72.72\ \text{k}\Omega$$

Now $$Z_i = Z_b \,||\, R_B = 72.72\ \text{k}\Omega \,||\, 470\ \text{k}\Omega = 62.98\ \text{k}\Omega$$

(c) $$Z_o \approx R_C = 2\ \text{k}\Omega$$

(d) $$A_V \approx -\frac{\beta\, R_C}{Z_b} = -\frac{(120)(2\ \text{k}\Omega)}{(72.72\ \text{k}\Omega)} = -3.3$$

(e) $$A_I = -\frac{A_V\, Z_i}{R_C} = -\frac{(-3.3)(62.98\ \text{k}\Omega)}{2\ \text{k}\Omega} = 103.92.$$

Note : If R_E is bypassed by C_E

- r_e remain unchanged since C_E does not affect dc conditions.
- In the calculations of Z_b, Z_i, A_V and A_I, we have to substitute $R_E = 0\ \Omega$, since R_E will be shorted out by C_E.

3.22 COMMON–EMITTER CONFIGURATION USING VOLTAGE DIVIDER BIAS WITH UNBYPASSED R_E

Figure 3.50 shows common-emitter configuration using voltage divider bias with unbypassed R_E. The ac equivalent circuit is shown in Fig. 3.51. Note that this ac equivalent circuit is exactly identical to that given in Fig. 3.44 with R_B equal to the parallel combination of R_1 and R_2. Hence the analysis given in section 3.20 can be readily applied to this circuit.

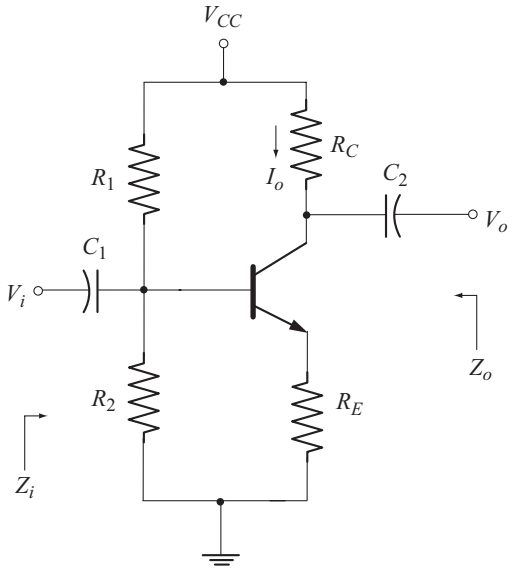


Fig. 3.50 CE Voltage divider configuration with un bypassed R_E

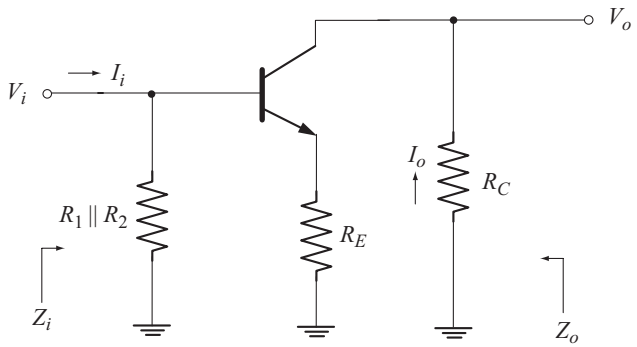


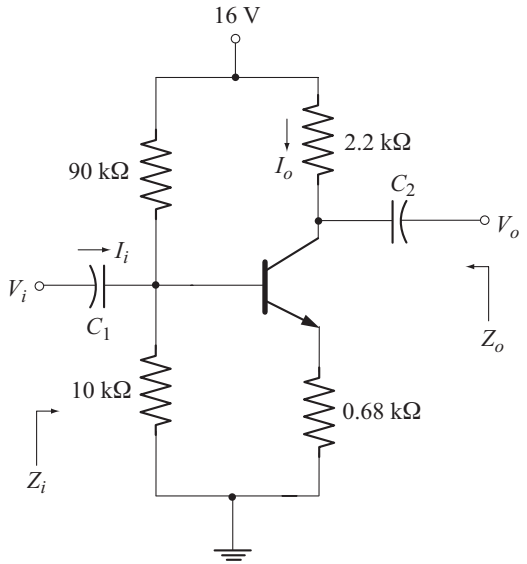
Fig. 3.51 *AC equivalent circuit*

Example 3.10

For the circuit shown below calculate

(a) r_e, Z_i and Z_o (b) A_V and A_I

Take $\beta = 210$ and $r_o = 50$ kΩ.



Solution

Using approximate analysis for voltage divider bias (**since $\beta R_E > 10 R_2$**) we get

$$I_E = 1.324 \text{ mA}$$

(a)
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{1.324\,\text{mA}} = 19.64\ \Omega.$$

$$R_B = R_{Th} = R'$$
$$= R_1 \parallel R_2 = 90\ \text{k}\Omega \parallel 10\ \text{k}\Omega = 9\ \text{k}\Omega$$
$$Z_b \approx \beta(r_e + R_E) = 210\ (19.64\ \Omega + 0.68\ \text{k}\Omega) = 146.92\ \text{k}\Omega$$
$$Z_i = Z_b \parallel R_B = 146.92\ \text{k}\Omega \parallel 9\ \text{k}\Omega = 8.48\ \text{k}\Omega$$
$$Z_o = R_C = 2.2\ \text{k}\Omega$$

(b)
$$A_V \approx -\frac{R_C}{r_e + R_E} = -\frac{2.2\ \text{k}\Omega}{19.64\ \Omega + 0.68\ \text{k}\Omega} = -3.14$$
$$A_I = -\frac{A_V Z_i}{R_C} = -\frac{(-3.14)(8.48\ \text{k}\Omega)}{(2.2\,\text{k}\Omega)} = 12.1$$

3.23 VOLTAGE DIVIDER BIAS AND EMITTER BIAS CONFIGURATIONS WITH PARTLY BYPASSED R_E

Figure 3.52 shows emitter-bias configuration with partly bypassed R_E. The voltage divider bias configuration with partly bypassed R_E is shown in Fig. 3.53.

For dc operation, C_E acts as an open circuit. Hence the emitter resistance for dc analysis (i.e., for the calculation of r_e) is $R_E = R_{E_1} + R_{E_2}$.

For ac operation, R_{E_2} is shorted out by C_E. Hence for ac analysis (i.e., to calculate Z_i, A_V etc) the emitter resistance is, $R_E = R_{E_1}$.

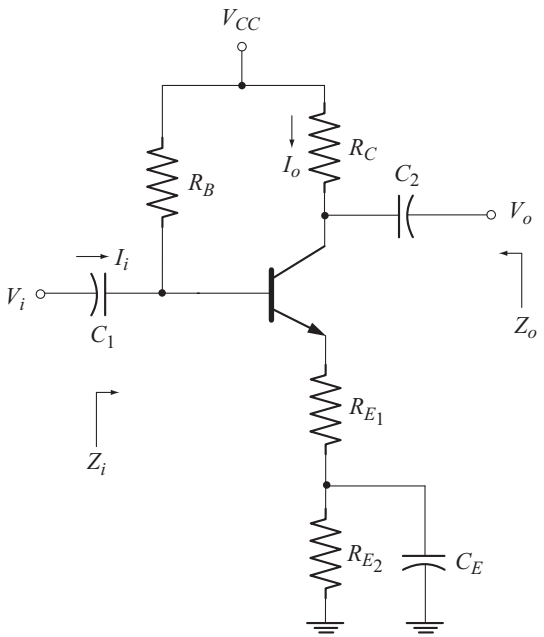


Fig. 3.52 Emitter-bias configuration with partly bypassed R_E

For both the circuits, analysis given in section 3.20 can be used. It is important to note that, for voltage divider configuration we have to take

$$R_B = R_{Th} = R' = R_1 \parallel R_2$$

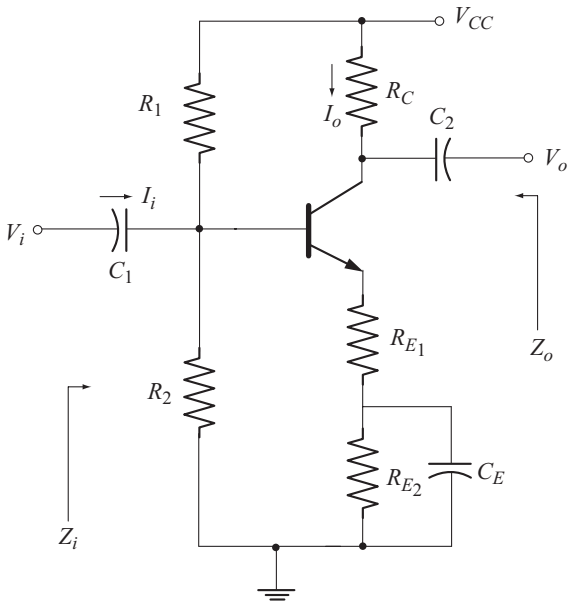


Fig. 3.53 Voltage divider-bias configuration with partly bypassed R_E

◆ 3.24 EMITTER-FOLLOWER CONFIGURATION

Figure 3.54 shows the circuit of emitter-follower configuration.

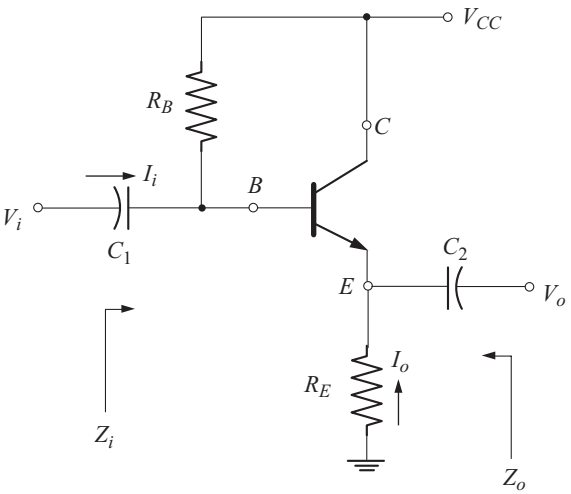


Fig. 3.54 Emitter-follower configuration

The input signal V_i is applied to the base of transistor through the input coupling capacitor C_1. The output signal V_o is taken at the emitter through the output coupling capacitor C_2.

Let us draw the ac equivalent circuit by reducing V_{CC} to zero and replacing the capacitors C_1 and C_2 by their short circuit equivalents as shown in Fig. 3.55.

Observe that the collector terminal is common to input and output circuits. Hence the configuration is common collector. The ac input voltage V_i is the sum of ac base-emitter voltage V_{be} and ac output voltage V_o.

$$\text{ie.} \qquad V_i = V_{be} + V_o$$

Neglecting V_{be} we can write

$$V_o \approx V_i \tag{3.82}$$

The output voltage (emitter voltage) follows the input voltage (base voltage). Hence the name emitter follower.

From Equation (3.82) we have

$$A_V = \frac{V_o}{V_i} \approx 1 \tag{3.83}$$

Thus for emitter follower the voltage gain is approximately unity.

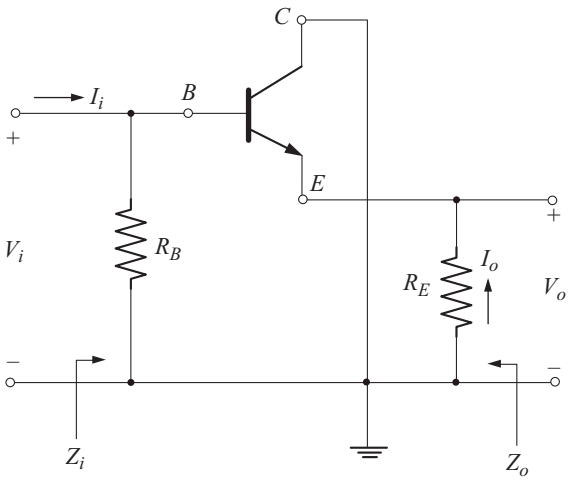


Fig. 3.55 *AC equivalent circuit*

Let us replace the transistor in the circuit of Fig. 3.55 by its r_e model as shown in Fig. 3.56. Note that r_o is not considered for simplicity.

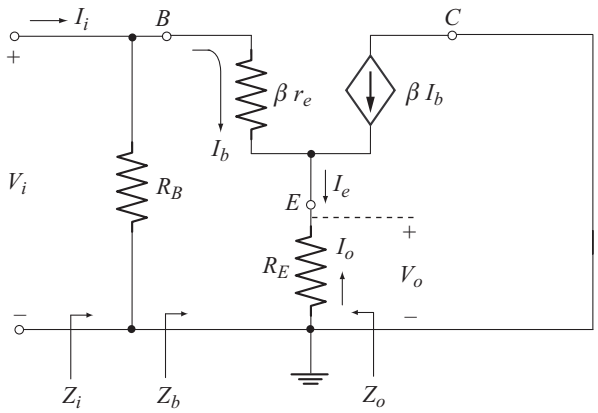


Fig. 3.56 AC equivalent circuit with r_e model

Input Impedance **(Z_i)**

Applying KVL to the input circuit we have

$$V_i = I_b \beta r_e + I_e R_E$$

Using $I_e = (1 + \beta) I_b$ we have

$$V_i = I_b \beta r_e + (1 + \beta) I_b R_E$$

Now
$$Z_b = \frac{V_i}{I_b} = \beta r_e + (1 + \beta) R_E \tag{3.84}$$

$$Z_i = \frac{V_i}{I_i} = R_B \parallel Z_b \tag{3.85}$$

Since $(1 + \beta) \approx \beta$, Equation (3.84) becomes

$$Z_b \approx \beta(r_e + R_E) \tag{3.86}$$

Taking $r_e + R_E \approx R_E$, we can write

$$Z_b \approx \beta R_E \tag{3.87}$$

Output Impedance **(Z_o)**

Consider
$$Z_b = \frac{V_i}{I_b} \quad \Rightarrow \quad I_b = \frac{V_i}{Z_b}$$

Using
$$I_b = \frac{I_e}{1+\beta} \quad \text{we have}$$

$$\frac{I_e}{1+\beta} = \frac{V_i}{Z_b}$$

$$I_e = \frac{(1+\beta) V_i}{Z_b}$$

Substituting for Z_b from Equation (3.84) we have

$$I_e = \frac{(1+\beta)V_i}{\beta r_e + (1+\beta)R_E} \tag{3.88}$$

$$(1 + \beta) \approx \beta$$

$$\beta r_e + (1 + \beta) R_E \approx \beta (r_e + R_E)$$

Using these relations in Equation (3.88) we have

$$I_e \approx \frac{\beta V_i}{\beta (r_e + R_E)}$$

$$V_i \approx I_e (r_e + R_E)$$

or
$$V_i \approx I_e r_e + I_e R_E \tag{3.89}$$

Equation (3.89) is KVL equation and its circuit representation is shown in Fig. 3.57. From Fig. 3.57 we note that $I_e R_E$ gives the output voltage V_o.

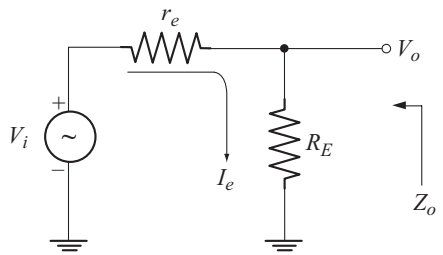


Fig. 3.57 Circuit representation of Equation (3.89)

To find Z_o let us set V_i to zero. The resulting circuit is shown in Fig. 3.58.

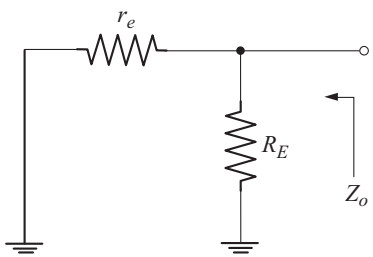


Fig. 3.58 Circuit to find Z_o

Since r_e and R_E are in parallel we have

$$Z_o = r_e \,||\, R_E = \frac{r_e R_E}{r_e + R_E} \tag{3.90}$$

Taking $r_e + R_E \approx R_E$, we get

$$Z_o \approx \frac{r_e R_E}{R_E}$$

or $$Z_o \approx r_e \tag{3.91}$$

Voltage Gain (A_V)

Applying voltage division rule to the circuit of Fig. 3.57 we have

$$V_o = \frac{R_E}{r_e + R_E} V_i$$

Now $$A_V = \frac{V_o}{V_i} = \frac{R_E}{r_e + R_E} \tag{3.92}$$

Usually $R_E \gg r_e$ $\quad \therefore \quad R_E + r_e \approx R_E$

$$A_V = \frac{V_o}{V_i} \approx 1 \tag{3.93}$$

or $$V_o \approx V_i$$

Note that the output voltage follows the input voltage as stated earlier.

Current Gain (A_I)

$$V_o = I_e R_E = -I_o R_E \qquad [\because I_e = -I_o]$$

$$\therefore \quad I_o = -\frac{V_o}{R_E}$$

Also $$I_i = \frac{V_i}{Z_i}$$

Now $$A_I = \frac{I_o}{I_i}$$

$$= \left[-\frac{V_o}{R_E}\right] \div \left[\frac{V_i}{Z_i}\right]$$

$$= -\left[\frac{V_o}{V_i}\right]\left[\frac{Z_i}{R_E}\right]$$

$$A_I = -\frac{A_V Z_i}{R_E} \tag{3.94}$$

Phase Relationship

The positive sign for A_V in Equation (3.93) reveals that V_o and V_I are in phase.

Note : r_o has no significant effect on ac analysis.

3.24.1 Important Characteristics of Emitter Follower

Based on the results obtained, we can list the following important characteristics of emitter follower.

- The input impedance is high.
- The output impedance is low.
- The voltage gain is approximately unity.
- The input and output voltages are in phase.
- The current gain is high.

Since emitter follower presents a high impedance at the input and a low impedance at the output it is used for impedance matching purposes. It is used as a buffer between the voltage source of high source impedance and a low impedance load.

◆ 3.25 EMITTER FOLLOWER USING VOLTAGE DIVIDER BIAS

Figure 3.59 shows an emitter follower using voltage divider bias. The ac analysis given in section 3.24 can also be used for this circuit, simply by replacing R_B by $R_1 \| R_2$.

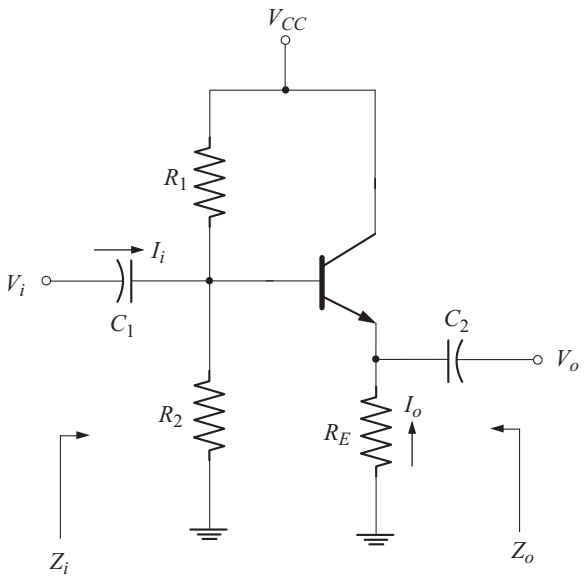


Fig. 3.59 Emitter follower using voltage divider bias

◆ 3.26 EMITTER FOLLOWER USING COLLECTOR RESISTOR

Figure 3.60 shows the circuit of emitter follower using collector resistor R_C. The presence of R_C affects only the dc operation of the circuit. Since R_C is not reflected into the base or emitter equivalent networks the ac analysis given in section 3.24 can be applied to this circuit simply by replacing R_B by $R_1 \| R_2$. It is important to note that since the addition of R_C does not affect I_E, the value of r_e remains unchanged. Only V_{CE} will get affected.

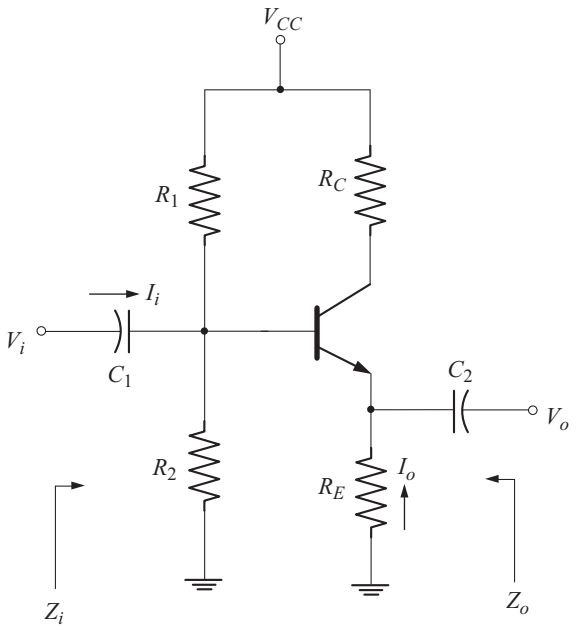


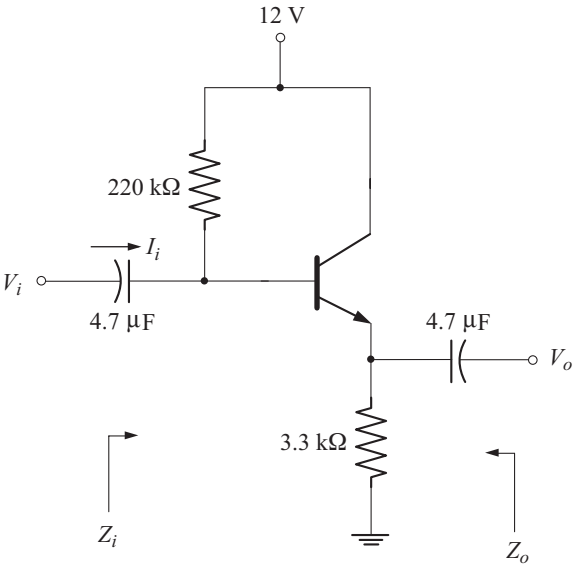
Fig. 3.60 Emitter follower using collector resistor

Example 3.11

For the emitter follower shown below calculate

(a) r_e (b) Z_i and Z_o (c) A_V and A_I

Take $\beta = 100$ and $r_o = \infty$.



Solution

(a)
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}$$
$$= \frac{12\text{ V} - 0.7\text{ V}}{220\text{ k}\Omega + (101)(3.3\text{ k}\Omega)} = 20.42\ \mu\text{A}$$
$$I_E = (1 + \beta)\, I_B = (101)\ (20.42\ \mu\text{A}) = 2.062\text{ mA}$$
$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.062\text{ mA}} = 12.61\ \Omega$$

(b)
$$Z_b = \beta\, r_e + (1 + \beta)\, R_E$$
$$= (100)\ (12.61\ \Omega) + (101)\ (3.3\text{ k}\Omega) = 334.56\text{ k}\Omega$$
$$Z_i = R_B \parallel Z_b = 220\text{ k}\Omega \parallel 334.56\text{ k}\Omega = 132.72\text{ k}\Omega$$
$$Z_o = R_E \parallel r_e = 3.3\text{ k}\Omega \parallel 12.61\ \Omega = 12.56\ \Omega$$

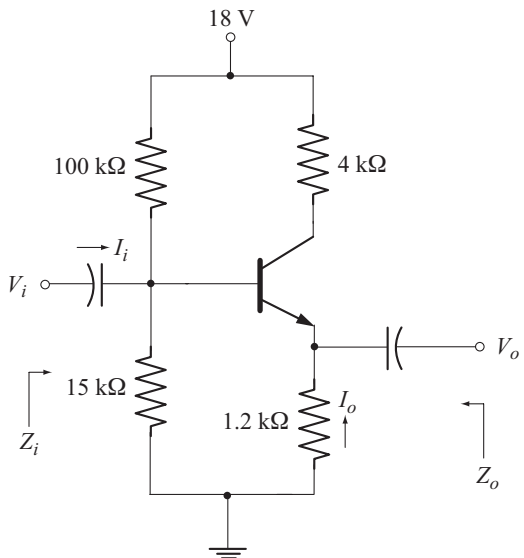
(c)
$$A_V = \frac{R_E}{R_E + r_e} = \frac{3.3\text{ k}\Omega}{3.3\text{ k}\Omega + 12.61\ \Omega} = 0.996$$
$$A_I = -\frac{A_V\, Z_i}{R_E} = -\frac{(0.996)(132.72\text{ k}\Omega)}{(3.3\text{ k}\Omega)} = -40$$

Example 3.12

For the circuit shown below calculate

(a) r_e (b) Z_i and Z_o (c) A_V and A_I

Take $\beta = 100$ and $r_o = 50\text{ k}\Omega$



Solution

(a) Using exact analysis for voltage divider bias circuit (since $\beta R_E < 10 R_2$) we get

$$I_E = 1.23 \text{ mA}$$

$$r_e = \frac{26\text{mV}}{I_E} = \frac{26\text{mV}}{1.23\text{mA}} = 21.13\ \Omega$$

(b)
$$Z_b = \beta (r_e + R_E) = 100\ (21.13\ \Omega + 1.2\ \text{k}\Omega) = 122.11\ \text{k}\Omega$$

$$Z_i = R_B \parallel Z_b$$

$$R_B = 100\ \text{k}\Omega \parallel 15\ \text{k}\Omega = 13.04\ \text{k}\Omega$$

$$Z_i = 13.04\ \text{k}\Omega \parallel 122.11\ \text{k}\Omega = 11.78\ \text{k}\Omega$$

$$Z_o = R_E \parallel r_e = 1.2\ \text{k}\Omega \parallel 21.13\ \Omega = 20.76\ \Omega$$

(c)
$$A_V = \frac{R_E}{r_e + R_E} = \frac{1.2\ \text{k}\Omega}{21.13\ \Omega + 1.2\ \text{k}\Omega} = 0.983$$

$$A_I = -\frac{A_V Z_i}{R_E} = -\frac{(0.983)(11.78\ \text{k}\Omega)}{(1.2\ \text{k}\Omega)} = -9.65$$

◆ 3.27 COMMON-BASE CONFIGURATION

Figure 3.61 shows the circuit of common-base configuration.

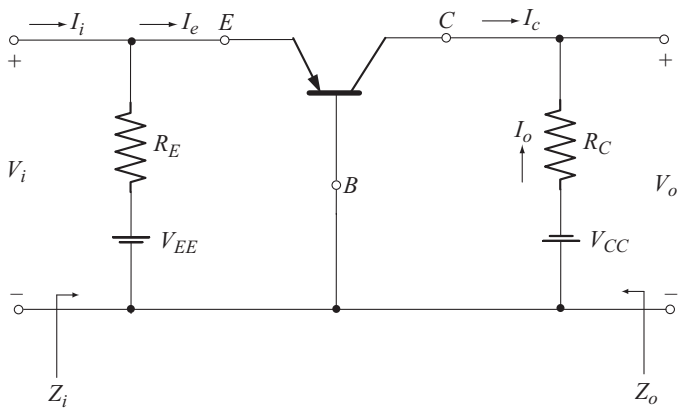


Fig. 3.61 Common-base configuration

The ac equivalent circuit is drawn in Fig. 3.62 by replacing the transistor with its r_e equivalent model. The output impedance r_o of the transistor in CB configuration is typically in the mega ohm range. Hence it is ignored in parallel with R_C.

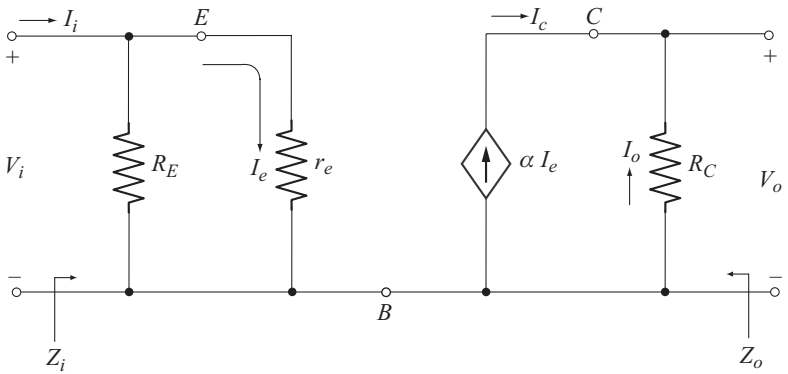


Fig. 3.62 AC equivalent circuit with r_e model

Input Impedance (Z_i)

From the ac equivalent circuit of Fig. 3.62 we find that Z_i is given by the parallel combination of R_E and r_e.

$$Z_i = \frac{V_i}{I_i} = R_E \parallel r_e \tag{3.95}$$

Since $r_e \ll R_E$

$$Z_i \approx r_e \tag{3.96}$$

Output Impedance (Z_o)

To find Z_o, we have to set $V_i = 0$. with $V_i = 0$, $I_e = 0$ and therefore $\alpha I_e = 0$. Thus the current source should be replaced by its open circuit equivalent as shown in Fig. 3.63.

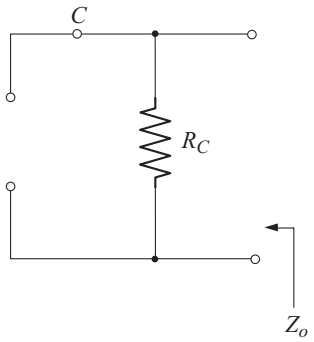


Fig. 3.63 Circuit to find Z_0

From the circuit of Fig. 3.63 we find that

$$Z_o = R_C \tag{3.97}$$

Voltage Gain **(A_V)**

Refer the circuit of Fig. 3.62

$$V_o = -I_o R_C$$
$$= -(-I_c) R_C \qquad (\because I_c = -I_o)$$
$$= I_c R_C$$
$$V_i = I_e r_e$$
$$= \frac{I_c}{\alpha} r_e \qquad (\because I_c = \alpha I_e)$$

Now
$$A_V = \frac{V_o}{V_i}$$
$$= [I_c R_C] \div \left[\frac{I_c r_e}{\alpha}\right]$$
$$A_V = \frac{\alpha R_C}{r_e} \tag{3.98}$$
$$A_V \approx \frac{R_C}{r_e} \qquad \text{(Since } \alpha \approx 1\text{)} \tag{3.99}$$

Current Gain **(A_I)**

Since $r_e \ll R_E$, we can take $I_e \approx I_i$

$$I_o = -I_c = -\alpha I_e$$
$$A_I = \frac{I_0}{I_i} = -\frac{\alpha I_e}{I_e}$$
$$A_I = -\alpha \tag{3.100}$$

Since $\alpha \approx 1$, $A_I \approx -1$ (3.101)

Phase Relationship

The positive sign for A_V reveals that, the input voltage V_i and the output voltage V_o are in phase.

Effect of r_o

For the CB configuration, the output resistance $r_o = 1/h_{ob}$ is typically in the megohm range and much larger than the parallel resistance R_C. Hence we can take

$$r_o \| R_C \approx R_C$$

◆ 3.28 IMPORTANT CHARACTERISTICS OF CB CONFIGURATION

Following are the important characteristics of CB configuration.

- Very low input impedance.

$$Z_i = R_E \| r_e \approx r_e$$

- High voltage gain.

$$A_V \approx \frac{R_C}{r_e} \gg 1 \qquad [\text{Since } r_e \ll R_C]$$

- Approximately unity current gain.
- High output impedance, since r_o is typically in the megohm range.
- Input and output voltages are in phase.

3.29 APPLICATIONS OF CB CONFIGURATION

Due to its low input impedance CB amplifier overloads most signal sources. Thus CB amplifier is not used at low frequencies. It is mainly used for high frequency applications (above 10 MHz) where low source impedances are common.

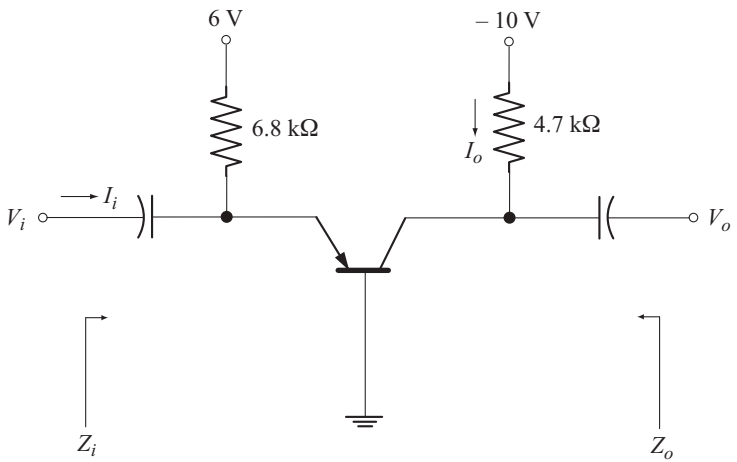
A common base-circuit is also used to couple a low impedance current source to a high impedance load. This application is called impedance matching.

Example 3.13

For the common–base configuration shown below calculate

(a) r_e (b) Z_i and Z_o (c) A_V and A_I

Take $\beta = 499$ and $r_o = 1$ MΩ.



Solution

$$\alpha = \frac{\beta}{1+\beta} = 0.998$$

(a)

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{6\,\text{V} - 0.7\,\text{V}}{6.8\,\text{k}\Omega} = 0.779\ \text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{0.779\,\text{mA}} = 33.38\ \Omega$$

(b) $$Z_i = R_E \parallel r_e = 6.8\ \text{k}\Omega \parallel 33.38\ \Omega = 33.21\ \Omega$$

$$Z_o = R_C = 4.7\ \text{k}\Omega$$

(c) $$A_V = \frac{\alpha R_C}{r_e} = \frac{(0.998)(4.7\ \text{k}\Omega)}{33.38\ \Omega} = 140.52$$

$$A_I = -\alpha = -0.998.$$

◆ 3.30 COLLECTOR FEEDBACK CONFIGURATION

Figure 3.64 shows the circuit of collector feedback configuration. Note that feedback is given from collector to base through R_F to increase the stability of the system.

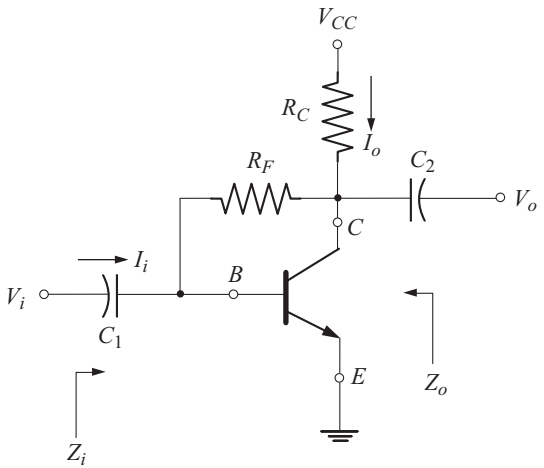


Fig. 3.64 Collector feedback configuration

The ac equivalent circuit is drawn by reducing V_{CC} to zero and replacing C_1 and C_2 by their short circuit equivalents as shown in Fig. 3.65. Note that the configuration is common-emitter since the emitter terminal is present in both input and output circuits.

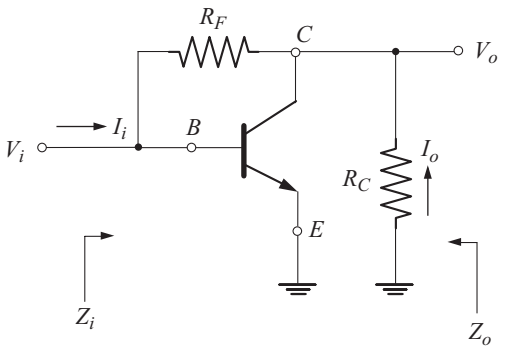


Fig. 3.65 AC equivalent circuit

Let us replace the transistor by its r_e equivalent model as shown in Fig. 3.66. Note that in the r_e model, the output resistance r_o of the transistor is not included, for simplicity.

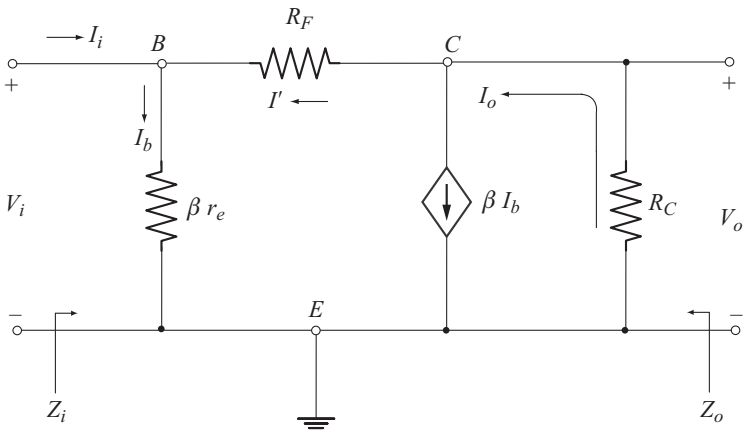


Fig. 3.66 *AC* Equivalent circuit with r_e model

Input Impedance **(Z_i)**

$$V_i = I_b \beta r_e \tag{3.102}$$

Applying KCL at the base node we have

$$I_b = I_i + I' \tag{3.103}$$

$$I' = \frac{V_0 - V_i}{R_F}$$

$$I' = \frac{V_0}{R_F} - \frac{V_i}{R_F} \tag{3.104}$$

$$V_o = -I_o R_C \tag{3.105}$$

Applying KCL at the collector node we have

$$I_o = \beta I_b + I'$$

Usually $\beta I_b \gg I'$

Thus $I_o \approx \beta I_b$

Using this relation in Equation (3.105) we have

$$V_o = -\beta I_b R_C$$

Substituting for I_b from Equation (3.102)

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right) R_C = -V_i \frac{R_C}{r_e}$$

Substituting this relation in Equation (3.104) we have

$$I' = -V_i \frac{R_C}{r_e R_F} - \frac{V_i}{R_F}$$

$$I' = -\frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right] V_i \tag{3.106}$$

Let us substitute this relation in Equation (3.103)

$$I_b = I_i - \frac{1}{R_F}\left[1+\frac{R_C}{r_e}\right] V_i$$

$$\frac{V_i}{\beta r_e} = I_i - \frac{1}{R_F}\left[1+\frac{R_C}{r_e}\right] V_i$$

$$V_i = I_i \beta r_e - \frac{\beta r_e}{R_F}\left[1+\frac{R_C}{r_e}\right] V_i$$

$$V_i\left[1 + \frac{\beta r_e}{R_F}\left[1 + \frac{R_C}{r_e}\right]\right] = I_i \beta r_e$$

Now

$$Z_i = \frac{V_i}{I_i} = \frac{\beta r_e}{1 + \frac{\beta r_e}{R_F}\left[1 + \frac{R_C}{r_e}\right]} \tag{3.107}$$

Usually,

$$R_C \gg r_e \Rightarrow 1 + \frac{R_C}{r_e} \approx \frac{R_C}{r_e}$$

Hence

$$Z_i \approx \frac{\beta r_e}{1 + \frac{\beta R_C}{R_F}}$$

or

$$Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}} \tag{3.108}$$

Output Impedance (Z_o)

To find Z_o, let us set $V_i = 0$. With $V_i = 0$, $I_b = 0$ and hence $\beta I_b = 0$. The circuit to find Z_o is shown in Fig. 3.67.

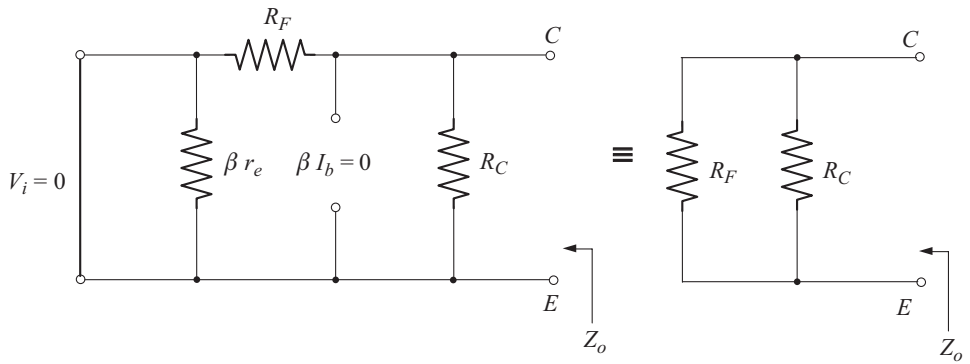


Fig. 3.67 Circuit to find Z_0

Z_o is given by the parallel combination of R_F and R_C

$$\therefore \qquad Z_o = R_F \parallel R_C \tag{3.109}$$

Voltage Gain **(A_V)**

Refer the circuit of Fig. 3.66

$$I_o = \beta I_b + I' \approx \beta I_b \qquad \text{Since } \beta I_b \gg I'$$

$$V_0 = -I_o R_C = -\beta I_b R_C$$

$$V_i = I_b \beta r_e \qquad \text{(From Equation (3.102))}$$

$$A_V = \frac{V_0}{V_i} = -\frac{\beta I_b R_C}{I_b \beta r_e}$$

$$A_V = -\frac{R_C}{r_e} \tag{3.110}$$

Current Gain **(A_I)**

$$V_o = -I_o R_C \quad \Rightarrow \quad I_o = \frac{-V_0}{R_C}$$

$$V_i = I_i Z_i \quad \Rightarrow \quad I_i = \frac{V_i}{Z_i}$$

$$\text{Now} \qquad A_I = \frac{I_o}{I_i} = \frac{-V_o/R_C}{V_i/Z_i}$$

$$= -\frac{V_0}{V_i}\frac{Z_i}{R_C}$$

$$\therefore \qquad A_I = -A_V \frac{Z_i}{R_C} \tag{3.111}$$

Phase Relationship

The negative sign for A_V in Equation (3.110) implies a 180° phase shift between V_o and V_i.

Note : If an emitter resistance R_E which is unbypassed and included in the circuit of Fig. 3.64 the expressions for Z_i and A_V gets modified as follows.

$$\therefore \qquad Z_i = \frac{R_E}{\frac{1}{\beta} + \frac{R_E + R_C}{R_F}}$$

$$Z_o = R_C \parallel R_F \qquad \text{(same as before)}$$

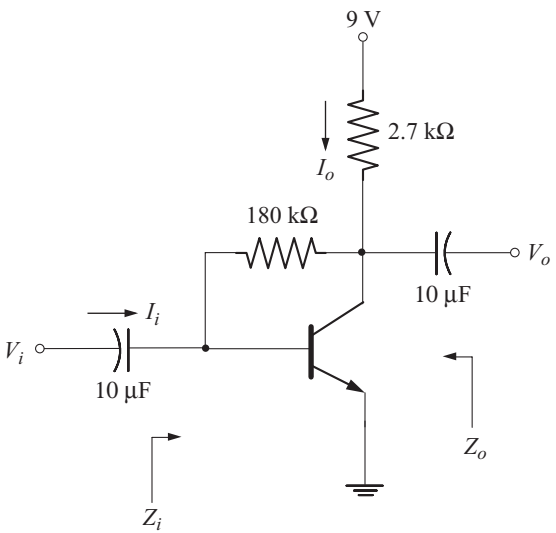
$$A_V = -\frac{R_C}{R_E}$$

Example 3.14

For the circuit shown below calculate

(a) r_e (b) Z_i and Z_o (c) A_V and A_I

Take $\beta = 200$ and $r_o = 60$ kΩ.



Solution

(a)

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{9\text{ V} - 0.7\text{ V}}{180\text{ k}\Omega + (200)(2.7\text{ k}\Omega)}$$

$$= 11.53\ \mu\text{A}$$

$$I_E = (1 + \beta)\, I_B = (201)\,(11.53\ \mu\text{A}) = 2.32\ \text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.32\ \text{mA}} = 11.21\ \Omega$$

(b)
$$Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}} = \frac{11.21\ \Omega}{\frac{1}{200} + \frac{2.7\ \text{k}\Omega}{180\ \text{k}\Omega}} = 560.5\ \Omega$$

$$Z_o = R_C \parallel R_F = 2.7\ \text{k}\Omega \parallel 180\ \text{k}\Omega = 2.66\ \text{k}\Omega$$

(c)
$$A_V = -\frac{R_C}{r_e} = -\frac{2.7\ \text{k}\Omega}{11.21\ \Omega} = -240.86.$$

$$A_I = -\frac{A_V\, Z_i}{R_C} = -\frac{(-240.86)(560.5\ \Omega)}{2.7\ \text{k}\Omega} = 50$$

3.31 COLLECTOR DC FEEDBACK CONFIGURATION

Figure 3.68 shows the circuit of collector dc feedback configuration. For dc operation capacitor C_3 acts as an open circuit. Hence the total dc feedback resistance is $R_{F1} + R_{F2}$. For ac operation C_3 acts as a short circuit. Thus R_{F1} appears on the input side and R_{F2} on the output side. The split feedback resistor arrangement improves the stability of the system.

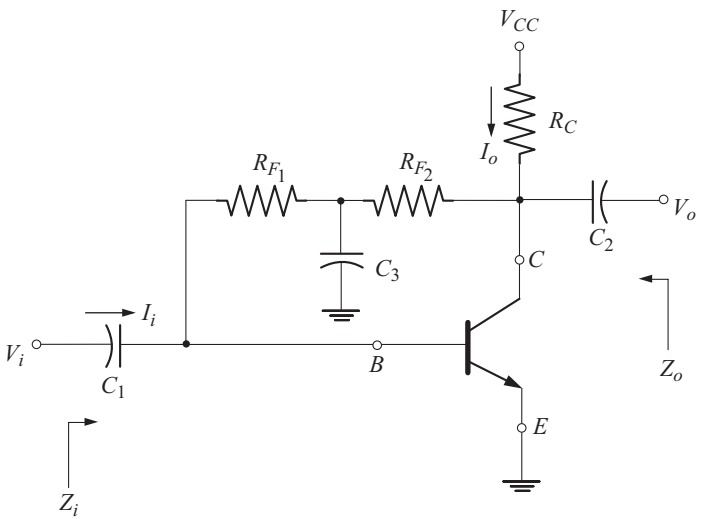


Fig. 3.68 Collector dc fedback configuration

The ac equivalent circuit is drawn by reducing V_{CC} to zero and replacing the capacitors by their short circuit equivalents as shown in Fig. 3.69.

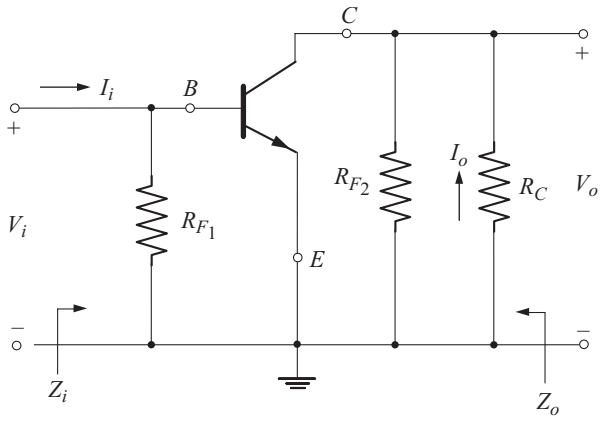


Fig. 3.69 *AC equivalent circuit*

Note that the configuration is common-emitter since the emitter terminal is present in both input and output circuits.

Let us replace the transistor by its r_e model as shown in Fig. 3.70.

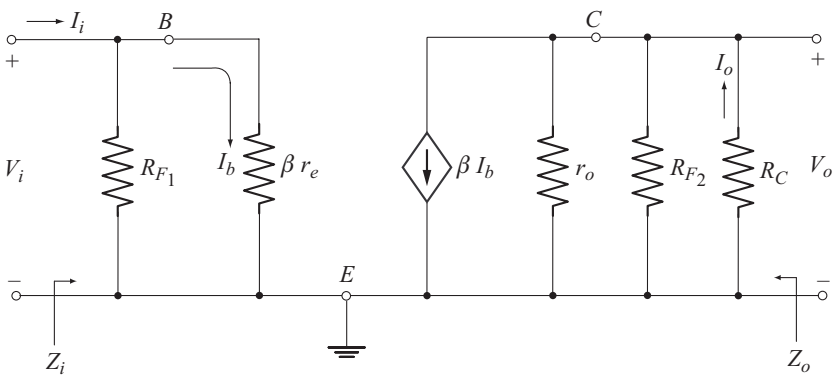


Fig. 3.70 *AC equivalent circuit with* r_e *model*

Input Impedance **(Z_i)**

As seen from the input circuit of Fig. 3.70, Z_i is given by the parallel combination of R_{F_1} and βr_e.

$$\therefore \qquad Z_i = \frac{V_i}{I_i} = R_{F_1} \| \beta r_e \tag{3.112}$$

Output Impedance **(Z_o)**

To find Z_o, let us set $V_i = 0$.

With $V_i = 0$, $I_i = 0$, $I_b = 0$ and therefore $\beta I_b = 0$.

The output equivalent circuit under this condition is shown in Fig. 3.71.

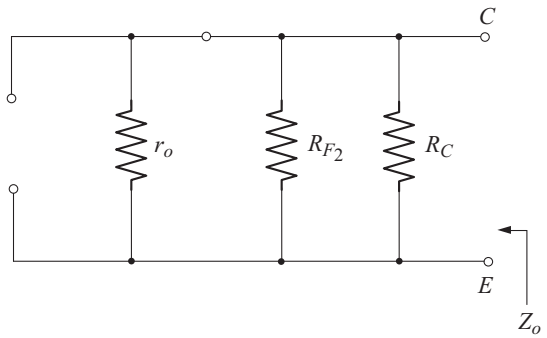


Fig. 3.71 Circuit to find Z_0

$$Z_o = r_o \| R_{F_2} \| R_C \tag{3.113}$$

If $r_o \geq 10\, R_C$, $\quad r_o \| R_C \approx R_C$

$$Z_o \approx R_{F_2} \| R_C \tag{3.114}$$

Voltage Gain **(A_V)**

Refer the circuit of Fig. 3.70.

Let us take,

$$R' = r_o \| R_{F_2} \| R_C \tag{3.115}$$

The simplified output equivalent circuit is shown in Fig. 3.72.

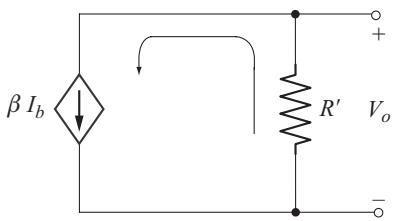


Fig. 3.72 Circuit to find V_o

$$V_o = -\beta I_b R'$$

$$V_i = \beta r_e I_b$$

$$A_V = \frac{V_0}{V_i} = -\frac{\beta I_b R'}{\beta r_e I_b}$$

$$A_V = -\frac{R'}{r_e} \tag{3.116}$$

For $r_o \geq 10\, R_C$, $\quad R' = r_o \| R_{F_2} \| R_C$

$$\approx R_{F_2} \| R_C$$

Now
$$A_V \approx -\frac{R_{F_2} \| R_C}{r_e} \tag{3.117}$$

Current Gain (A_I)

$$V_o = -I_o R_C \quad \Rightarrow \quad I_o = -\frac{V_o}{R_C}$$

$$V_i = I_i Z_i \quad \Rightarrow \quad I_i = \frac{V_i}{Z_i}$$

Now
$$A_I = \frac{I_0}{I_i} = \frac{-(V_0 / R_C)}{(V_i / Z_i)}$$

$$A_I = -A_V \frac{Z_i}{R_C} \tag{3.118}$$

Phase Relationship

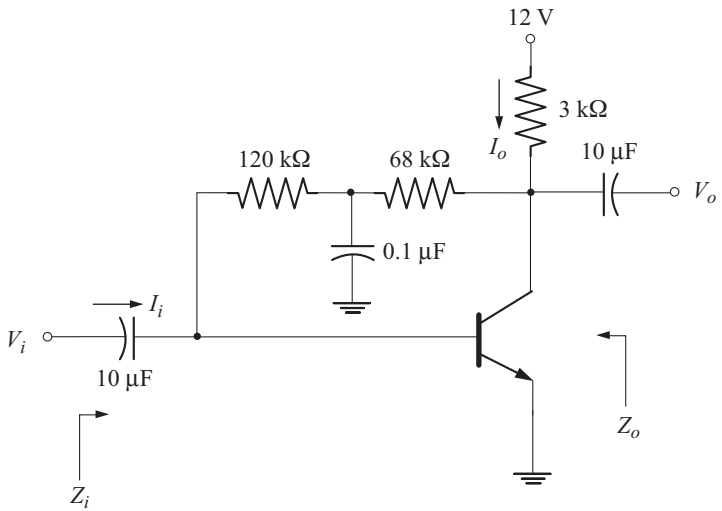
The negative sign for A_V clearly reveals that V_o and V_i are 180° out of phase.

Example 3.15

For the circuit shown below calculate

(a) r_e (b) Z_i and Z_o (c) A_V and A_I

Take $\beta = 140$ and $r_o = 30$ kΩ.



Solution

(a) For dc operation, 0.1 μF capacitor acts as an open circuit.

Thus the total dc feedback resistance is

$$R_F = 120 \text{ k}\Omega + 68 \text{ k}\Omega = 188 \text{ k}\Omega.$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{12\text{ V} - 0.7\text{ V}}{188\text{ k}\Omega + (140)(3\text{ k}\Omega)} = 18.59\ \mu\text{A}$$

$$I_E = (\beta + 1)\, I_B = (141)\,(18.59\ \mu\text{A}) = 2.62\text{ mA}.$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.62\text{ mA}} = 9.92\ \Omega$$

(b)

$$Z_i = R_{F_1} \| \beta r_e = 120\text{ k}\Omega \| (140)\,(9.92\ \Omega) = 1.37\text{ k}\Omega$$

$$Z_o = r_o \| R_{F_2} \| R_C = 30\text{ k}\Omega \| 68\text{ k}\Omega \| 3\text{ k}\Omega = 2.62\text{ k}\Omega$$

(c)

$$A_V = -\frac{r_o \| R_{F_2} \| R_C}{r_e} = -\frac{2.62\text{ k}\Omega}{9.92\ \Omega} = -264.11$$

$$A_I = -\frac{A_V Z_i}{R_C} = -\frac{(-264.11)(1.37\text{ k}\Omega)}{3\text{ k}\Omega} = 120.61$$

◆ 3.32 EFFECTS OF R_S AND R_L

So for we have analyzed amplifiers with out the load resistance R_L and the source resistance R_S. Now let us proceed to analyze the amplifiers considering the effects of R_S and R_L. Now we will define three voltage gains for distinction as given below.

***No Load Voltage Gain* [*Unloaded voltage gain*]**

The no load voltage gain is defined with R_L not connected between the output terminals and with out considering R_S as shown in Fig. 3.73.

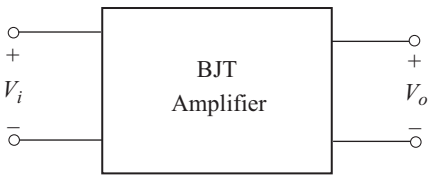


Fig. 3.73 Defining no load voltage gain

The no load voltage gain is given by

$$A_{V_{NL}} = \frac{V_o}{V_i} \tag{3.119}$$

It is important to note that $A_{V_{NL}}$ is exactly identical to A_V determined in the preceding sections. Thus in the subsequent analysis we shall use for $A_{V_{NL}}$, the relations derived earlier for A_V.

Loaded Voltage Gain

The loaded voltage gain is defined with R_L connected between the output terminals and without considering R_S as shown in Fig. 3.74.

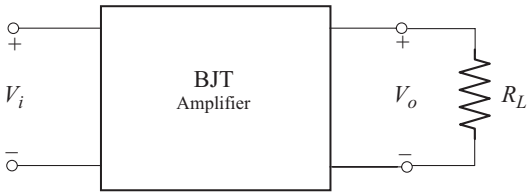


Fig. 3.74 Defining loaded voltage gain

The loaded voltage gain is given by

$$A_V = \frac{V_o}{V_i} \tag{3.120}$$

Though Equations (3.119) and (3.120) seem identical, the difference is that in the latter V_o is measured in the presence of R_L with same V_i.

Loaded Voltage Gain with Source Resistance

The loaded Voltage gain taking R_S into consideration is given by

$$A_{V_S} = \frac{V_o}{V_s} \tag{3.121}$$

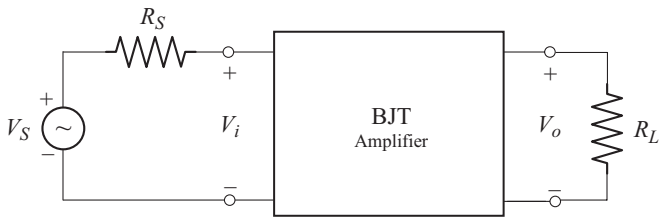


Fig. 3.75 Defining loaded voltage gain with R_s

3.32.1 Methods of Analysis of Amplifiers with R_s and R_L

There are two methods to analyze the amplifier networks with load and/or source resistance.

In the first method the r_e model is used as has been used in the previous sections.

In the second method a two port system approach is used.

First we will consider the r_e model approach.

◆ 3.33 FIXED BIAS COMMON-EMITTER AMPLIFIER WITH R_s AND R_L

Figure 3.76 shows the fixed bias CE amplifier with R_S and R_L. The ac equivalent circuit is drawn by replacing the transistor with its r_e model as shown in Fig. 3.77.

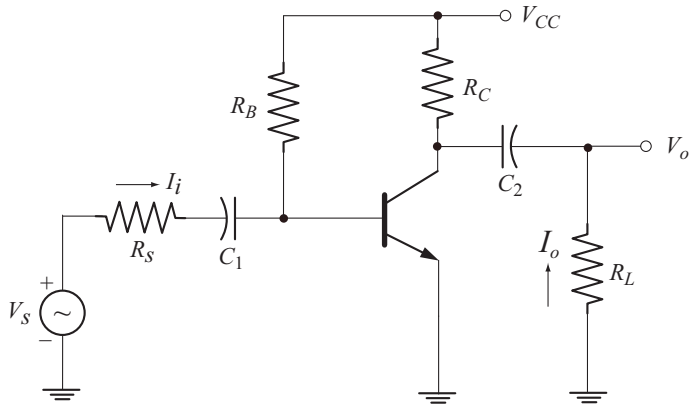


Fig. 3.76 Fixed bias CE configuration with R_s and R_L

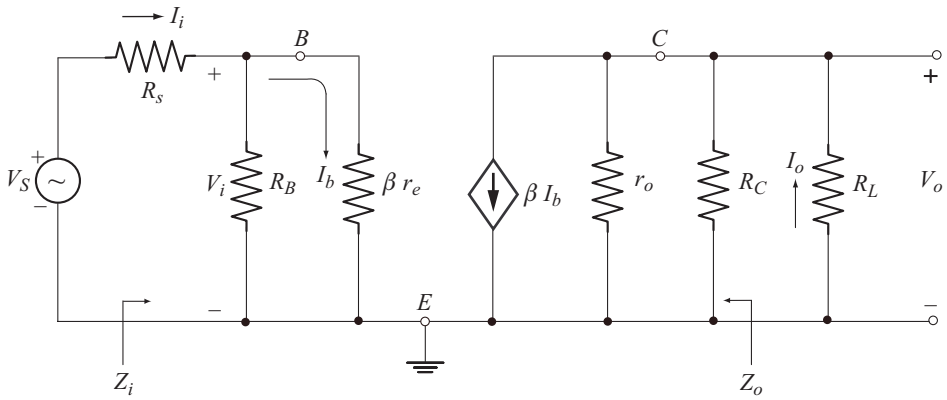


Fig. 3.77 AC equivalent circuit

Input Impedance **(Z_i)**

As seen from the input circuit of Fig. 3.77, the input impedance Z_i, is given by the parallel combination of R_B and $\beta\, r_e$.

$$\therefore \qquad Z_i = \frac{V_i}{I_b} = R_B \,\|\, \beta\, r_e \tag{3.122}$$

which is same as before.

Output Impedance **(Z_o)**

From the output circuit of Fig. 3.77 we find that, the output impedance is given by the parallel combination of r_o and R_C.

$$Z_o = r_o \,\|\, R_C \tag{3.123}$$

as before.

It is important to note that, Z_o does not take R_L into account.

Voltage Gain

Let R_L' represent the parallel combination of r_o, R_C and R_L.

$$\text{Now} \qquad R_L' = r_o \parallel R_C \parallel R_L \tag{3.124}$$

To simplify the analysis let us ignore the effect of r_o.

$$R_L' = R_C \parallel R_L$$

The simplified output equivalent circuit is shown in Fig. 3.78.

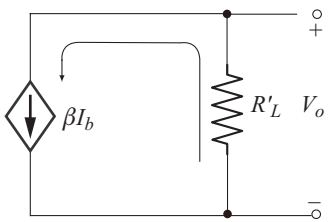


Fig. 3.78 Simplified output equivalent circuit

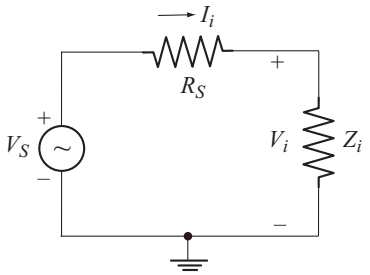


Fig. 3.79 Simplified input equivalent circuit

$$V_o = -\beta I_b R_L' \tag{3.125}$$

From the input circuit of Fig. 3.77

$$V_i = I_b \beta r_e \tag{3.126}$$

$$A_V = \frac{V_o}{V_i}$$

$$= -\frac{\beta I_b R_L'}{I_b \beta r_e}$$

$$A_V = -\frac{R_L'}{r_e} = -\frac{R_C \parallel R_L}{r_e} \tag{3.127}$$

To find A_{V_S} let us consider the input equivalent circuit shown in Fig. 3.79.

Using voltage division rule we have

$$V_i = V_S \frac{Z_i}{R_S + Z_i}$$

or

$$\frac{V_i}{V_S} = \frac{Z_i}{R_S + Z_i} \tag{3.128}$$

$$A_{V_S} = \frac{V_o}{V_S} = \frac{V_o}{V_i} \frac{V_i}{V_S}$$

$$A_{V_S} = A_V \frac{Z_i}{Z_i + R_S} \tag{3.129}$$

The following interesting observations can be made with reference to the voltage gain.

(a) $$A_V = -\frac{R_C \| R_L}{r_e}$$

For an unloaded amplifier, $R_L = \infty\ \Omega$

$$\therefore \quad R_C \| R_L = R_C$$

Thus $$A_{V_{NL}} = -\frac{R_C}{r_e}$$

Since $R_C \| R_L < R_C$, it follows that

$$|A_V| < |A_{V_{NL}}|$$

The loaded voltage gain of an amplifier is always less than the no load voltage gain.

(b) $$A_{V_S} = A_V \frac{Z_i}{R_S + Z_i}$$

Since $\frac{Z_i}{R_S + Z_i} < 1$, it follows that

$$A_{V_S} < A_V$$

The voltage gain obtained with R_S in place will always be less than that obtained under loaded or unloaded conditions.

Thus for the same configuration

$$|A_{V_{NL}}| > |A_V| > |A_{V_S}|$$

In total, the highest gain is obtained under no load condition and the lowest gain with a source impedance and load in place

(c) R_L' increases with increase in R_L. Therefore:

For a particular design, voltage gain increases with increase in R_L.

(d) With smaller R_S, $\frac{Z_i}{R_S + Z_i}$ approaches unity so that

A_{V_S} approaches A_V. Thus:

For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the voltage gain.

***Current Gain* (A_I)**

$$A_I = \frac{I_o}{I_i}$$

$$V_o = -I_o R_L \quad \Rightarrow \quad I_o = -\frac{V_o}{R_L}$$

$$V_i = I_i Z_i \quad \Rightarrow \quad I_i = \frac{V_i}{Z_i}$$

Now
$$A_I = \frac{-(V_o / R_L)}{(V_i / Z_i)}$$

$$= -\left(\frac{V_o}{V_i}\right)\left(\frac{Z_i}{R_L}\right)$$

$$A_I = -A_V \left(\frac{Z_i}{R_L}\right) \tag{3.130}$$

also
$$A_I = -\left.\frac{A_V Z_i}{R_C}\right|_{R_L = \infty}$$

Example 3.16

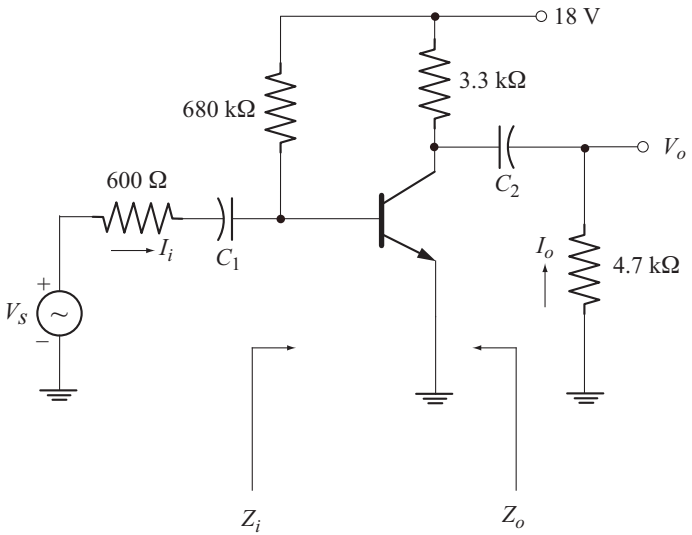
For the fixed bias configuration shown below

(a) Calculate $A_{V_{NL}}$, Z_i and Z_o

(b) Calculate A_V, A_{V_S} and A_I

(c) Calculate V_o if $V_S = 20$ mV

Take $\beta = 100$.



Solution

(a)
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\,\text{V} - 0.7\,\text{V}}{680\,\text{k}\Omega} = 25.44\ \mu\text{A}$$

$$I_E = (1+\beta)\, I_B = (101)\,(25.44\ \mu\text{A}) = 2.57\ \text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.57\,\text{mA}} = 10.116\ \Omega$$

$$A_{V_{NL}} = -\frac{R_C}{r_e} = -\frac{3.3\,\text{k}\Omega}{10.116\,\Omega} = -326.22$$

$$Z_i = R_B \,\|\, \beta\, r_e = 680\ \text{k}\Omega \,\|\, (100)\,(10.116\ \Omega) = 1.01\ \text{k}\Omega$$

$$Z_o = R_C = 3.3\ \text{k}\Omega$$

(b)

$$A_V = -\frac{R_C \| R_L}{r_e} = -\frac{3.3\ \text{k}\Omega\ \|\ 4.7\ \text{k}\Omega}{10.116\ \Omega} = -191.65$$

$$A_{V_S} = A_V \frac{Z_i}{R_S + Z_i} = (-191.65)\left[\frac{1.01\text{k}\Omega}{0.6\text{k}\Omega + 1.01\text{k}\Omega}\right]$$

$$= -120.22$$

$$A_I = -A_V \frac{Z_i}{R_L} = -(-191.65)\,\frac{1.01\ \text{k}\Omega}{4.7\ \text{k}\Omega} = 41.18$$

(c)

$$A_{V_S} = \frac{V_o}{V_s} \quad \Rightarrow \quad V_o = A_{V_S} V_S$$

$$V_o = (-120.22)\ (20\ \text{mV}) = -2.4\ \text{V}$$

◆ 3.34 COMMON-EMITTER VOLTAGE DIVIDER BIAS CONFIGURATION, WITH R_S AND R_L

Figure 3.80 shows CE voltage divider bias configuration with R_S and R_L. Its ac equivalent circuit using r_e model is shown in Fig. 3.81.

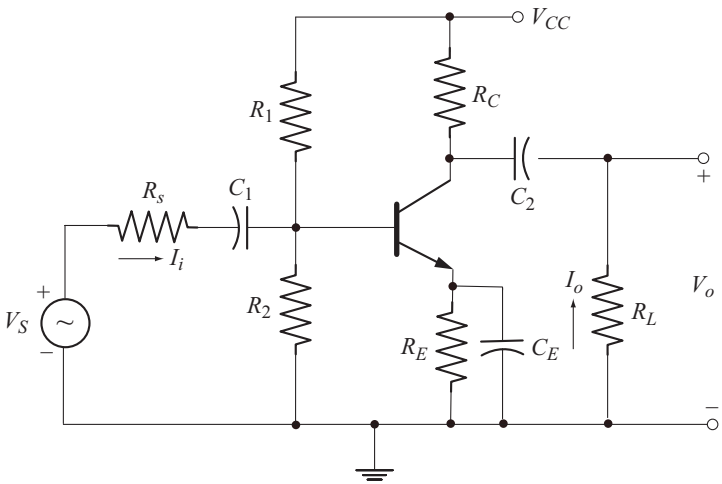


Fig. 3.80 CE voltage divider bias configuration with R_S and R_L

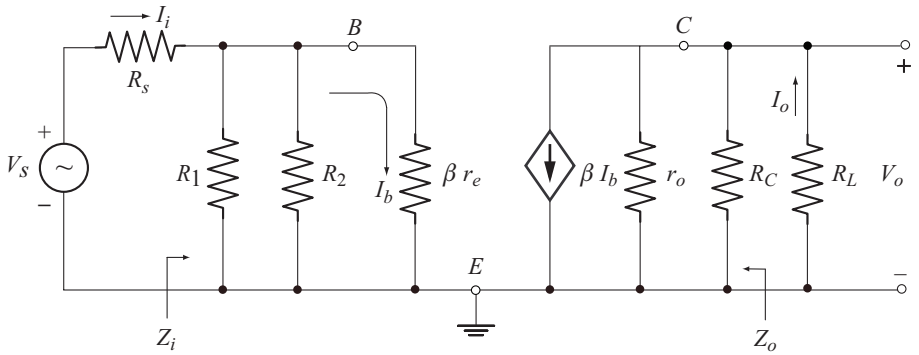


Fig. 3.81 Ac equivalent circuit using r_e model

Following the same procedure given in the previous section we obtain the following results.

- $$Z_i = R' \,||\, \beta r_e$$

  where $$R' = R_1 \,||\, R_2$$

- $$Z_o = r_o \,||\, R_C$$

- $$A_V = -\frac{R_C \,||\, R_L}{r_e}$$

- $$A_{V_{NL}} = -\frac{R_C}{r_e}$$

- $$A_{V_S} = \frac{V_o}{V_S}$$

  $$= A_V \frac{Z_i}{R_S + Z_i}$$

- $$A_I = \frac{I_o}{I_i} = -\frac{A_V Z_i}{R_L}$$

- $$A_I = -\left.\frac{A_V Z_i}{R_C}\right|_{R_L = \infty}$$

3.35 EMITTER-FOLLOWER CONFIGURATION WITH R_s AND R_L

Figure 3.82 shows the emitter-follower configuration with R_S and R_L. Its ac equivalent circuit using r_e model is shown in Fig. 3.83.

To simplify the analysis r_o is not included in the model.

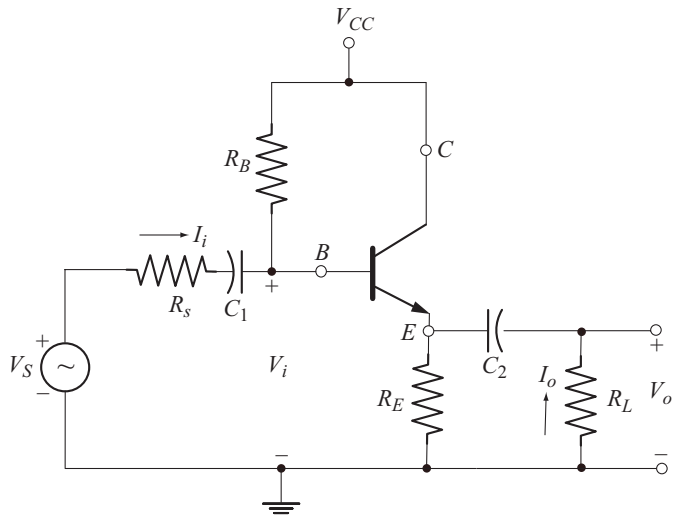


Fig. 3.82 Emitter-follower configuration with R_s and R_L

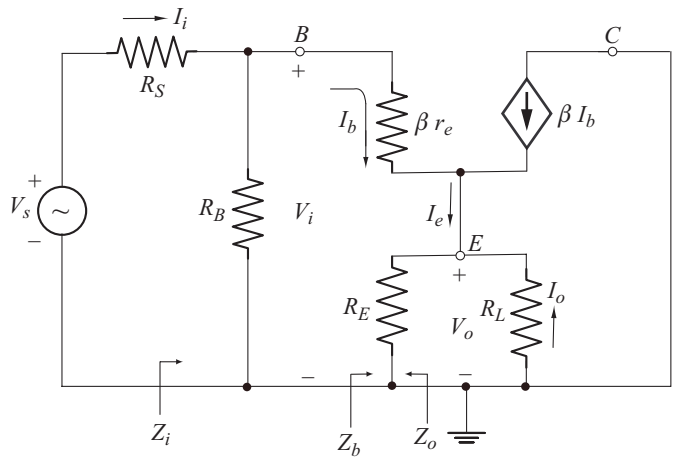


Fig. 3.83 Ac equivalent circuit using r_e model

The analysis given in section 3.24 can be readily applied to this circuit by replacing R_E with $R_E \parallel R_L$ in the equations of Z_b and A_V. The results are given below.

- $$Z_b = \beta r_e + (1+\beta)(R_E \parallel R_L) \approx \beta (R_E \parallel R_L) \quad (3.131)$$
- $$Z_i = R_B \parallel Z_b \quad (3.132)$$
- $$Z_o = r_e \parallel R_E \approx r_e \quad (3.133)$$
- $$A_V = \frac{R_E \parallel R_L}{r_e + R_E \parallel R_L} \quad (3.134)$$

- $$A_{V_{NL}} = \frac{R_E}{r_e + R_E} \tag{3.135}$$
- $$A_{V_S} = A_V \frac{Z_i}{Z_i + R_S} \tag{3.136}$$
- $$A_I = -\frac{A_V Z_i}{R_L} \tag{3.137}$$
- $$A_I = -\frac{A_V Z_i}{R_C}\bigg|_{R_L = \infty}$$

3.36 CE EMITTER-BIAS CONFIGURATION WITH R_S AND R_L

Figure 3.84 shows CE emitter-bias configuration with R_S and R_L. For this circuit the analysis given in section 3.22 can be used by replacing R_C by $R_C \parallel R_L$ in the equation of A_V.

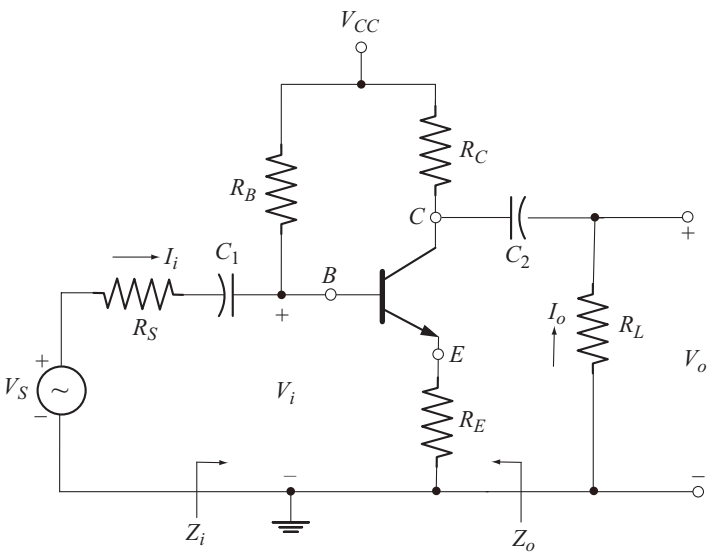


Fig. 3.84 CE emitter-bias configuration with R_S and R_L

The results are as follows:

- $$Z_b = \beta r_e + (1 + \beta) R_E \tag{3.138}$$
- $$Z_i = R_B \parallel Z_b \tag{3.139}$$
- $$Z_o = R_C \tag{3.140}$$
- $$A_V = -\frac{R_C \parallel R_L}{r_e + R_E} \tag{3.141}$$

- $$A_I = -\frac{A_V Z_i}{R_L} \tag{3.142}$$
- $$A_{V_{NL}} = -\frac{R_C}{r_e + R_E} \tag{3.143}$$
- $$A_I = -\frac{A_V Z_i}{R_C}\bigg|_{R_L = \infty} \tag{3.144}$$

3.37 TWO-PORT SYSTEMS APPROACH

In two port system approach the amplifier is represented by a two port network as shown in Fig. 3.85. The parameters of the two port network are the input impedance Z_i, output impedance Z_o and the voltage gain $A_{V_{NL}}$. These parameters are specified for the unloaded condition. Using these results, the gain and impedances can be calculated under loaded conditions.

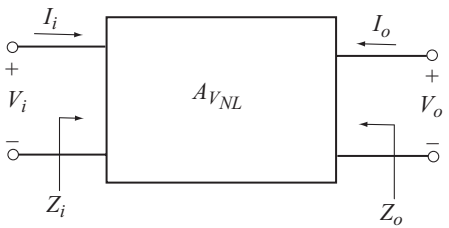


Fig. 3.85 Two – port system

The input Voltage V_i and the input current I_i are related by $V_i = I_i Z_i$. Therefore, between the input terminals, the amplifier can be represented by an impedance Z_i.

Under no load condition

$$A_{V_{NL}} = \frac{V_o}{V_i} \quad \Rightarrow \quad V_o = A_{V_{NL}} V_i$$

Thus at the output side, the amplifier can be represented by a controlled voltage source, $A_{V_{NL}} V_i$. Also it is appropriate to place the output impedance Z_o in series with the controlled voltage source.

The voltage source $A_{V_{NL}} V_i$ in series with the impedance Z_o is referred to as Thevenin equivalent circuit. We oftenly write

$$V_{Th} = A_{V_{NL}} V_i$$

and

$$Z_{Th} = Z_o$$

where V_{Th} is the open circuit voltage or the Thevenin voltage or no load output voltage and Z_{Th} is the Thevenins impedance.

For BJT and FET amplifiers, both Z_o and Z_i are resistive. Thus we represent Z_i by R_i and Z_o by R_o. The two port representation of the amplifier with its internal elements is shown in Fig. 3.86.

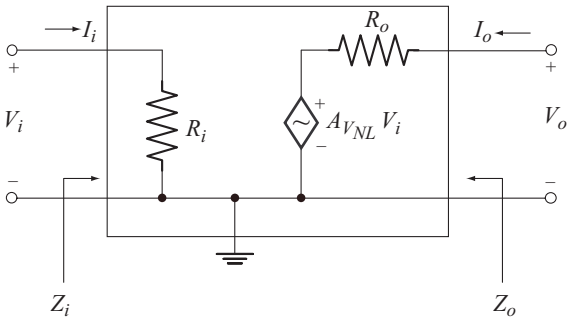


Fig. 3.86 Amplifier represented by two – port system

Now let us justify the placement of the parameters R_o and $A_{V_{NL}}$ in the output circuit. Applying KVL to the output circuit, we have

$$A_{V_{NL}} V_i + I_o R_o - V_o = 0.$$

Under no load condition (output open circuited), $I_o = 0$.

$$\therefore V_o = A_{V_{NL}} V_i = \text{open circuit output voltage.}$$

or

$$A_{V_{NL}} = \frac{V_o}{V_i} = \text{no load or open circuit voltage gain.}$$

To find the output impedance, we set $V_i = 0$. As a result $A_{V_{NL}} V_i = 0$ which represents a short circuit. The resulting circuit is shown in Fig. 3.87.

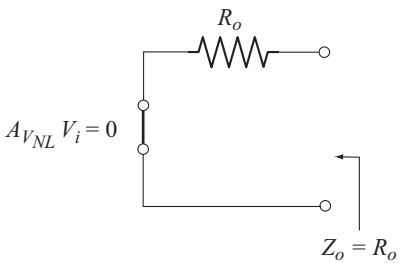


Fig. 3.87 justifying the placement of R_o

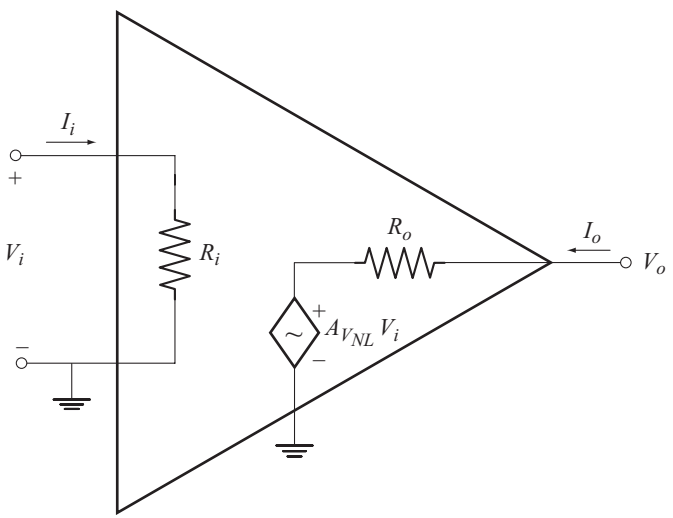


Fig. 3.88 Two port notation for op-amp

The circuit of Fig. 3.87 we find that $Z_o = R_o$ which justifies the placement of R_o.

A second format of two port representation of amplifiers which is popular with op-amps is shown in Fig. 3.88.

◆ 3.38 ANALYSIS OF AMPLIFIERS USING TWO – PORT SYSTEM APPROACH CONSIDERING THE EFFECTS OF R_S AND R_L

Figure 3.89 shows the two port representation of an amplifier driven by a source of internal resistance R_S and supplying the load R_L.

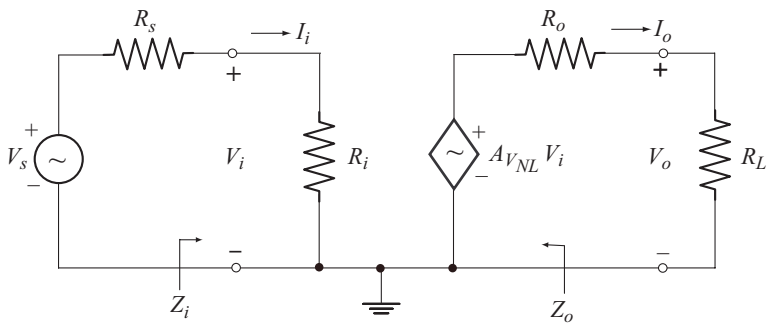


Fig. 3.89 Two - port system with R_s and R_L

Using voltage division rule in the input circuit we have

$$V_i = \frac{R_i}{R_S + R_i} V_S \tag{3.145}$$

or

$$\frac{V_i}{V_S} = \frac{R_i}{R_S + R_i} \tag{3.146}$$

Applying voltage division rule to the output circuit we get

$$V_o = \frac{R_L}{R_o + R_L} A_{V_{NL}} V_i \tag{3.147}$$

or

$$A_V = \frac{V_o}{V_i} = \frac{R_L}{R_o + R_L} A_{V_{NL}} \tag{3.148}$$

The total voltage gain is given by

$$A_{V_S} = \frac{V_o}{V_S}$$

$$= \frac{V_o}{V_i} \frac{V_i}{V_S} \tag{3.149}$$

Substituting Equations (3.146) and (3.148) into Equation (3.149) we have

$$A_{V_S} = \frac{R_i}{R_S + R_i} \cdot \frac{R_L}{R_o + R_L} A_{V_{NL}} \tag{3.150}$$

The current gain is given by

$$A_I = \frac{I_o}{I_i}$$

Using $I_o = -\frac{V_o}{R_L}$ and $I_i = \frac{V_i}{R_i}$ we get

$$A_I = \frac{\left(-V_o/R_L\right)}{\left(V_i/R_i\right)}$$

$$= -\frac{V_o}{V_i} \cdot \frac{R_i}{R_L}$$

$$A_I = -A_V \frac{R_i}{R_L} \tag{3.151}$$

The current gain taking R_S into account is given by

$$A_{I_S} = \frac{I_o}{I_i}$$

But $$I_i = \frac{V_S}{R_S + R_i}$$

$\therefore$ $$A_{I_S} = (-V_o / R_L) \div \frac{V_S}{R_S + R_i}$$

$$= -\frac{V_o}{V_S} \cdot \frac{R_S + R_i}{R_L}$$

$$A_{I_S} = -A_{V_S} \frac{R_S + R_i}{R_L} \tag{3.152}$$

It is important to note that $A_I = A_{I_S}$ when $R_S = 0$

◆ 3.39 ADVANTAGES OF TWO-PORT SYSTEM APPROACH

Now a days the amplifiers are available in the packaged form. Along with the packaged product, the manufacturer supplies the no load values of gain, input and output impedances. Thus the designer can quickly and efficiently find the results for loaded conditions without worrying about the internal components of the package.

Example 3.17

For the circuit of example 3.16

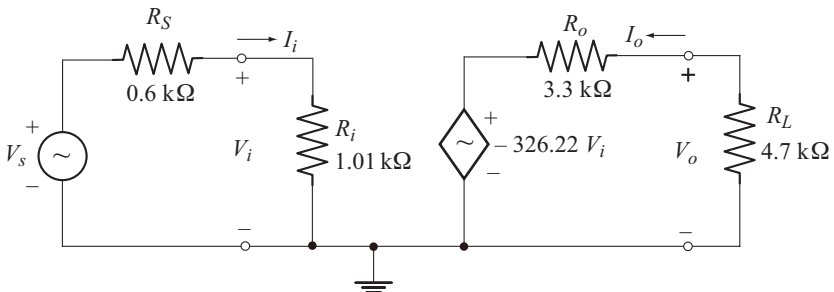
(a) Calculate the parameters of the two port system.
(b) Sketch the two port model
(c) Determine A_V, A_{V_S} and A_I
(d) Calculate A_V, A_{V_S} and A_I when $R_L = 2.7$ kΩ and $R_S = 0.3$ kΩ.

Solution

(a)

$$A_{V_{NL}} = -326.22$$
$$Z_i = R_i = 1.01\ \text{k}\Omega \qquad \text{[as calculated in example 3.16]}$$
$$Z_o = R_o = 3.3\ \text{k}\Omega$$

(b) The two port model is shown below.



(c)
$$A_V = \frac{R_L}{R_o + R_L} A_{V_{NL}}$$
$$= \frac{4.7\,\text{k}\Omega}{3.3\,\text{k}\Omega + 4.7\,\text{k}\Omega}(-326.22) = -191.65$$
$$A_{V_S} = A_V \frac{R_i}{R_S + R_i}$$
$$= (-191.65)\frac{1.01\,\text{k}\Omega}{0.6\,\text{k}\Omega + 1.01\,\text{k}\Omega} = -120.22$$
$$A_I = -A_V \frac{R_i}{R_L} = -(-191.65)\frac{1.01\,\text{k}\Omega}{4.7\,\text{k}\Omega} = 41.18$$

Note that these results agree with those obtained in example 3.16

(d) $R_L = 2.7\ \text{k}\Omega \qquad R_S = 0.3\ \text{k}\Omega.$

$$A_V = (-326.22)\frac{2.7\,\text{k}\Omega}{3.3\,\text{k}\Omega + 2.7\,\text{k}\Omega} = -146.79$$
$$A_{V_S} = (-146.79)\frac{1.01\ \text{k}\Omega}{0.3\ \text{k}\Omega + 1.01\ \text{k}\Omega} = -113.17$$
$$A_I = -(-146.79)\frac{1.01\ \text{k}\Omega}{2.7\ \text{k}\Omega} = 54.91$$

Note: Similarly we can analyse any BJT configuration using two-port system approach, with R_S and R_L.

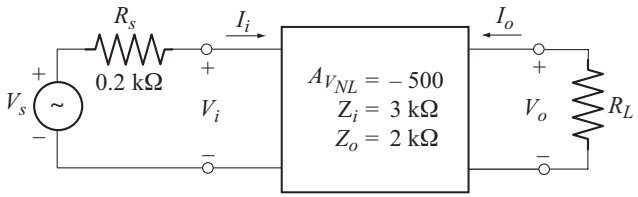
Example 3.18

For the packaged amplifier shown below:

(a) Calculate A_V for R_L = 1.2 kΩ and 5.6 kΩ and compare these values with $A_{V_{NL}}$.

(b) Calculate A_{V_S} with R_L = 1.2kΩ.

(c) Determine A_I with R_L = 5.6 kΩ.



Solution:

(a)
$$A_V = \frac{R_L}{R_o + R_L} A_{V_{NL}}$$

with $R_L = 1.2$ kΩ
$$A_V = \frac{1.2\text{k}\Omega}{2\text{k}\Omega + 1.2\text{k}\Omega}(-500)$$
$$= -187.5$$

with $R_L = 5.6$ kΩ
$$A_V = \frac{5.6\text{k}\Omega}{2\text{k}\Omega + 5.6\text{k}\Omega}(-500)$$
$$= -368.42$$

Note that as R_L decreases, A_V also decreases. It is important to note that $A_V \to A_{V_{NL}}$ for $R_L \gg R_o$.

(b)
$$A_{V_S} = \frac{R_i}{R_S + R_i} A_V$$

with $R_L = 1.2$ kΩ, $A_V = -187.5$
$$A_{V_S} = \frac{3\text{k}\Omega}{0.2\text{k}\Omega + 3\text{k}\Omega}(-187.5)$$
$$= -175.78.$$

Note that $A_{V_S} \to A_V$ for $R_i \gg R_S$.

(c)
$$A_I = -\frac{A_V Z_i}{R_L}$$

with $R_L = 5.6$ kΩ, $A_V = -368.42$
$$A_I = -\frac{(-368.42)(3\text{k}\Omega)}{5.6\text{k}\Omega} = 197.36.$$

Exercise Problems

3.1 A CE fixed bias configuration has R_C = 2 kΩ, R_B = 330 kΩ, β = 100, r_o = 50 kΩ and V_{CC} = 15 V. Calculate Z_i, Z_o, A_V and A_I.

3.2 A CE emitter-bias configuration with unbypassed R_E has R_C = 2.7 kΩ, R_B = 390 kΩ, R_E = 1.2 kΩ, β = 150, r_o = 25 kΩ and V_{CC} = 16 V. Calculate Z_i, Z_o, A_V and A_I.

3.3 The following component values are available for an emitter follower.
R_1 = 62 kΩ, R_2 = 10 kΩ, R_E = 1.5 kΩ, β = 200, r_o = 50 kΩ and V_{CC} = 18 V.
Calculate Z_i, Z_o, A_V and A_I.

3.4 A CB amplifier has R_C = 3.9 kΩ, R_E = 3.3 kΩ, V_{CC} = 9 V, V_{EE} = 4 V, β = 100. Calculate Z_i, Z_o, A_V and A_I.

3.5 A CE collector dc feedback configuration has V_{CC} = 14 V, R_C = 3.3 kΩ, R_{F_1} = 120 kΩ, R_{F_2} = 68 kΩ, β = 140, and r_o = 50 kΩ. Calculate Z_i, Z_o, A_V and A_I.

Chapter 4

TRANSISTOR FREQUENCY RESPONSE

◆ INTRODUCTION

The frequency response of an amplifier is the plot of the magnitude of voltage gain as a function of frequency. In transistor amplifier the low frequency response is governed by the coupling and bypass capacitors. The high frequency response is affected by the transistor parasitic capacitances and the stray wiring capacitances. The mid frequency response is unaffected by these capacitances.

This chapter discusses the effect of coupling and bypass capacitors on low frequency response. The effect of transistor parasitic capacitances and wiring capacitances has also been considered.

◆ 4.1 GENERAL FREQUENCY CONSIDERATIONS

The response of a single stage or multistage amplifier depends on the frequency of the applied signal. The coupling and bypass capacitors affect the low frequency response since the reactance of these capacitors decreases with increase in frequency. The internal capacitances of the active devices (BJT or FET) and the stray wiring capacitances will limit the high frequency response of the system. An increase in the number of stages of a cascaded system will also limit the low and high frequency responses.

4.1.1 Frequency Response of R-C Coupled Amplifier

The frequency response of an amplifier is the plot of the magnitude of voltage gain as a function of frequency. Figure 4.1 shows the frequency response of R-C coupled amplifier.

The scale on horizontal axis is a logarithmic scale to facilitate the plot extending from the low to the high frequency regions.

The frequency range is divided into three regions

- Low frequency region
- Mid frequency region
- High frequency region.

The drop in the gain at low frequencies is due to the coupling capacitors (C_C and C_S) and bypass capacitors (C_E).

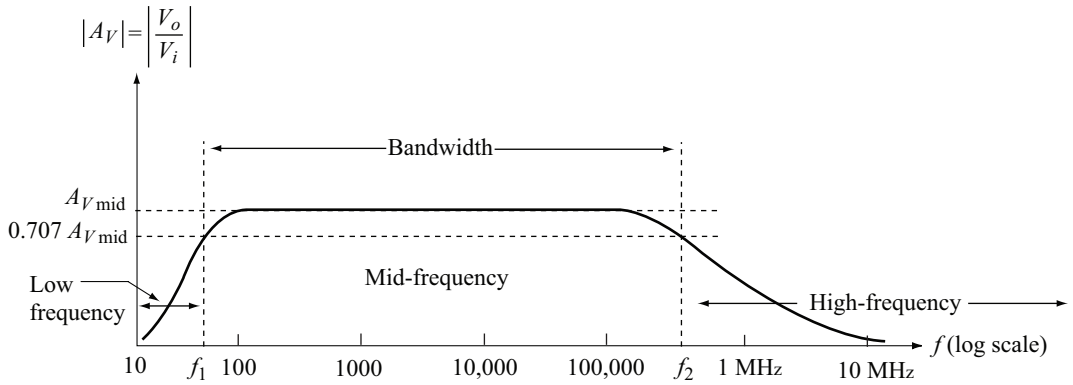


Fig. 4.1 Frequency response of R-C coupled amplifier

At high frequencies the drop in gain is due to the internal device capacitances and the stray wiring capacitances.

In the mid frequency range the gain is almost independent of the frequency. This is due to the fact that at mid frequencies the coupling and bypass capacitors act as short circuits and the device and stray wiring capacitances act as open circuits due to their low capacitance. The mid band gain is denoted by $A_{V\,\text{mid}}$.

4.1.2 Frequency Response of Transformer Coupled Amplifier

Figure 4.2 shows the frequency response of transformer coupled amplifier.

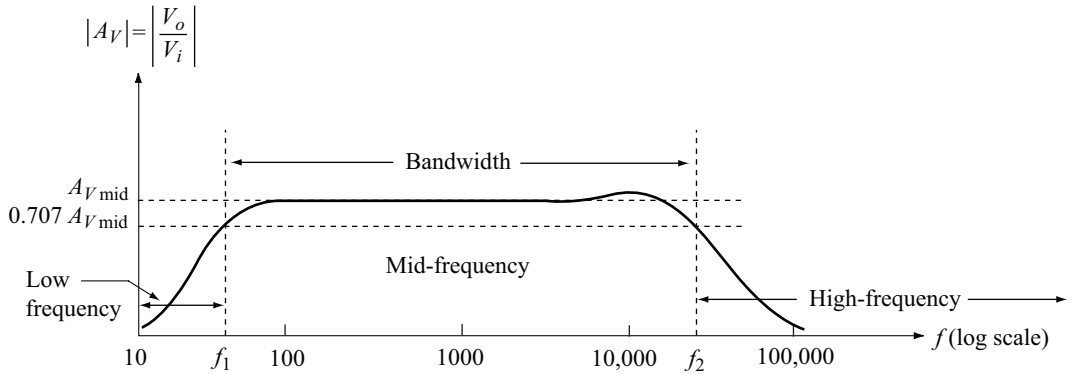


Fig 4.2 Frequency response of transformer coupled amplifier

The magnetising inductive reactance of the transformer winding is $X_L = 2\,\pi\,f\,L$.

At low frequencies the gain drops due to the small value of X_L. At $f = 0$ (DC) there is no change in flux in the core. As a result the secondary induced voltage or output voltage is zero and hence the gain.

At high frequencies the gain drops due to the stray capacitance between the turns of primary and secondary windings.

4.1.3 Frequency Response of Direct Coupled Amplifier

Figure 4.3 shows the frequency response of direct coupled amplifier.

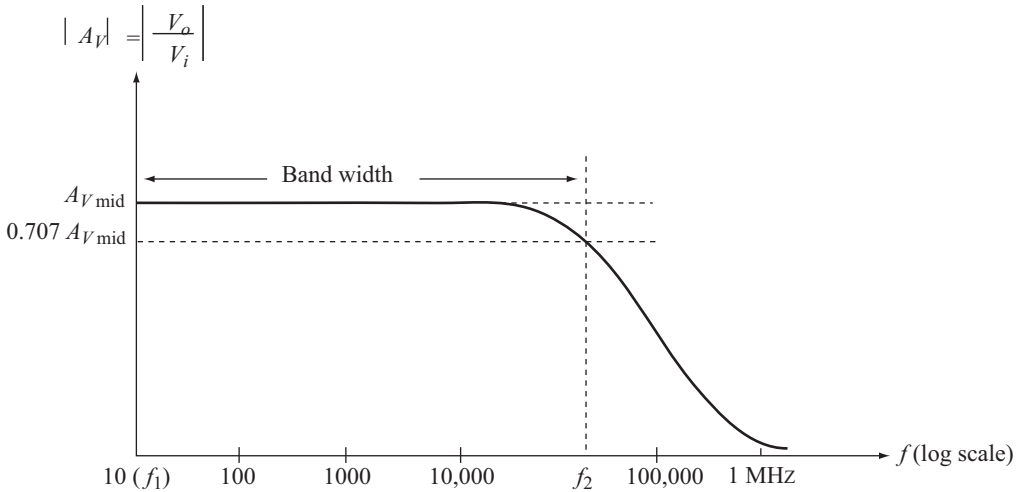


Fig. 4.3 Frequency response of direct coupled amplifier

Direct coupled amplifier do not use coupling and bypass capacitors. As a result there is no drop in gain at low frequencies. The frequency response curve is flat upto the upper cutoff frequency.

Gain drops at high frequencies due to the device internal capacitances and the stray wiring capacitances.

4.1.4 Half Power Frequencies and Band Width

The frequencies f_1 and f_2 at which the gain is 0.707 $A_{V\,\text{mid}}$ are called cut-off frequencies or corner frequencies or break frequencies. f_1 is called the lower cut-off frequency and f_2 the upper cut-off frequency.

The band width or the pass band of the amplifier is given by

$$\text{Band width,} \qquad BW = f_2 - f_1 \tag{4.1}$$

The output voltage in the mid band is

$$|V_o| = |A_{V\,\text{mid}}|\ |V_i|$$

Output power in the mid band is

$$P_{o\,(\text{mid})} = \frac{|V_o|^2}{R_o} = \frac{|A_{V\,\text{mid}}|^2\,|V_i|^2}{R_o} \tag{4.2}$$

The output voltage at cut-off frequencies is

$$|V_o| = |0.707\,A_{V\,\text{mid}}|\,|V_i|$$

and the output power at cut-off frequencies is

$$P_{o\,(\text{cut-off})} = \frac{|0.707 A_{V\,\text{mid}}|^2 |V_i|^2}{R_o}$$

$$= 0.5 \frac{|A_{V\,\text{mid}}|^2 |V_i|^2}{R_o}$$

or $$P_{o\,(\text{cut-off})} = 0.5\, P_{o\,(\text{mid})} \tag{4.3}$$

Note that the output power at cut-off frequencies is half the mid band power output. For this reason f_1 and f_2 are also called the half power frequencies. More specifically f_1 is called the lower half-power frequency and f_2 the upper half power frequency.

4.1.5 Normalised Gain versus Frequency Plot

The normalized gain is obtained by dividing the gain A_V at each frequency by the mid band gain $A_{V\,\text{mid}}$. Therefore

$$\text{Normalised gain} = \frac{A_V}{A_{V\,\text{mid}}} \tag{4.4}$$

Figure 4.4 shows the normalized gain versus frequency plot for an RC-coupled amplifier. Note that:

- The normalised mid band gain is $\frac{A_{V\,\text{mid}}}{A_{V\,\text{mid}}} = 1$ and
- The normalised gain at cut-off frequencies is $\frac{0.707 A_{V\,\text{mid}}}{A_{V\,\text{mid}}} = 0.707$.

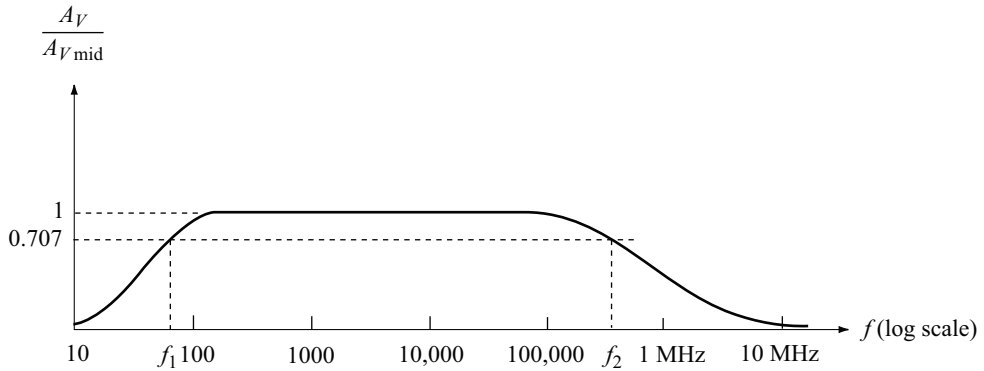


Fig. 4.4 Normalised gain versus frequency plot

In communication applications such as audio and video it is more useful to plot the normalised decibel voltage gain versus frequency rather than the normalised voltage gain versus frequency.

Normalised decibel voltage gain is

$$\left.\frac{A_V}{A_{V\,\text{mid}}}\right|_{dB} = 20 \log_{10}\left[\frac{A_V}{A_{V\,\text{mid}}}\right] \tag{4.5}$$

Normalised decibel voltage gain in mid band is

$$20 \log_{10}\left[\frac{A_{V\,\text{mid}}}{A_{V\,\text{mid}}}\right] = 0$$

Normalised decibel voltage gain at cut-off frequencies is

$$20 \log_{10}\left[\frac{0.707 A_{V\,\text{mid}}}{A_{V\,\text{mid}}}\right] = -3 \text{ dB}.$$

Note that normalised decibel voltage gain at cut-off frequencies is 3dB less than the normalised decibel midband voltage gain. For this reason the frequencies f_1 and f_2 are also called the 3 dB frequencies. More specifically f_1 is called the lower 3 dB frequency and f_2 the upper 3 dB frequency.

Figure 4.5 shows the plot of normalised decibel voltage gain versus frequency for an RC-coupled amplifier.

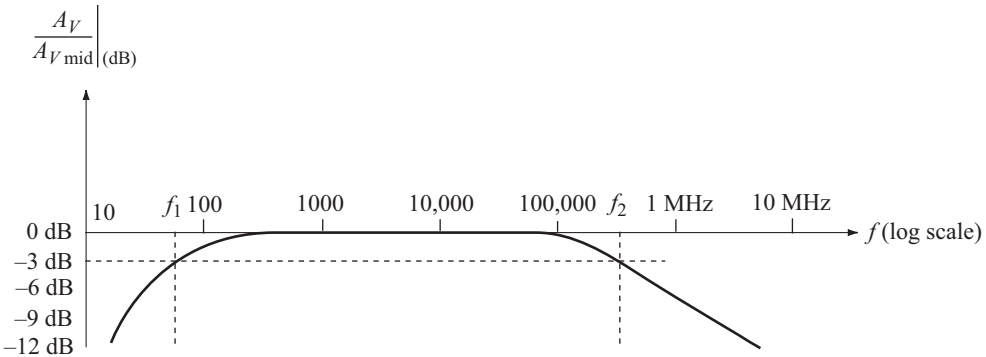


Fig. 4.5 Plot of normalised decibel voltage gain versus frequency

4.1.6 Phase Angle Plot

A single stage RC coupled amplifier introduces a 180° phase shift between input and output signals in the mid band region. At low frequencies the output voltage V_o lags V_i by an additional angle θ_1. Therefore the total phase shift between V_o and V_i is more than 180°. At high frequencies V_o leads V_i by an additional angle θ_2. As a result the total phase shift drops below 180°. Figure 4.6 shows the phase plot for a single stage RC-coupled amplifier.

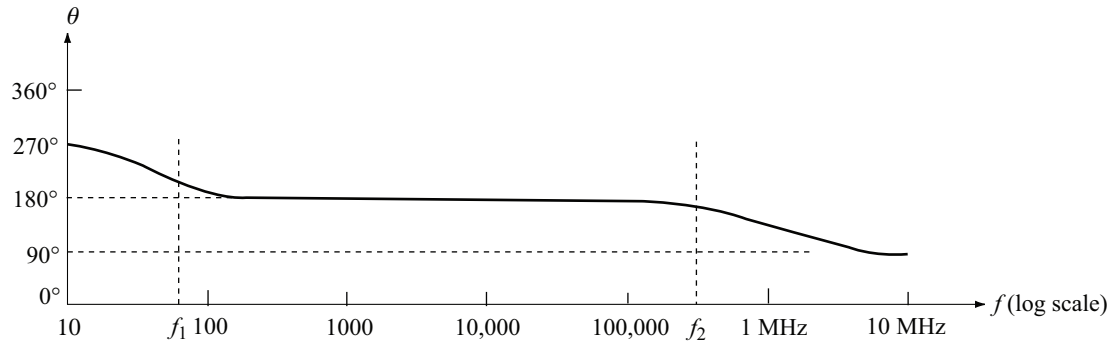


Fig. 4.6 Phase plot of single stage RC-coupled amplifier

◆ 4.2 LOW FREQUENCY ANALYSIS

In low frequency region, we have seen that the amplifier gain increases with frequency. Hence it can be modelled as a high-pass RC circuit as shown in Fig. 4.7.

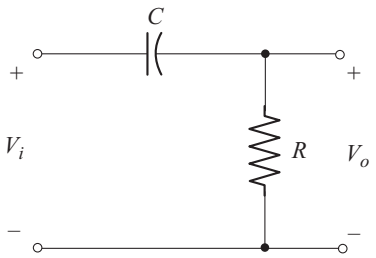


Fig. 4.7 Amplifier modelled as high-pass RC circuit

The capacitor C represents the combined effect of coupling and bypass capacitors and the resistance R represents the combined effect of resistive elements of the amplifier network.

The capacitive reactance is given by

$$X_C = \frac{1}{2\pi f C} \tag{4.6}$$

At $f = 0$, $X_C = \infty\ \Omega$

i.e. at low frequencies the capacitor acts as an open circuit as shown in Fig. 4.8.

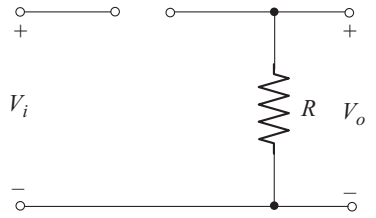


Fig. 4.8 Capacitor acts as open circuit at f = 0

From the circuit of Fig. 4.8 we find that, $V_o = 0$.
At high frequencies, $X_C \approx 0\ \Omega$
i.e., at high frequencies the capacitor acts as a short circuit as shown in Fig. 4.9.

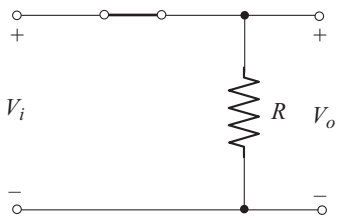


Fig. 4.9 Capacitor acts as short circuit at high frequencies

Form the circuit of Fig. 4.9, we find that, $V_o \approx V_i$. Note that as the input signal frequency increases from zero to the mid band value, the output voltage rises from zero to V_i and hence the gain from zero to one. Let us verify this fact using mathematical analysis.

Mathematical Analysis

Using voltage division rule in the circuit of Fig. 4.7, we have

$$V_o = \frac{V_i\, R}{R - j\, X_C}$$

Voltage gain is given by

$$A_V = \frac{V_o}{V_i} = \frac{R}{R - j\, X_C}$$

$$A_V = \frac{1}{1 - j\left[\dfrac{X_C}{R}\right]} \tag{4.7}$$

The magnitude of voltage gain is

$$|A_V| = \frac{1}{\sqrt{1 + \left[\dfrac{X_C}{R}\right]^2}} \tag{4.8}$$

Now let us find the gain at different frequencies:

- At $f = 0$, $\quad X_C = \dfrac{1}{2\pi f C} = \infty\ \Omega$

  $\therefore \quad |A_V| = 0$

- At high frequencies

  $f \to \infty$ and therefore $X_C \to 0$

as a result, $|A_V| \to 1 = |A_V|_{\text{mid}}$

Now $|A_V|_{\text{mid (dB)}} = 20 \log_{10}(1) = 0$ dB.

- When the capacitive reactance equals the resistance

$$\text{ie} \quad X_C = R \tag{4.9}$$

$$|A_V| = \frac{1}{\sqrt{2}} \Rightarrow \frac{V_o}{V_i} = \frac{1}{\sqrt{2}} \quad \text{or} \quad V_o = 0.707\, V_i$$

The corresponding decibel gain is

$$20 \log_{10} \frac{1}{\sqrt{2}} = -3 \text{ dB}$$

Note that this condition must give the cut-off frequency
From Equation (4.9)

$$\frac{1}{2\pi f C} = R$$

$$f = \frac{1}{2\pi RC}$$

The frequency given by the above equation is the lower cut-off frequency or the lower 3dB cut-off frequency denoted by f_1.

$$\therefore \quad f_1 = \frac{1}{2\pi RC} \tag{4.10}$$

$$\frac{X_C}{R} = \frac{1}{2\pi f C R} = \left[\frac{1}{2\pi RC}\right]\left[\frac{1}{f}\right] = \boldsymbol{\frac{f_1}{f}}$$

Using this relation in Equations (4.7) and (4.8) we have

$$A_V = \frac{1}{1 - j\left[\frac{f_1}{f}\right]} \tag{4.11}$$

$$|A_V| = \frac{1}{\sqrt{1 + \left[\frac{f_1}{f}\right]^2}} \tag{4.12}$$

From Equation (4.11) the phase angle of A_V is

$$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right] \tag{4.13}$$

Since θ_1 is positive, V_o leads V_i by an angle θ_1.

In magnitude and phase form, Equation (4.11) can be written as

$$A_V = |A_V| \angle \theta_1$$

$$A_V = \frac{1}{\sqrt{1+\left[\frac{f_1}{f}\right]^2}} \angle \tan^{-1}\left[\frac{f_1}{f}\right] \tag{4.14}$$

Figure 4.10 shows the plot of $|A_V|$ versus frequency.

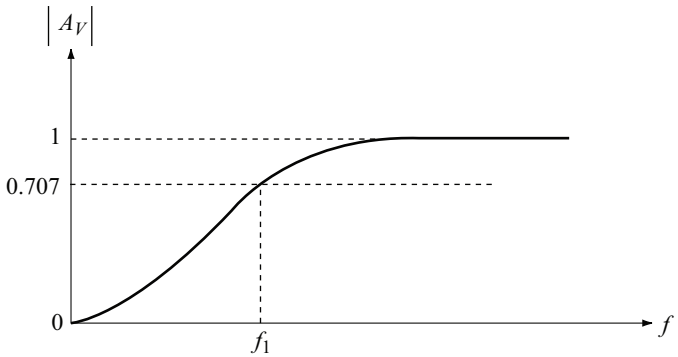


Fig. 4.10 Low frequency response of high pass-RC circuit

Bode Plot of Low Frequency Response

From Equation (4.12) we have

$$|A_V| = \frac{1}{\sqrt{1+\left[\frac{f_1}{f}\right]^2}}$$

Voltage gain in dB is

$$|A_V|_{\text{dB}} = 20 \log_{10} \left[\frac{1}{\sqrt{1+\left[\frac{f_1}{f}\right]^2}}\right]$$

$$= -20 \log_{10} \sqrt{1+\left[\frac{f_1}{f}\right]^2} \tag{4.15}$$

Now let us construct the plot of $|A_V|_{\text{dB}}$ versus frequency using the straight line segments by considering the following frequency ranges.

1. **For frequencies,** $f \ll f_1$ **or** $\dfrac{f_1}{f} \gg 1$

Equation (4.15) can be approximated by

$$|A_V|_{\text{dB}} \approx -20 \log_{10} \sqrt{\left[\frac{f_1}{f}\right]^2}$$

or

$$|A_V|_{\text{dB}} = -20 \log_{10} \left[\frac{f_1}{f}\right] \tag{4.16}$$

$|A_V|_{\text{dB}}$ is calculated at different values of $\dfrac{f_1}{f}$ and tabulated in Table 4.1.

Table 4.1 $|A_V|_{\text{dB}}$ at different frequencies

f	$\dfrac{f_1}{f}$	$\lvert A_V \rvert_{\text{dB}} = -20 \log_{10} \left[\dfrac{f_1}{f}\right]$
$\dfrac{f_1}{10}$	10	– 20 dB
$\dfrac{f_1}{4}$	4	– 12 dB
$\dfrac{f_1}{2}$	2	– 6 dB
f_1	1	0 dB

From the results given in Table 4.1, we can draw the following interesting conclusions.

- A change in frequency by a factor of two is equal to one octave. When the frequency changes from $\dfrac{f_1}{4}$ to $\dfrac{f_1}{2}$ or $\dfrac{f_1}{2}$ to f_1 (one octave), the gain increases by 6 dB.
- A change in frequency by a factor of ten, is equal to one decade. When the frequency changes from $\dfrac{f_1}{10}$ to f_1 (one decade), the gain increases by 20 dB.
- If we plot $|A_V|_{\text{dB}}$ against log scale in the frequency range $\dfrac{f_1}{10} < f < f_1$, we get a straight line with slope 6 dB/octave or 20 dB/decade, as shown in Fig. 4.11.

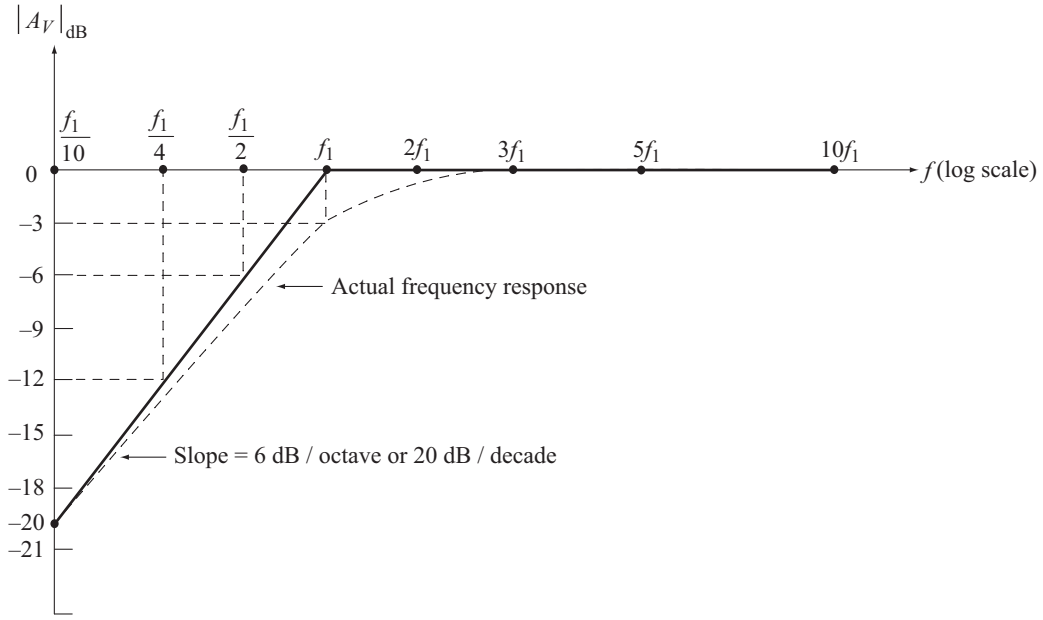


Fig. 4.11 Bode plot for low frequency region

2. **For frequencies,** $f \gg f_1$ **or** $\frac{f_1}{f} \ll 1$

Equation (4.15) can be approximated by

$$|A_V|_{dB} \approx -20 \log_{10} 1 = 0 \text{ dB}$$

The plot of $|A_V|_{dB}$ against log scale for the frequency range $f \gg f_1$, is a straight line on the frequency axis as shown in Fig 4.15. Note that the slope of this line is zero since the gain is constant at 0 dB.

The plot shown in Fig 4.11 is made up of two straight line segments called asymptotes with a break point at f_1. Hence f_1 is called the break frequency or the corner frequency. This piece wise linear plot is also called the Bode magnitude plot or simply Bode plot.

The actual frequency response is also indicated in Fig. 4.11. Note that

From Bode plot, at $f = f_1$, $|A_V|_{dB} = 0$.

From actual plot, at $f = f_1$, $|A_V|_{dB} = -3$.

We find that at $f = f_1$, the gain read from the Bode plot differs from the actual gain by 3 dB.

Phase Plot

At low frequencies, V_o leads V_i by an angle θ_1 given in Equation (4.13) by

$$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right] \tag{4.17}$$

The value of θ_1 is calculated at different values of $\frac{f_1}{f}$ and tabulated in Table 4.2.

Table 4.2 Phase angle between V_o and V_i

f	$\frac{f_1}{f}$	$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right]$	*Total phase shift* $\theta = 180 + \theta_1$
0	∞	90°	270°
$\frac{f_1}{100}$	100	89.4°	269.4°
f_1	1	45°	225°
$100 f_1$	0.01	0.572°	180.572°
∞	0	0°	180°

The total phase shift θ between V_o and V_i is the sum of the phase shift of RC network and the inherent phase shift (180°) introduced by the amplifier.

The following observations can be made from the results given in Table 4.2.

When the input signal frequency increases from zero to the mid band value ($f \gg f_1$).

- The phase shift θ_1 due to RC network decreases from 90° to 0°. The plot of θ_1 versus frequency is shown in Fig. 4.12.
- The total phase θ, decreases from 270° to 180°.

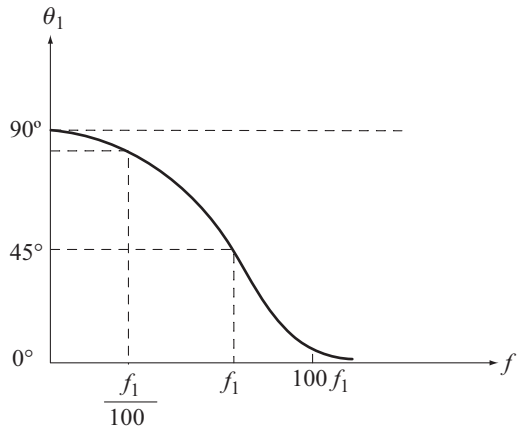


Fig. 4.12 Phase response of RC network of Fig 4.7

Example 4.1

For the circuit shown below

(a) Determine the mathematical expression for $\left|\frac{V_o}{V_i}\right|$

(b) Calculate the break frequency

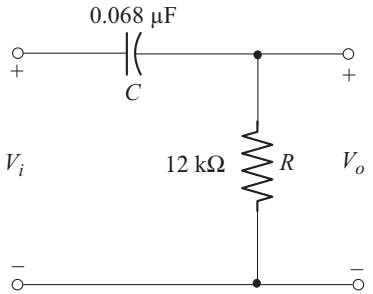
(c) Calculate $\left|\frac{V_o}{V_i}\right|$ at 10 Hz, 100 Hz, 1 kHz, 2 kHz, 5 kHz and 10 kHz

(d) Sketch the frequency response of $\left|\frac{V_o}{V_i}\right|$

(e) Construct the Bode magnitude plot

(f) Sketch the actual frequency response

(g) Compare the results obtained in part (d) and part (e).



Solution

(a) The expression for $\left|\frac{V_o}{V_i}\right|$ is given in Equation (4.12) which is derived under mathematical analysis in section 4.2.

$$|A_V| = \left|\frac{V_o}{V_i}\right| = \left[\frac{1}{\sqrt{1+\left[\frac{f_1}{f}\right]^2}}\right]$$

(b) The break frequency is

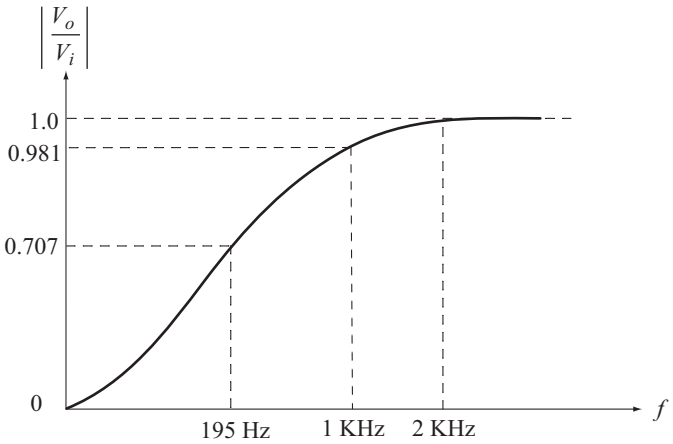
$$f_1 = \frac{1}{2\pi RC}$$

$$= \frac{1}{(2)(\pi)(12\ \text{k}\Omega)(0.068\ \mu\text{F})} = 195\ \text{Hz}.$$

(c) **Table A**

f	$\frac{f_1}{f}$	$\lvert A_V \rvert = \left\lvert \frac{V_o}{V_i} \right\rvert$	$\lvert A_V \rvert_{dB} = 20 \log_{10} \lvert A_V \rvert$
10 Hz	19.5	0.0512	– 25.8
19.5 Hz $\left[= \frac{f_1}{10} \right]$	10	0.0995	– 20.04
100 Hz	1.95	0.456	– 6.82
195 Hz $[= f_1]$	1	0.707	– 3
1 KHz	0.195	0.981	– 0.166
2 KHz	0.0975	1	0
5 KHz	0.039	1	0
10 KHz	0.0195	1	0

(d) Frequency response of $\left| \frac{V_o}{V_i} \right|$



(e) Bode plot

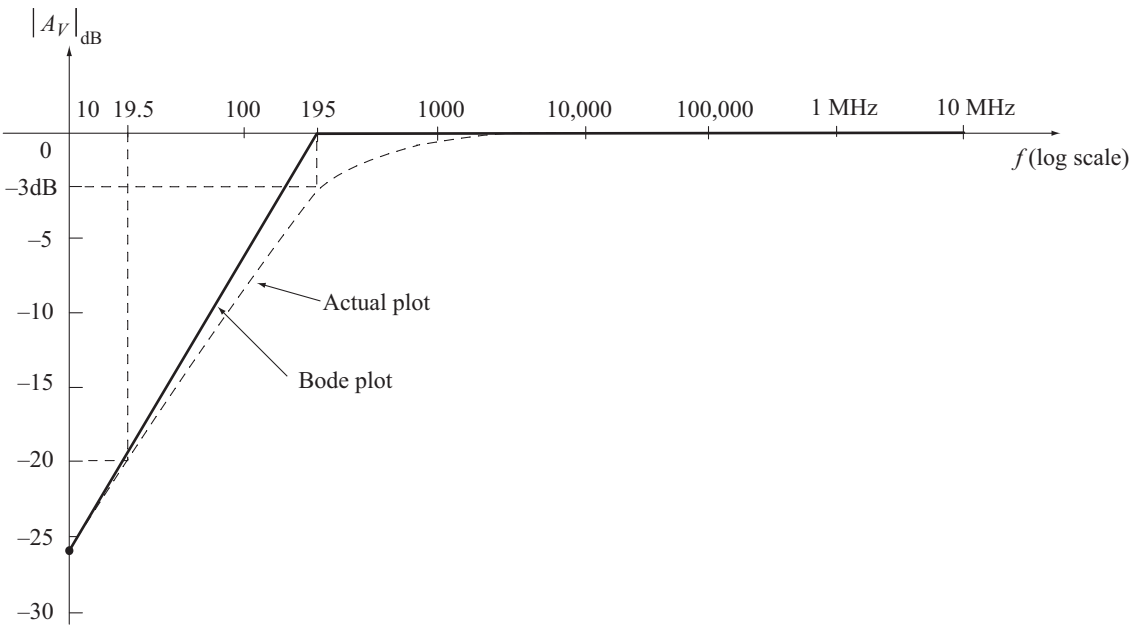
It consists of two straight line segments.

at $f = \frac{f_1}{10}$ $\quad \lvert A_V \rvert_{dB} = -20 \log_{10} \left[\frac{f_1}{f} \right] = -20$

at $f = f_1$ $\quad \lvert A_V \rvert_{dB} = -20 \log_{10} [1] = 0$

The first line is obtained by joining these two points.
This line has a slope of 20 dB/decade or 6 dB/octave.
The second line is drawn on frequency axis starting from $f = f_1$ at it has slope of 0 dB/decade.

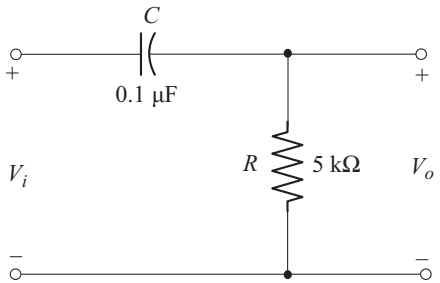
(f) The actual plot is sketched using the values given in the 4th column of Table A, along with Bode plot in the following figure.



Example 4.2

For the circuit shown below

(a) Determine the mathematical expression for the phase angle θ_1 between V_o and V_i.
(b) Calculate the break frequency.
(c) Calculate phase angle θ_1 at f = 100 Hz, 1 KHz, 2 KHz, 5 KHz and 10 KHz.
(d) Sketch the phase angle versus frequency plot using the results obtained in part (c).



Solution

(a) The expression for θ_1 is given in Equation (4.13) which is derived under mathematical analysis in section 4.2.

$$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right]$$

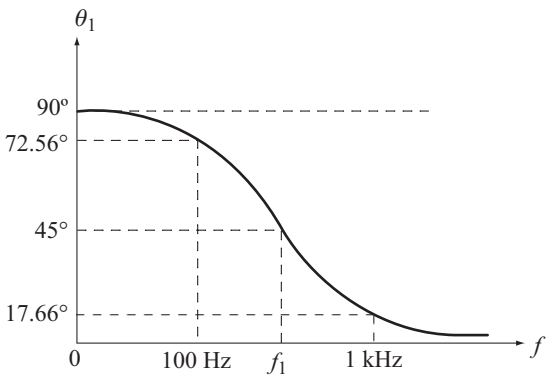
(b) The break frequency is

$$f_1 = \frac{1}{2\pi RC} = \frac{1}{2\pi(5\ \text{k}\Omega)(0.1\ \mu\text{F})} = 318.3\ \text{Hz}$$

(c) Calculation of θ_1 at different frequencies

f	$\frac{f_1}{f}$	$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right]$
0	∞	90°
100 Hz	3.183	72.56°
318.3 Hz [= f_1]	1	45°
1 KHz	0.3183	17.66°
2 KHz	0.15915	9.043°
5 KHz	0.06366	3.643°
10 KHz	0.03183	1.823°

(d) The phase angle plot is shown below



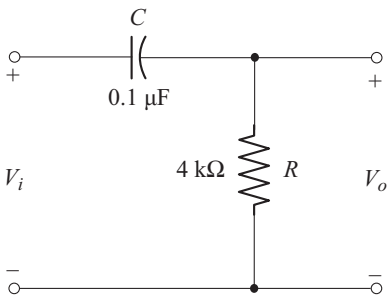
Example 4.3

For the circuit shown below

(a) Calculate the lower 3 dB frequency.

(b) Find the magnitude and phase angle of A_V at 1000 Hz.

(c) Calculate the output voltage if the input voltage is $v_i = 10 \sin [12566\, t]$ V



Solution

(a) Lower 3 dB frequency is

$$f_1 = \frac{1}{2\pi RC} = \frac{1}{2\pi\,(4\text{ k}\Omega)\,(0.1\ \mu\text{F})} = 397.88\text{ Hz}$$

(b) Magnitude of A_V is

$$|A_V| = \frac{1}{\sqrt{1+\left[\dfrac{f_1}{f}\right]^2}}$$

Phase angle of A_V is

$$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right]$$

At $f = 1000$Hz

$$|A_V| = \frac{1}{\sqrt{1+\left[\dfrac{397.88}{1000}\right]^2}} = 0.929$$

$$\theta_1 = \tan^{-1}\left[\frac{397.88}{1000}\right] = 21.69°$$

(c)
$$v_i = 10 \sin [12566\, t] = V_m \sin \omega t$$
$$V_m = 10\text{ V}$$
$$\omega = 12566\text{ rad/s}$$
$$f = \frac{\omega}{2\pi} = \frac{12566}{2\pi} = 2000\text{ Hz}$$

$$|A_V| = \frac{1}{\sqrt{1+\left[\dfrac{397.88}{2000}\right]^2}} = 0.98$$

$$\theta_1 = \tan^{-1}\left[\frac{397.88}{2000}\right] = 11.25°$$

v_o leads v_i by an angle θ_1

$$\therefore \quad v_o = V_m \cdot |A_V| \cdot \sin[\omega t + \theta_1]$$
$$= [10][0.98] \sin[12566\, t + 11.25°]$$
$$= 9.8 \sin[12566\, t + 11.25°]\ \text{V}$$

Example 4.4

It is desired that the voltage gain of an RC-coupled amplifier at 60 Hz should not decrease by more than 10% from its mid band value. Calculate

(a) the lower 3dB frequency
(b) the required C if $R = 2000\ \Omega$

Solution

(a) Note that 60 Hz lies in the low frequency region

$$\therefore \quad |A_V| = \frac{1}{\sqrt{1+\left[\frac{f_1}{f}\right]^2}} \qquad \text{(A)}$$

Given at $f = 60$ Hz, $|A_V| = 0.9$

Using this condition in Equation (A), we get

$$0.9 = \frac{1}{\sqrt{1+\left[\frac{f_1}{60}\right]^2}}$$

Solving we get, $f_1 = 29$ Hz

(b)
$$f_1 = \frac{1}{2\pi RC}$$
$$C = \frac{1}{2\pi f_1 R} = \frac{1}{2\pi(29\,\text{Hz})(2000\,\Omega)}$$
$$= 2.74\ \mu\text{F}$$

◆ 4.3 LOW FREQUENCY RESPONSE OF BJT AMPLIFIER

Figure 4.13 shows the circuit of single stage BJT amplifier. The coupling capacitors C_S and C_C and the bypass capacitor C_E determine the low frequency response. Now let us study the influence of each of these on low frequency response.

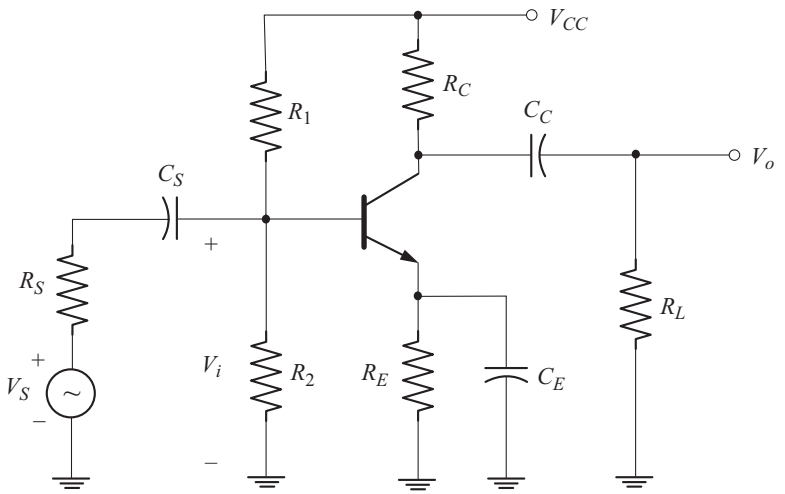


Fig. 4.13 Single stage BJT amplifier with coupling and bypass capacitors

Effect of Input Coupling Capacitor C_S on Low Frequency Response

The input coupling capacitor C_S couples the source signal to the active device (BJT). To study the effect of C_S on low frequency response we have to neglect the effects of C_C and C_E. This can be done by treating them as short circuits.

Now let us obtain the ac equivalent circuit by reducing V_{CC} to zero and replacing C_C and C_E by their short circuit equivalents. C_S is retained as it is. The ac equivalent circuit is shown in Fig. 4.14.

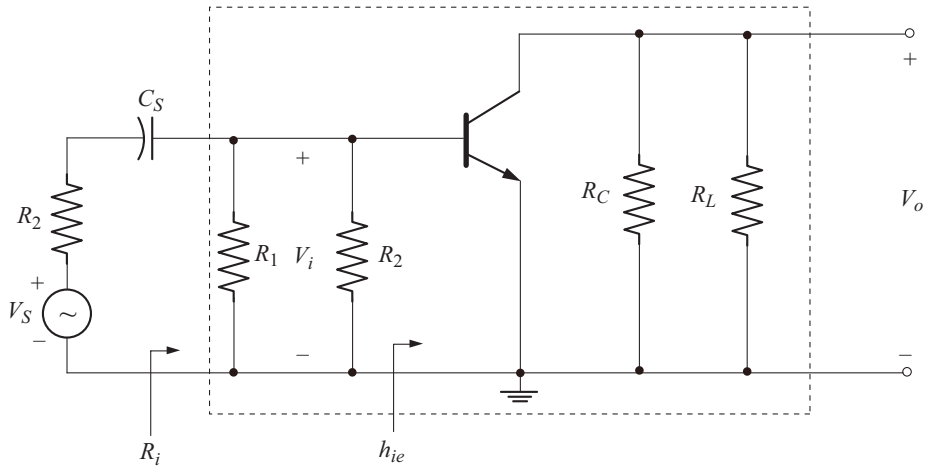


Fig. 4.14 AC equivalent circuit

The resistance of the transistor between base emitter is h_{ie}. The input ac equivalent circuit is shown in Fig. 4.15.

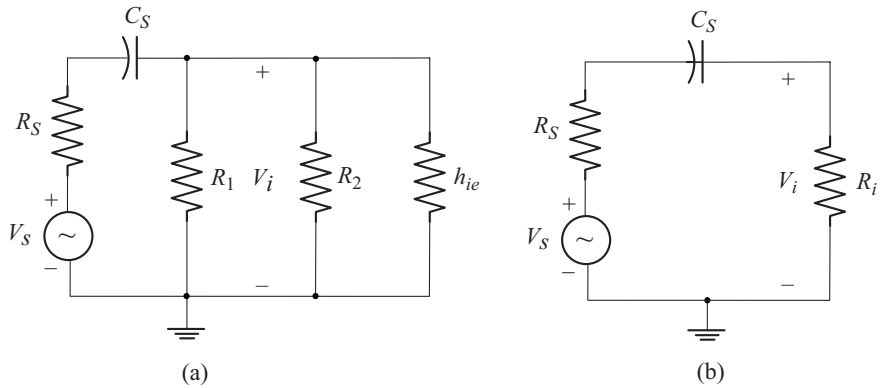


Fig. 4.15 (a) Input ac equivalent circuit
(b) Simplified input ac equivalent circuit

Let
$$R_i = R_1 \parallel R_2 \parallel h_{ie} \tag{4.18}$$

where
$$h_{ie} = \beta\, r_e \tag{4.19}$$

Using voltage division rule in the circuit of Fig. 4.15(b), the voltage applied to the amplifier is given by

$$V_i = \frac{V_S\, R_i}{\left[R_S + R_i\right] - j\, X_{C_S}} \tag{4.20}$$

where
$$X_{C_S} = \frac{1}{2\pi f\, C_S} \tag{4.21}$$

$$V_i = \frac{V_S\left[\dfrac{R_i}{R_S + R_i}\right]}{1 - j\left[\dfrac{X_{C_S}}{R_S + R_i}\right]}$$

$$|V_i| = \frac{|V_S|\left[\dfrac{R_i}{R_S + R_i}\right]}{\sqrt{1 + \left[\dfrac{X_{C_S}}{R_S + R_i}\right]^2}} \tag{4.22}$$

In the mid frequency band, f is sufficiently large. As a result, $X_{C_S} \to 0$. Now from Equation (4.22) we have

$$|V_i|_{\text{mid}} = \frac{|V_S|R_i}{R_S + R_i} \tag{4.23}$$

Using this relation in Equation (4.22), we have

$$|V_i| = \frac{|V_i|_{\text{mid}}}{\sqrt{1+\left[\frac{X_{C_S}}{R_S+R_i}\right]^2}} \tag{4.24}$$

The lower 3 dB cut-off occurs, when

$$|V_i| = \frac{|V_i|_{\text{mid}}}{\sqrt{2}} = 0.707\,|V_i|_{\text{mid}}$$

From Equation (4.24) we find that, the 3 dB cut off occurs, when

$$\frac{X_{C_S}}{R_S+R_i} = 1 \quad \text{or} \quad X_{C_S} = R_S + R_i$$

$$\frac{1}{2\pi f C_S} = R_S + R_i$$

or

$$f = \frac{1}{2\pi\left[R_S+R_i\right]C_S} \tag{4.25}$$

Equation (4.25) gives the lower 3dB cut-off frequency due to C_S. Let us denote it by f_{L_S}. Now we have

$$f_{L_S} = \frac{1}{2\pi\left[R_S+R_i\right]C_S} \tag{4.26}$$

Effect of Output Coupling Capacitor C_C on Low Frequency Response

The output coupling capacitor C_C couples the output of the active device to the load. To study the effect of C_C on low frequency response, let us neglect the effect of C_S and C_E by treating them as short circuits.

From the circuit of Fig 4.14, we can write the ac equivalent circuit on the output side as shown in Fig. 4.16(a).

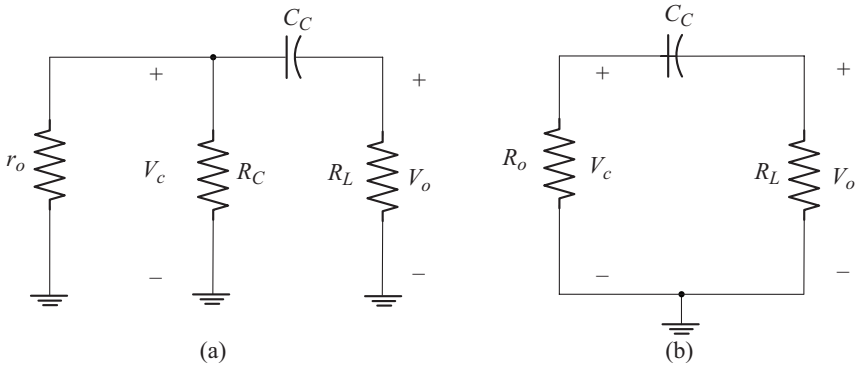


Fig. 4.16 (a) AC equivalent circuit of output side
(b) Simplified ac equivalent circuit

Let $$R_o = r_o \parallel R_C \tag{4.27}$$

The simplified ac equivalent circuit is shown in Fig. 4.16(b).

V_c = Output voltage of active device

V_o = Load voltage

Using voltage division rule in the circuit of Fig. 4.16(b), the load voltage is given by

$$V_o = \frac{V_c \, R_L}{\left[R_o + R_L\right] - j\, X_{C_C}} \tag{4.28}$$

where $$X_{C_C} = \frac{1}{2\pi f C_C} \tag{4.29}$$

$$V_o = \frac{V_c \left[\dfrac{R_L}{R_o + R_L}\right]}{1 - j\left[\dfrac{X_{C_C}}{R_o + R_L}\right]}$$

$$|V_o| = \frac{|V_c| \left[\dfrac{R_L}{R_o + R_L}\right]}{\sqrt{1 + \left[\dfrac{X_{C_C}}{R_o + R_L}\right]^2}} \tag{4.30}$$

In the mid frequency band, $X_{C_C} \to 0$. Now from Equation (4.30) we have

$$|V_o|_{\text{mid}} = \frac{|V_c| \, R_L}{R_o + R_L} \tag{4.31}$$

Using this relation in Equation (4.30) we have

$$|V_o| = \frac{|V_o|_{\text{mid}}}{\sqrt{1 + \left[\dfrac{X_{C_C}}{R_o + R_L}\right]^2}} \tag{4.32}$$

The lower 3dB cut-off occurs when

$$|V_o| = \frac{|V_o|_{\text{mid}}}{\sqrt{2}} = 0.707\,|V_o|_{\text{mid}}$$

From Equation (4.32) we find that, the 3dB cut-off occurs when

$$\frac{X_{C_C}}{R_o + R_L} = 1 \quad \text{or} \quad X_{C_C} = R_o + R_L$$

$$\frac{1}{2\pi f C_C} = R_o + R_L$$

or
$$f = \frac{1}{2\pi \left[R_o + R_L\right] C_C} \tag{4.33}$$

Equation (4.33) gives the lower 3 dB cut-off frequency due to C_C. Let us denote it by f_{L_C}. Now we have

$$f_{L_C} = \frac{1}{2\pi \left[R_o + R_L\right] C_C} \tag{4.34}$$

Effect of Emitter Bypass Capacitor C_E on Low Frequency Response

To study the effect of C_E on low frequency response, let us neglect the effect of C_S and C_C by treating them as short circuits.

From the circuit of Fig. 4.13, we can write the ac equivalent as shown in Fig. 4.17.

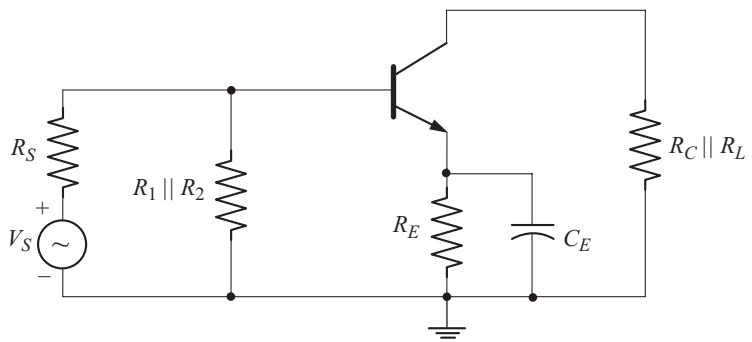


Fig. 4.17 AC equivalent circuit to study the effect of C_E

Let us replace the transistor by its low frequency small signal hybrid model as shown in Fig. 4.18.

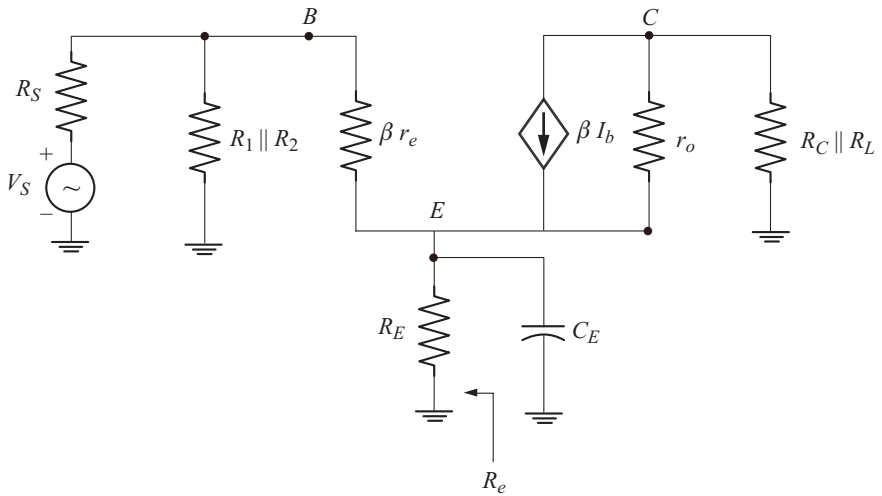


Fig. 4.18 AC equivalent circuit using hybrid model

R_e is the ac equivalent resistance seen by C_E. To find R_e we reduce V_S to zero as shown in Fig. 4.19. For simplicity the output circuit is omitted.

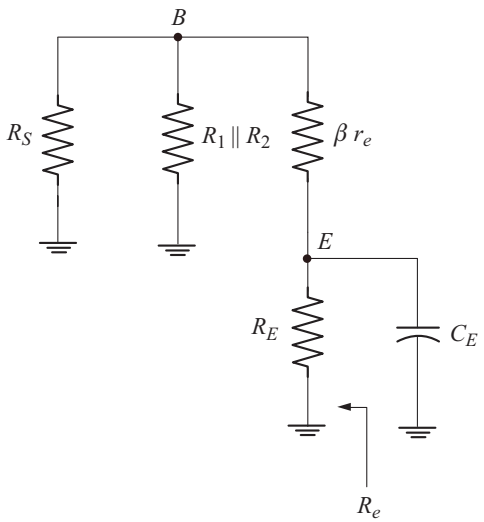


Fig. 4.19 Circuit to find R_e

$$\text{Let} \qquad R'_S = R_S \| R_1 \| R_2 \tag{4.35}$$

The ac equivalent circuit is redrawn as shown in Fig. 4.20.

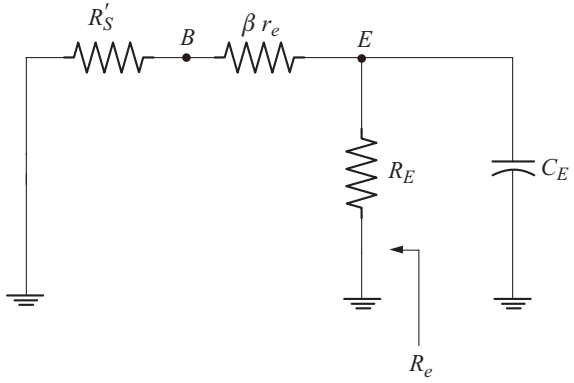


Fig. 4.20 AC equivalent circuit redrawn

Note that $R'_S + \beta\, r_e$ is in the base circuit. When it is transferred to the emitter circuit it gets divided by β, since the emitter current is approximately β times the base current. The resulting circuit is shown in Fig. 4.21.

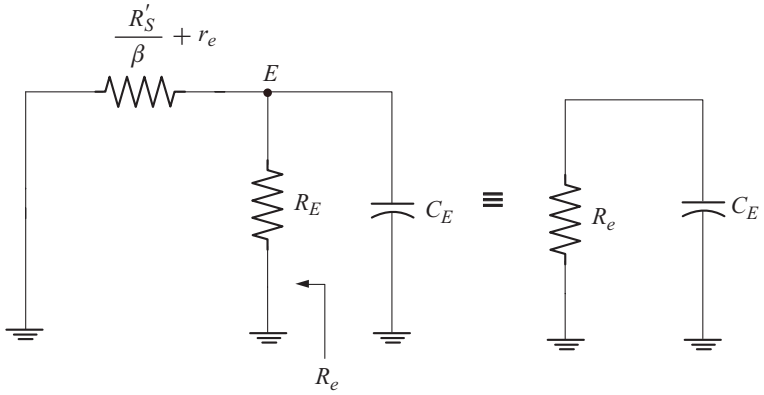


Fig. 4.21 Circuit to find R_e

Note that

$$R_e = R_E \| \left[\frac{R_S'}{\beta} + r_e \right] \tag{4.36}$$

For the circuit of Fig. 4.21, the lower cut-off frequency due to C_E is given by

$$f_{L_E} = \frac{1}{2\pi R_e C_E} \tag{4.37}$$

Effect of C_E on Voltage Gain

The midband voltage gain of the amplifier of Fig. 4.13 with out C_E is given by

$$A_{V\,\text{mid}} = - \frac{R_o \| R_L}{r_e + R_E} \tag{4.38}$$

where $R_o = R_C \| r_o$

If C_E is connected in parallel with R_E, then the voltage gain becomes a function of frequency. Now the voltage gain at any frequency is given by

$$A_V = - \frac{R_o \| R_L}{r_e + R_E \| X_{C_E}} \tag{4.39}$$

where

$$X_{C_E} = \frac{1}{2\pi f C_E} \tag{4.40}$$

As the frequency increases:

- X_{C_E} decreases
- $R_E \| X_{C_E}$ decreases
- A_V increases in magnitude

As the frequency approaches the midband value

- X_{C_E} approaches zero
- $R_E \,||\, X_{C_E}$ approaches zero (i.e R_E is shorted out)
- A_V approaches the maximum value or midband value

$$A_{V\,\text{mid}} = -\frac{R_o \,||\, R_L}{r_e} \tag{4.41}$$

Note that, Equation (4.41) can be obtained from Equation (4.39) by substituting $R_E = 0\ \Omega$

Over all Lower Cut-off Frequency

The low frequency response of the amplifier is influenced by the capacitors C_S, C_C and C_E. The lower cut-off frequencies due to C_S, C_C and C_E respectively are f_{L_S}, f_{L_C} and f_{L_E}. If these cut-off frequencies are relatively apart (i.e., one is greater than the other by four times or more) the higher of the three is approximately the lower cut-off frequency for the amplifier stage.

For example if $f_{L_S} = 6$ Hz, $f_{L_C} = 25$ Hz and $f_{L_E} = 320$ Hz

then the lower cut-off frequency of the amplifier is $f_{L_E} = 320$ Hz, since

$$f_{L_C} > 4 f_{L_S} \quad \text{and} \quad f_{L_E} > 4 f_{L_C}$$

Example 4.5

For the circuit shown below calculate the following:

(a) r_e

(b) Input resistance, R_i

(c) Mid band voltage gains $A_V = \dfrac{V_o}{V_i}$ and $A_{V_S} = \dfrac{V_o}{V_S}$

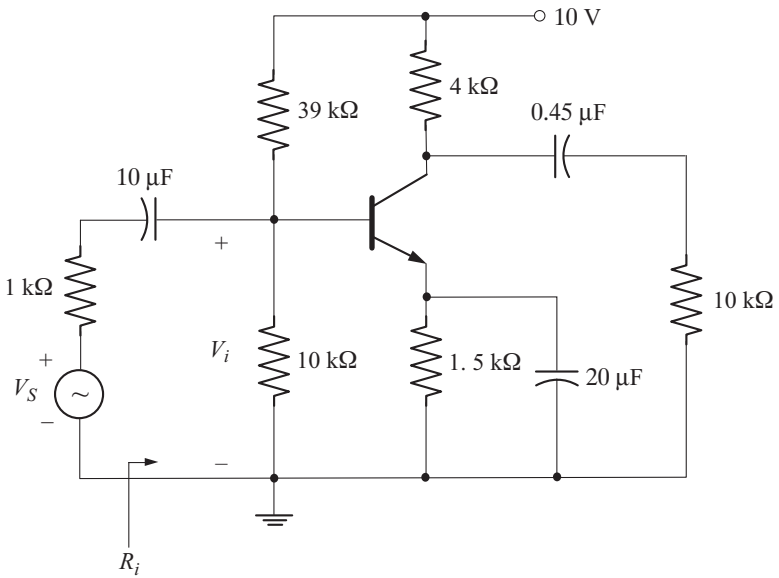
(d) Lower cut-off frequency due to C_S

(e) Lower cut-off frequency due to C_C

(f) Lower cut-off frequency due to C_E

(g) Overall lower cut-off frequency

For the transistor, $\beta = 100$ and $r_o = \infty\ \Omega$.



Solution

(a) Calculation of r_e

Check for,

$$\beta R_E \geq 10 R_2$$
$$\beta R_E = (100)\,(1.5\ \text{k}\Omega) = 150\ \text{k}\Omega$$
$$10 R_2 = (10)\,(10\ \text{k}\Omega) = 100\ \text{k}\Omega$$

Since $\beta R_E > 10 R_2$, we can use approximate analysis

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{(10\ \text{V})(10\ \text{k}\Omega)}{39\ \text{k}\Omega + 10\ \text{k}\Omega} = 2.04\ \text{V}$$
$$V_E = V_B - V_{BE} = 2.04\ \text{V} - 0.7\ \text{V} = 1.34\ \text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{1.34\,\text{V}}{1.5\ \text{k}\Omega} = 0.893\ \text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{0.893\,\text{mA}} = 29.1\ \Omega$$

(b) ***Input Resistance***

$$R_i = R_1 \,\|\, R_2 \,\|\, \beta r_e$$
$$= 39\ \text{k}\Omega \,\|\, 10\ \text{k}\Omega \,\|\, (100)\ (29.1\ \Omega) = 2.13\ \text{k}\Omega$$

(c) ***Midband Voltage Gain***

$$A_V = \frac{V_o}{V_i} = -\frac{R_o \,\|\, R_L}{r_e}$$

$$R_o = R_C \,||\, r_o = 4\ \text{k}\Omega \,\|\, \infty = 4\ \text{k}\Omega$$

$$R_o \,||\, R_L = 4\ \text{k}\Omega \,\|\, 10\ \text{k}\Omega = 2.86\ \text{k}\Omega$$

$$A_V = -\frac{2.86\ \text{k}\Omega}{29.1\ \Omega} = -98.28$$

$$A_{V_S} = \frac{V_o}{V_S}$$

$$= \frac{V_o}{V_i} \cdot \frac{V_i}{V_S}$$

$$= A_V \frac{V_i}{V_S} \qquad \text{(A)}$$

In the midband, C_S represents short circuit. The input equivalent circuit in the mid band is shown in Fig. A.

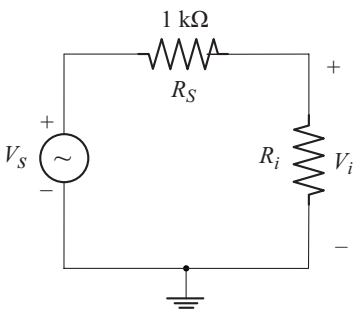


Fig. A

Using voltage division rule

$$V_i = \frac{V_S R_i}{R_S + R_i}$$

$$\frac{V_i}{V_S} = \frac{R_i}{R_S + R_i} = \frac{2.13\ \text{k}\Omega}{1\ \text{k}\Omega + 2.13\ \text{k}\Omega} = 0.68$$

Using this value in Equation (A) we get

$$A_V = (-98.28)\,(0.68) = -66.83$$

(d) *Lower Cut-off Frequency due to C_S*

$$f_{L_S} = \frac{1}{2\pi\left[R_S + R_i\right]C_S}$$

$$= \frac{1}{2\pi\left[1\ \text{k}\Omega + 2.13\ \text{k}\Omega\right]\left[10\ \mu\text{F}\right]} = 5.08\ \text{Hz}$$

(e) *Lower Cut-off Frequency due to C_C*

$$f_{L_C} = \frac{1}{2\pi \left[R_o + R_L\right] C_C}$$

$$R_o = R_C \,||\, r_o = 4\ \text{k}\Omega \,\|\, \infty = 4\ \text{k}\Omega$$

$$f_{L_C} = \frac{1}{2\pi\left[4\ \text{k}\Omega + 10\ \text{k}\Omega\right]\left[0.45\ \mu\text{F}\right]} = 25.26\ \text{Hz}$$

(f) *Lower Cut-off frequency due to C_E*

$$f_{L_E} = \frac{1}{2\pi R_e C_E}$$

$$R_e = R_E \,||\, \left[\frac{R_S'}{\beta} + r_e\right]$$

$$R_S' = R_S \,||\, R_1 \,||\, R_2 = 1\ \text{k}\Omega \,\|\, 39\ \text{k}\Omega \,\|\, 10\ \text{k}\Omega = 0.888\ \text{k}\Omega$$

$$\frac{R_S'}{\beta} + r_e = \frac{0.888\ \text{k}\Omega}{100} + 29.1\ \Omega = 37.98\ \Omega$$

$$R_e = 1.5\ \text{k}\Omega \,\|\, 37.98\ \Omega = 37\ \Omega$$

$$f_{L_E} = \frac{1}{2\pi\left[37\Omega\right]\left[20\ \mu\text{F}\right]} = 215\ \text{Hz}$$

(g) *Over all Lower Cut-off Frequency*

We have

$$f_{L_S} = 5.08\ \text{Hz} \quad f_{L_C} = 25.26\ \text{Hz} \quad f_{L_E} = 215\ \text{Hz}$$

Note that $f_{L_C} > 4 f_{L_S}$

and $f_{L_E} > 4 f_{L_C}$

Therefore over all lower cut-off frequency is f_{LE}

$$f_L = f_{L_E} = 215\ \text{Hz}$$

Example 4.6

Repeat example 4.5 with $r_o = 40\ \text{k}\Omega$.

Solution

$$r_o = 40\ \text{k}\Omega$$

$$R_C = 4\ \text{k}\Omega$$

Since $r_o \geq 10\ R_C$, the effect of r_o can be neglected. Therefore, all the results remain unaffected.

Example 4.7

Repeat example 4.5 with $r_o = 20\ \text{k}\Omega$.

Solution

In this case $r_o < 10\ R_C$. Only A_V, $A_{V\,\text{mid}}$ and f_{L_C} get affected. Other values remain unchanged.

$$\left.\begin{array}{ll} r_e = 29.1\ \Omega & R_i = 2.13\ \text{k}\Omega \\ f_{L_S} = 5.08\ \text{Hz} & f_{L_E} = 215\ \text{Hz} \end{array}\right\} \quad \text{As calculated in example 4.5}$$

Midband Voltage Gain

$$A_V = \frac{V_o}{V_i} = -\frac{R_o \,||\, R_L}{r_e}$$

$$R_o = R_C \,||\, r_o = 4\text{k}\ \Omega \,\|\, 20\ \text{k}\Omega = 3.33\ \text{k}\Omega$$

$$R_o \,||\, R_L = 3.33\ \text{k}\Omega \,\|\, 10\ \text{k}\Omega = 2.49\ \text{k}\Omega$$

$$A_V = -\frac{2.49\ \text{k}\Omega}{29.1\ \Omega} = -85.56$$

$$A_{V_S} = A_V \left[\frac{R_i}{R_i + R_S}\right] = (-85.56)\,(0.68) = -58.18$$

Lower Cut-off Frequency due to C_C

$$f_{L_C} = \frac{1}{2\pi \left[R_o + R_L\right] C_C}$$

$$= \frac{1}{2\pi\left[3.33\ \text{k}\Omega + 10\ \text{k}\Omega\right]\left[0.45\ \mu\text{F}\right]} = 26.53\ \text{Hz}$$

Over all Lower Cut-off Frequency

$$f_{L_S} = 5.08\ \text{Hz}$$

$$f_{L_C} = 26.53\ \text{Hz}$$

$$f_{L_E} = 215\ \text{Hz}$$

Note that $f_{L_C} > 4 f_{L_S}$

and $f_{L_E} > 4 f_{L_S}$

Hence the overall lower cut-off frequency is

$$f_L = f_{L_E} = 215\ \text{Hz}$$

Example 4.8

For the circuit shown below calculate the following:

(a) r_e

(b) Input resistance R_i

(c) Mid band voltage gains $A_V = \dfrac{V_o}{V_i}$ and $A_{V_S} = \dfrac{V_o}{V_s}$

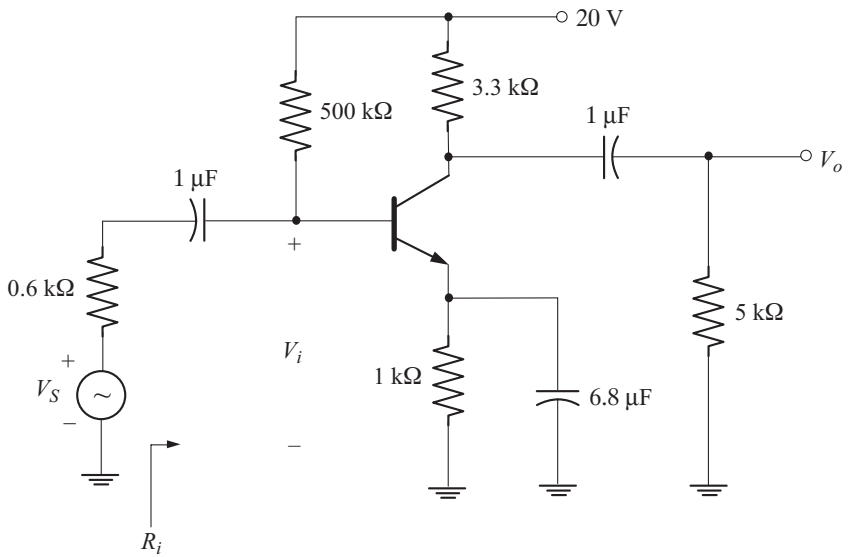
(d) Lower cut-off frequency due to C_S

(e) Lower cut-off frequency due to C_C

(f) Lower cut-off frequency due to C_E

(g) Over all lower cut-off frequency

For the transistor β =100 and $r_o = \infty$.



Solution

(a) ***Calculation of*** r_e

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$= \frac{20\,\text{V} - 0.7\,\text{V}}{500\,\text{k}\Omega + (101)(1\,\text{k}\Omega)} = 32.11\ \mu\text{A}$$

$$I_E = (1+\beta)\, I_B = (101)\ (32.11\ \mu\text{A}) = 3.24\ \text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{3.24\,\text{mA}} = 8.02\ \Omega$$

(b) ***Input Resistance***

$$R_i = R_B \,||\, \beta\, r_e$$

$$= 500\ \text{k}\Omega\ ||\ (100)\ (8.02\ \Omega) = 800.72\ \Omega$$

(c) *Midband Voltage Gain*

$$A_V = \frac{V_o}{V_i} = -\frac{R_o \,||\, R_L}{r_e}$$

$$R_o = R_C \,||\, r_o = 3.3\ \text{k}\Omega \,||\, \infty = 3.3\ \text{k}\Omega$$

$$R_o \,||\, R_L = 3.3\ \text{k}\Omega \,||\, 5\ \text{k}\Omega = 1.98\ \text{k}\Omega$$

$$A_V = -\frac{1.98\ \text{k}\Omega}{8.02\ \Omega} = -246.88$$

$$A_{V_S} = A_V \frac{R_i}{R_S + R_i}$$

$$= [-246.88]\ \frac{800.72\ \Omega}{0.6\ \text{k}\Omega + 800.72\ \Omega} = -141.12$$

(d) *Lower Cut-off Frequency due to C_S*

$$f_{L_S} = \frac{1}{2\pi [R_S + R_i] C_S}$$

$$= \frac{1}{2\pi\ [0.6\ \text{k}\Omega + 800.72\ \Omega][1\ \mu\text{F}]} = 113.6\ \text{Hz}$$

(e) *Lower Cut-off Frequency due to C_C*

$$f_{L_C} = \frac{1}{2\pi\ [R_o + R_L] C_C}$$

$$= \frac{1}{2\pi\ [3.3\ \text{k}\Omega + 5\ \text{k}\Omega][1\ \mu\text{F}]} = 19.17\ \text{Hz}$$

(f) *Lower Cut-off Frequency due to C_E*

$$f_{L_E} = \frac{1}{2\pi R_e C_E}$$

$$R_e = R_E \,||\, \left[\frac{R'_S}{\beta} + r_e\right]$$

$$R'_S = R_B \,||\, R_S = 500\ \text{k}\Omega \,||\, 0.6\ \text{k}\Omega = 599.28\ \Omega$$

$$\frac{R'_S}{\beta} + r_e = \frac{599.28\Omega}{100} + 8.02\ \Omega = 14.01\ \Omega$$

$$R_e = 1\ \text{k}\Omega \,||\, 14.01\ \Omega = 13.82\ \Omega$$

$$f_{L_E} = \frac{1}{2\pi [13.82\Omega][6.8\mu F]} = 1693.5\ \text{Hz}$$

(g) *Over all Lower 3dB Frequency*

$$f_{L_S} = 113.6 \text{ Hz}$$
$$f_{L_C} = 19.17 \text{ Hz}$$
$$f_{L_E} = 1693.5 \text{ Hz}$$

Note that $f_{L_S} > 4\, f_{L_C}$

$f_{L_E} > 4\, f_{L_S}$

Hence the over all lower 3 dB frequency is

$$f_L = f_{L_E} = 1693.5 \text{ Hz}$$

Example 4.9

For the emitter follower circuit shown below, calculate the following:

(a) r_e

(b) Input resistance R_i

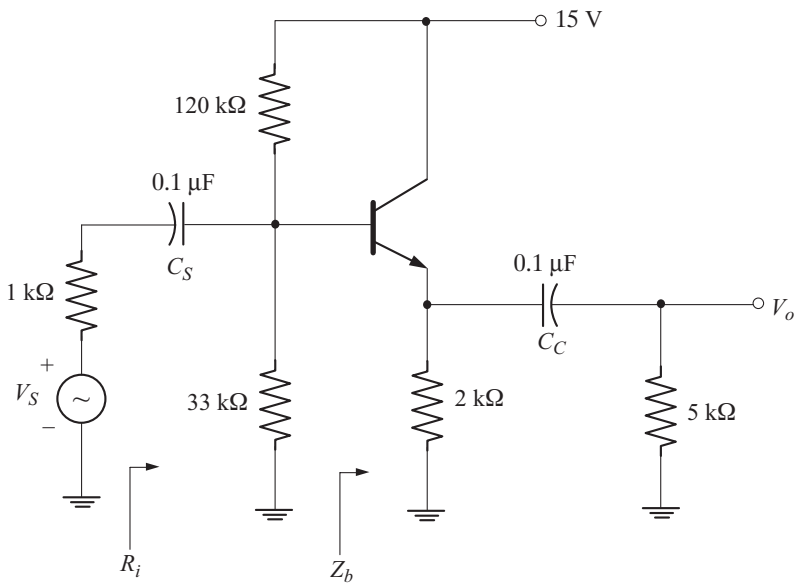
(c) Mid band voltage gains $A_V = \dfrac{V_o}{V_i}$ and $A_{V_S} = \dfrac{V_o}{V_S}$

(d) Lower cut-off frequency due to C_S

(e) Lower cut-off frequency due to C_C

(f) Over all lower cut-off frequency

For the transistor, $\beta = 100$ and $r_o = \infty$.



Solution

(a) ***Calculation of r_e***

$$\beta R_E = (100)\,(2\ \text{k}\Omega\ ) = 200\ \text{k}\Omega$$

$$10\,R_2 = (10)\,(33\ \text{k}\Omega) = 330\ \text{k}\Omega$$

Note that, $\beta R_E < 10\,R_2$

Hence we have to use exact analysis

$$V_{Th} = \frac{V_{CC}\,R_2}{R_1 + R_2} = \frac{(15\ \text{V})(33\ \text{k}\Omega)}{120\ \text{k}\Omega + 33\ \text{k}\Omega} = 3.23\ \text{V}$$

$$R_{Th} = R_1 \,||\, R_2 = 120\ \text{k}\Omega \,||\, 33\ \text{k}\Omega = 25.88\ \text{k}\Omega$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E} = \frac{3.23\,\text{V} - 0.7\,\text{V}}{25.88\ \text{k}\Omega + (101)(2\ \text{k}\Omega)} = 11.1\ \mu\text{A}$$

$$I_E = (1+\beta)\,I_B = (101)\,(11.1\ \mu\text{A}) = 1.12\ \text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\ \text{mV}}{1.12\ \text{mA}} = 23.21\ \Omega$$

(b) ***Input Resistance***

$$R_i = R_1 \,||\, R_2 \,||\, Z_b$$

$$Z_b = \beta\, r_e + (1 + \beta\ )\,[R_E \,||\, R_L]$$

$$= (100)\,(23.21\Omega) + (101)\,[2\text{k}\Omega \,||\, 5\text{k}\Omega] = 146.6\ \text{k}\Omega$$

$$R_i = 120\ \text{k}\Omega \,||\, 33\ \text{k}\Omega \,||\, 146.6\ \text{k}\Omega = 22\ \text{k}\Omega$$

(c) ***Midband Voltage Gain***

$$A_V = \frac{R_E \,||\, R_L}{(R_E \,||\, R_L) + r_e}$$

$$R_E \,||\, R_L = 2\ \text{k}\Omega \,||\, 5\ \text{k}\Omega = 1.43\ \text{k}\Omega$$

$$A_V = \frac{1.43\ \text{k}\Omega}{1.43\ \text{k}\Omega + 23.21\ \Omega} = 0.984$$

$$A_{V_S} = A_V \frac{R_i}{R_S + R_i} = (0.984)\left[\frac{22\ \text{k}\Omega}{22\ \text{k}\Omega + 1\ \text{k}\Omega}\right] = 0.941$$

(d) ***Lower Cut-off Frequency due to C_S***

$$f_{L_S} = \frac{1}{2\pi\left[R_S + R_i\right]C_S}$$

$$= \frac{1}{2\,\pi\left[1\ \text{k}\Omega + 22\ \text{k}\Omega\right]\left[0.1\ \mu\text{F}\right]} = 69.19\ \text{Hz}$$

(e) *Lower Cut-off Frequency due to C_C*

$$f_{L_C} = \frac{1}{2\pi \left[R_o + R_L\right] C_C}$$

$$R_o = R_E \parallel r_e = 2\ \text{k}\Omega \parallel 23.21\ \Omega = 22.94\ \Omega$$

$$f_{L_C} = \frac{1}{2\pi \left[22.94\ \Omega + 5\ \text{k}\Omega\right]\left[0.1\ \mu\text{F}\right]} = 316.85\ \text{Hz}$$

(g) *Over all Lower Cut-off Frequency*

$$f_{L_S} = 66.39\ \text{Hz} \quad f_{L_C} = 316.85\ \text{Hz}$$

Note that $f_{L_C} > 4 f_{L_S}$

Hence f_{L_C} is the over all lower cut-off frequency.

Example 4.10

For the common-base amplifier shown below, calculate the following:

(a) r_e

(b) Input resistance, R_i

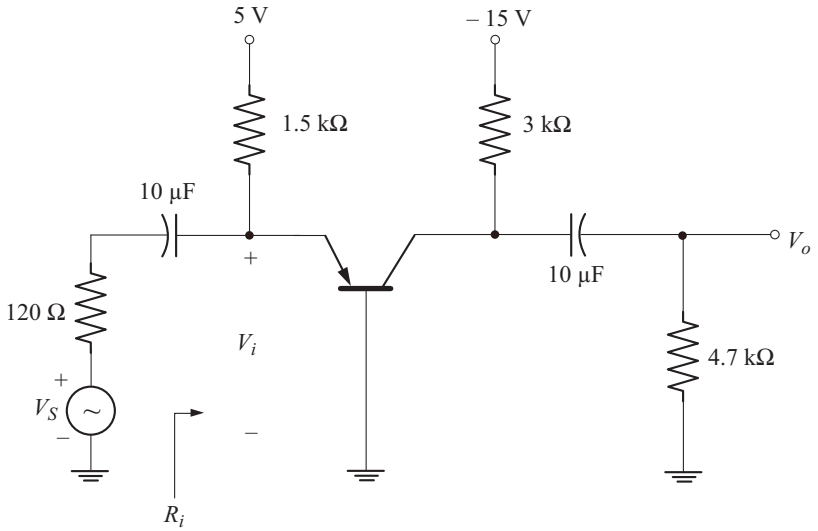
(c) Mid band voltage gains $A_V = \frac{V_o}{V_i}$ and $A_{V_S} = \frac{V_o}{V_S}$

(d) Lower cut-off frequency due to C_S

(e) Lower cut-off frequency due to C_C

(f) Over all lower cut-off frequency.

For the transistor $\beta = 75$ and $r_o = \infty$.



Solution

(a) ***Calculation of*** r_e

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{5\text{ V} - 0.7\text{ V}}{1.5\text{ k}\Omega} = 2.86\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.86\text{ mA}} = 9.09\ \Omega$$

(b) ***Input Resistance***

$$R_i = R_E \,||\, r_e = 1.5\text{ k}\Omega \,||\, 9.09\ \Omega = 9.03\ \Omega$$

(c) ***Midband Voltage Gain***

$$A_V = \frac{\alpha \left[R_C \,||\, R_L\right]}{r_e}$$

$$\alpha = \frac{\beta}{1+\beta} = \frac{75}{76} = 0.986$$

$$R_C \,||\, R_L = 3\text{ k}\Omega \,||\, 4.7\text{ k}\Omega = 1.83\text{ k}\Omega$$

$$A_V = \frac{(0.986)(1.83\text{ k}\Omega)}{9.09\ \Omega} = 198.5$$

$$A_{V_S} = A_V\left[\frac{R_i}{R_S + R_i}\right] = [198.5]\left[\frac{9.03\ \Omega}{120\ \Omega + 9.03\ \Omega}\right] = 13.89$$

(d) ***Lower Cut-off Frequency due to*** C_S

$$f_{L_S} = \frac{1}{2\pi\left[R_S + R_i\right]C_S}$$

$$= \frac{1}{2\pi\left[120\ \Omega + 9.03\ \Omega\right]\left[10\ \mu\text{F}\right]} = 123.34\text{ Hz}$$

(e) ***Lower cut-off Frequency due to*** C_C

$$f_{L_C} = \frac{1}{2\pi\left[R_o + R_L\right]C_C}$$

$$R_o = R_C = 3\text{ k}\Omega$$

$$f_{L_C} = \frac{1}{2\pi\left[3\text{ k}\Omega + 4.7\text{ k}\Omega\right]\left[10\ \mu\text{F}\right]} = 2.06\text{ Hz}$$

(f) ***Over all Lower Cut-off Frequency***

$$f_{L_S} = 123.34\text{ Hz}$$

$$f_{L_C} = 2.06\text{ Hz}$$

Note that $f_{L_S} > 4 f_{L_C}$

$\therefore$ Over all lower cut-off frequency is f_{L_S}

$$f_L = f_{L_S} = 123.34 \text{ Hz}$$

Example 4.11

It is desired that the voltage gain of an RC-coupled amplifier at 60 Hz should not decrease by more than 10 % from its mid band value. Show that the coupling capacitor C_S must be at least equal to $\frac{5.5}{R}$ where $R = R_S + R_i$. R is in kilo-ohms and C_S in micro farads. Neglect the effects of C_E and C_C.

Solution

(a) Voltage gain in low frequency region is given by

$$|A_V| = \frac{1}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}} \quad \text{(A)}$$

at $f = 60$ Hz, $|A_V| > 0.9$

Using this data in Equation (A), we have

$$\frac{1}{\sqrt{1+\left(\frac{f_L}{60}\right)^2}} > 0.9$$

$$\Rightarrow \quad 1+\left(\frac{f_L}{60}\right)^2 < 1.235$$

or $f_L < 29$ Hz

(b) Since the effects of C_C and C_E are to be neglected,

$$f_L = f_{L_S}$$

But $$f_{L_S} = \frac{1}{2\pi [R_S + R_i] C_S} < 29 \text{ Hz}$$

$$2\pi [R_S + R_i] C_S > \frac{1}{29}$$

$$C_S > \frac{1}{(2\pi)(29)(R_S + R_i)}$$

Since C_S is in micro Farad and $R = R_S + R_i$ in kilo-ohms we have

$$C_S\,[10^{-6}] > \frac{1}{(2\pi)(29)(R)(10^3)}$$

$$C_S > \frac{5.5}{R}$$

Example 4.12

It is desired that the lower cut-off frequency due to C_S be not more than 10 Hz for the RC-coupled amplifier of Fig. 4.13. Calculate the minimum value of input coupling capacitor C_S. Take $R_1 = 39\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_S = 1\ \text{k}\Omega$, $\beta = 100$, $V_{CC} = 10$ V.

Solution

Given $f_{L_S} < 10\text{Hz}$

$$f_{L_S} = \frac{1}{2\pi\,[R_S + R_i]\,C_S} < 10\ \text{Hz}$$

$$2\pi\,[R_S + R_i]\,C_S > 0.1$$

$$C_S > \frac{0.1}{2\pi\,[R_S + R_i]}$$

$R_i = 2.13\ \text{k}\Omega$ [see example 4.5]

$$C_S > \frac{0.1}{2\pi[1\,\text{k}\Omega + 2.13\,\text{k}\Omega]}$$

$$C_S > 5.08\ \mu\text{F}$$

◆ 4.4 MILLER EFFECT CAPACITANCE

Figure 4.22 shows an inverting amplifier with a capacitance C_f between the input and output nodes.

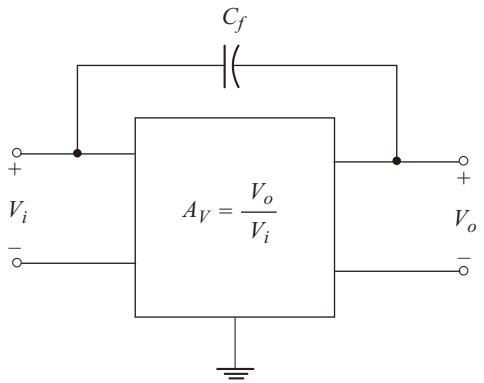


Fig. 4.22 Inverting amplifier with capacitance between input and output nodes

It is important to note that, A_V is negative for inverting amplifier since V_o and V_i are 180° out of phase. Using Millers theorem we can find the loading effect of C_f on the input and output circuits of the amplifier.

To find the Miller Input Capacitance [C_{M_i}]

We use the circuit of Fig. 4.23 to find the Miller input capacitance.

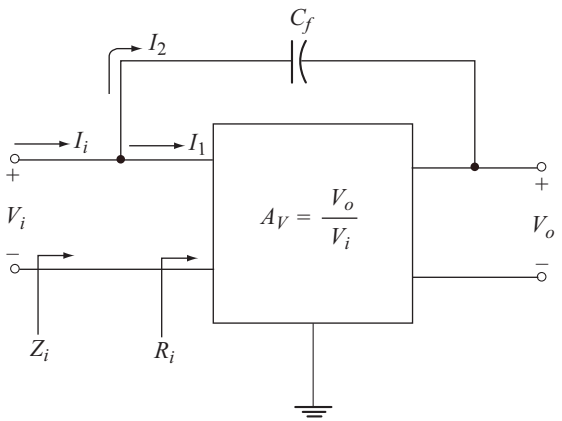


Fig. 4.23 Circuit to find Miller input capacitance

Let $$R_i = \frac{V_i}{I_1} \Rightarrow I_1 = \frac{V_i}{R_i}$$

and $$Z_i = \frac{V_i}{I_i} \Rightarrow I_i = \frac{V_i}{Z_i}$$

Applying KCL at the input node we have

$$I_i = I_1 + I_2 \tag{4.42}$$

$$I_2 = \frac{V_i - V_o}{X_{C_f}}$$

$$= \frac{V_i - A_V V_i}{X_{C_f}} \qquad [\because V_o = A_V V_i]$$

$$I_2 = \frac{[1 - A_V]V_i}{X_{C_f}}$$

Substituting for I_i, I_1 and I_2 in Equation (4.42) we get

$$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{[1 - A_V]V_i}{X_{C_f}}$$

Eliminating V_i throughout we have

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{\left[\frac{X_{C_f}}{1-A_V}\right]}$$

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_{Mi}}} \tag{4.43}$$

where $$X_{C_{Mi}} = \frac{X_{C_f}}{1-A_V} \tag{4.44}$$

$$X_{C_f} = \frac{1}{2\pi f C_f}$$

Using this relation in Equation (4.44) we have

$$X_{C_{Mi}} = \frac{1}{2\pi f [1-A_V] C_f}$$

$$X_{C_{Mi}} = \frac{1}{2\pi f C_{Mi}} \tag{4.45}$$

where $$C_{Mi} = [1-A_V]\, C_f \tag{4.46}$$

C_{Mi} is called the Miller input capacitance.

From Equation (4.43), Z_i can be interpreted as the impedance resulting from the parallel combination of R_i and C_{Mi}. This is shown in Fig. 4.24.

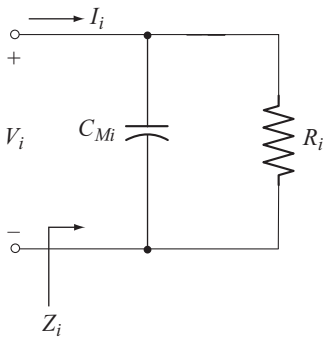


Fig 4.24 Miller input capacitance [C_{Mi}]

To find the Miller Output Capacitance [C_{Mo}]

We use the circuit of Fig. 4.25 to find the miller output capacitance.

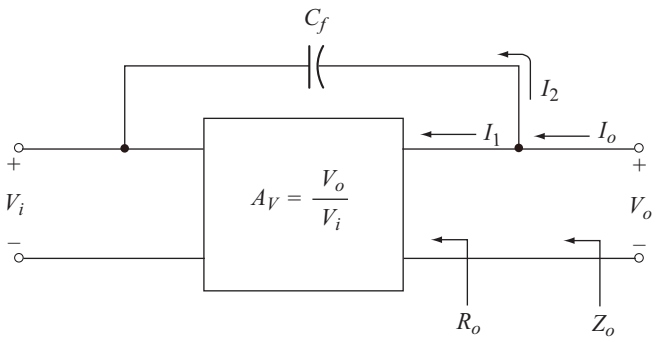


Fig 4.25 Circuit to find miller output capacitance

Let $$R_o = \frac{V_o}{I_1} \Rightarrow I_1 = \frac{V_o}{R_o}$$

and $$Z_o = \frac{V_o}{I_o} \Rightarrow I_o = \frac{V_o}{Z_o}$$

Appling KCL at the output node we have

$$I_o = I_1 + I_2 \tag{4.47}$$

$$I_2 = \frac{V_o - V_i}{X_{C_f}}$$

Using $V_i = \frac{V_o}{A_V}$ we have

$$I_2 = \frac{V_o - \frac{V_o}{A_V}}{X_{C_f}} = \frac{V_o\left[1 - \frac{1}{A_V}\right]}{X_{C_f}}$$

Substituting for I_1 and I_2 into Equation (4.47) we have

$$I_o = \frac{V_o}{R_o} + \frac{V_o\left[1 - \frac{1}{A_V}\right]}{X_{C_f}}$$

Usually R_o is large and hence the term $\frac{V_o}{R_o}$ can be neglected.

Now $$I_o \approx \frac{V_o\left[1 - \frac{1}{A_V}\right]}{X_{C_f}}$$

$$Z_o = \frac{V_o}{I_o} = \frac{X_{C_f}}{\left[1 - \frac{1}{A_V}\right]}$$

$$Z_o = \frac{1}{2\pi f \left[1 - \frac{1}{A_V}\right] C}$$

$$Z_o = \frac{1}{2\pi f C_{Mo}} \tag{4.48}$$

where $$C_{Mo} = \left[1 - \frac{1}{A_V}\right] C_f \tag{4.49}$$

C_{Mo} is called the miller output capacitance.

Summary of Millers Theorem

A capacitance C_f connected between the input and output nodes of an inverting amplifier can be replaced by

- A miller input capacitance, $C_{Mi} = [1 - A_V]\, C_f$ connected between input node and ground and
- A miller output capacitance, $C_{Mo} = \left[1 - \frac{1}{A_V}\right] C_f$ connected between output node and ground.

For non inverting amplifier A_V is positive. In order to obtain positive values for C_{Mi} and C_{Mo}, Equations (4.46) and (4.49) should be modified as follows

$$C_{Mi} = [1 + A_V]\, C_f \tag{4.50}$$

$$C_{Mo} = \left[1 + \frac{1}{A_V}\right] C_f \tag{4.51}$$

Application of millers theorem to the amplifier of Fig. 4.25 results in the network shown in Fig. 4.26.

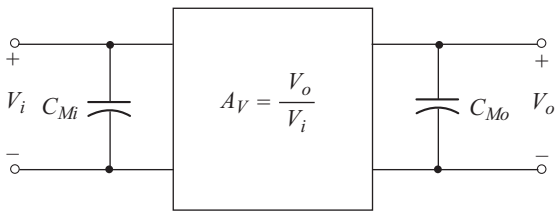


Fig. 4.26 Amplifier with C_f replaced by Miller capacitances

Applications of Millers Theorem

Millers theorem is applied:

- In feed back amplifier circuits to replace the feed back resistors / impedances connected between input and output nodes with their miller input and output impedances. An example is a voltage shunt feed back amplifier discussed in Chapter 6.
- In high frequency analysis of amplifiers to replace the internal capacitances of active devices with their miller input and output capacitances. This application is discussed in the next section.

◆ 4.5 HIGH-FREQUENCY RESPONSE OF BJT AMPLIFIER

In the high frequency response of BJT amplifier, the upper 3-dB cut-off point is defined by the following two factors.

- The network capacitance which includes the parasitic capacitances of the transistor and the wiring capacitances.
- The frequency dependence of the short circuit common emitter current gain h_{fe} or β.

4.5.1 Network Parameters

Figure 4.27 shows the RC-coupled amplifier with parasitic and wiring capacitances. C_{be}, C_{bc} and C_{ce} are the parasitic capacitances of the transistor. C_{Wi} and C_{Wo} are the input and output wiring capacitances which are introduced during the construction of the amplifier circuit.

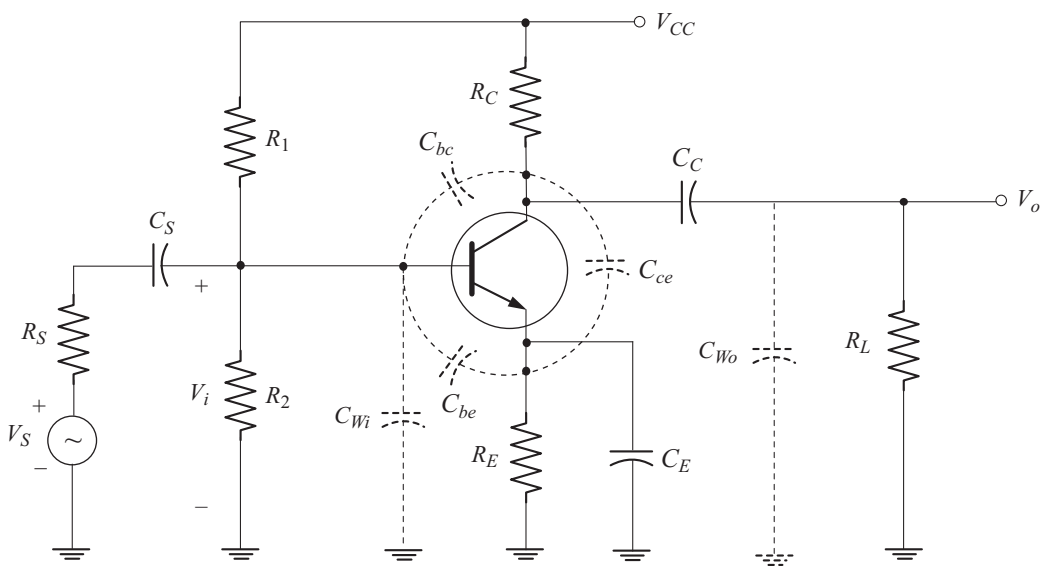


Fig. 4.27 RC-coupled amplifier with parasitic and wiring capacitances

Figure 4.28 shows the high frequency ac equivalent circuit of the RC-coupled amplifier.

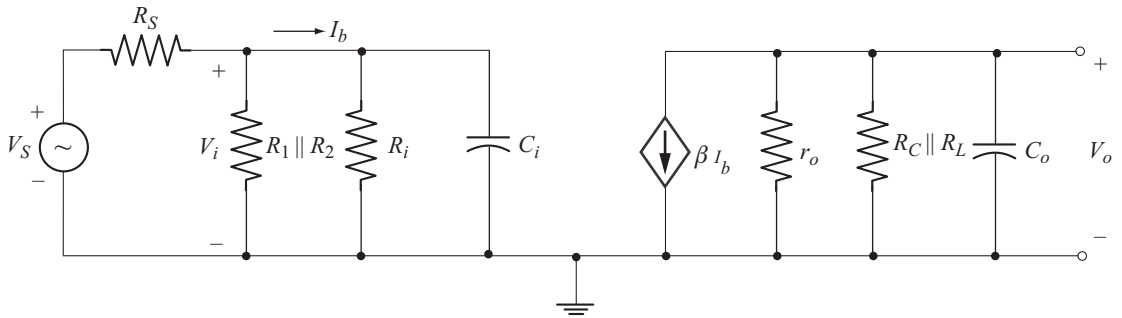


Fig. 4.28 High frequency ac equivalent circuit of the amplifier of Fig 4.27

- Using Millers theorem, the transition capacitance, C_{bc} can be replaced by two capacitances: C_{Mi} at the input and C_{Mo} at the output.
- The total input capacitance C_i, is the sum of the miller input capacitance C_{Mi}, base-emitter input capacitance C_{be} and the input wiring capacitance C_{Wi}

$$C_i = C_{Wi} + C_{be} + C_{Mi} \tag{4.52}$$

where $$C_{Mi} = [1 - A_V] C_{bc} \tag{4.53}$$

- The total output capacitance C_o, is the sum of the miller output capacitance C_{M_o}, the collector-emitter parasitic capacitance C_{Ce} and the output wiring capacitance C_{W_i}

$$C_o = C_{W_o} + C_{ce} + C_{Mo} \tag{4.54}$$

where $$C_{Mo} = \left[1 - \frac{1}{A_V}\right] C_{bc} \tag{4.55}$$

Upper Cut-off Frequency due to Input Capacitance C_i

To find the upper cut-off frequency due to the input capacitance C_i, we consider the input circuit of Fig. 4.28 which is shown in Fig. 4.29(a).

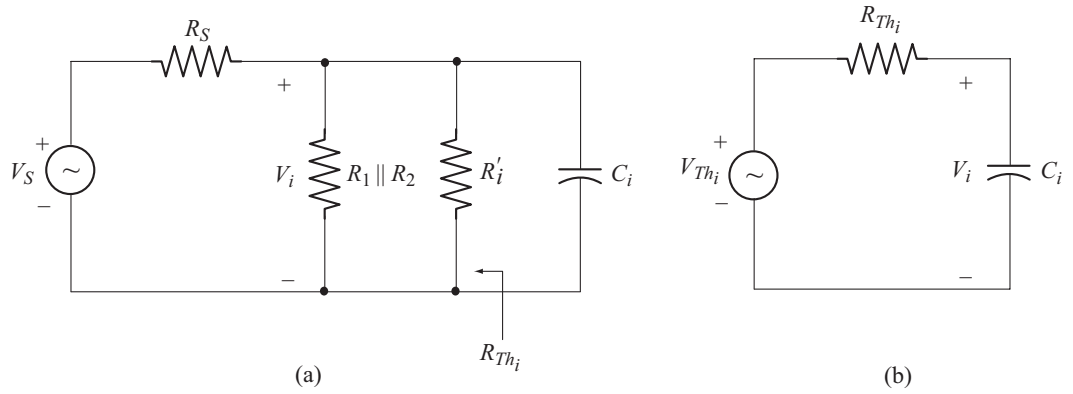


Fig. 4.29 (a) Input ac equivalent circuit (b) Thevenin equivalent of input circuit

The network consisting of V_S, R_S, $R_1 \parallel R_2$ and R_i' can be replaced by its Thevenin equivalent as shown in Fig. 4.29(b).

The Thevenin voltage V_{Th_i} and Thevenin resistance R_{Th_i} can be calculated using the networks of Fig. 4.30(a) and 4.30(b) respectively.

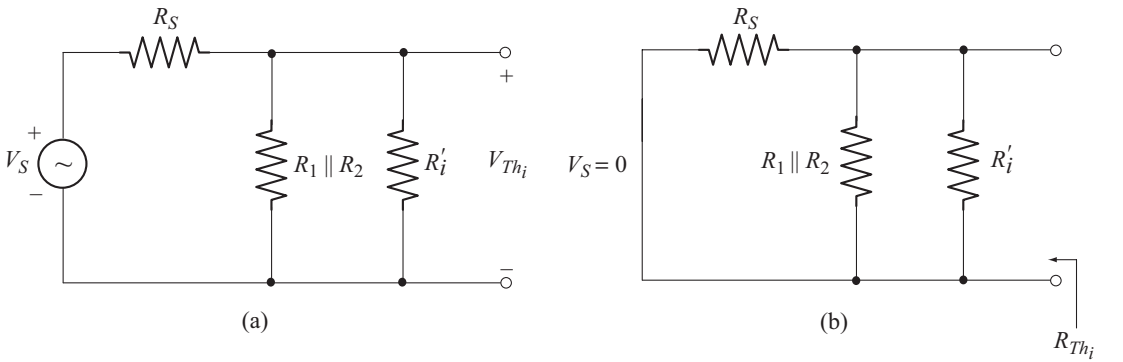


Fig. 4.30 (a) Circuit to find V_{Th_i} (b) Circuit to find R_{Th_i}

Using voltage division rule in the circuit of Fig. 4.30(a), we have

$$V_{Th_i} = V_S \left[\frac{R_1 \parallel R_2 \parallel R_i'}{R_S + R_1 \parallel R_2 \parallel R_i'} \right] \tag{4.56}$$

and from the circuit of Fig. 4.30(b)

$$R_{Th_i} = R_S \parallel R_1 \parallel R_2 \parallel R_i' \tag{4.57}$$

where $R_i' = \beta r_e$.

Now let us find the amplifier input voltage V_i, as a function of frequency from the circuit of Fig. 4.29(b).

Using voltage division rule we have

$$| V_i | = | V_{Th_i} | \left[\frac{X_{C_i}}{\sqrt{\left(R_{Th_i}\right)^2 + \left[X_{C_i}\right]^2}} \right]$$

$$| V_i | = \frac{| V_{Th_i} |}{\sqrt{1 + \left[\frac{R_{Th_i}}{X_{C_i}}\right]^2}} \tag{4.58}$$

where $$X_{C_i} = \frac{1}{2\pi f C_i} \tag{4.59}$$

- In the midband, the effect of C_i is negligible. As a result X_{C_i} can be treated as open circuit (i.e., $X_{C_i} = \infty$)

$$\therefore \qquad |V_i|_{\text{mid}} \approx |V_{Th_i}|$$

- At high frequencies, C_i comes into play. With increase in frequency, X_{C_i} decreases, $\frac{R_{Th_i}}{X_{C_i}}$ increases, $|V_i|$ decreases and hence the voltage gain decreases.

3dB cut-off occurs at a frequency at which

$$|V_i| = \frac{|V_i|_{\text{mid}}}{\sqrt{2}} = \frac{|V_{Th_i}|}{\sqrt{2}}$$

From Equation (4.58) we find that, this condition occurs when

$$R_{Th_i} = X_{C_i}$$

$$R_{Th_i} = \frac{1}{2\pi f C_i}$$

or
$$f = \frac{1}{2\pi R_{Th_i} C_i} \tag{4.60}$$

Equation (4.60) gives the upper 3 dB cutoff frequency due to the input capacitance C_i. Let us denote it by f_{H_i}

$$f_{H_i} = \frac{1}{2\pi R_{Th_i} C_i} \tag{4.61}$$

Consider
$$\frac{R_{Th_i}}{X_{C_i}} = \frac{R_{Th_i}}{\left[\frac{1}{2\pi f C_i}\right]} = f[2\pi R_{Th_i} C_i]$$

$$= \left[\frac{f}{f_{H_i}}\right]$$

Using this relation in Equation (4.58) we have

$$|V_i| = \frac{|V_{Th_i}|}{\sqrt{1+\left[\frac{f}{f_{H_i}}\right]^2}} \tag{4.62}$$

Based on the above relation we can write

$$|A_V| = \frac{1}{\sqrt{1+\left[\frac{f}{f_{H_i}}\right]^2}} \tag{4.63}$$

Figure 4.31 shows the Bode plot of $|A_V|_{dB}$ obtained using Equation (4.63).

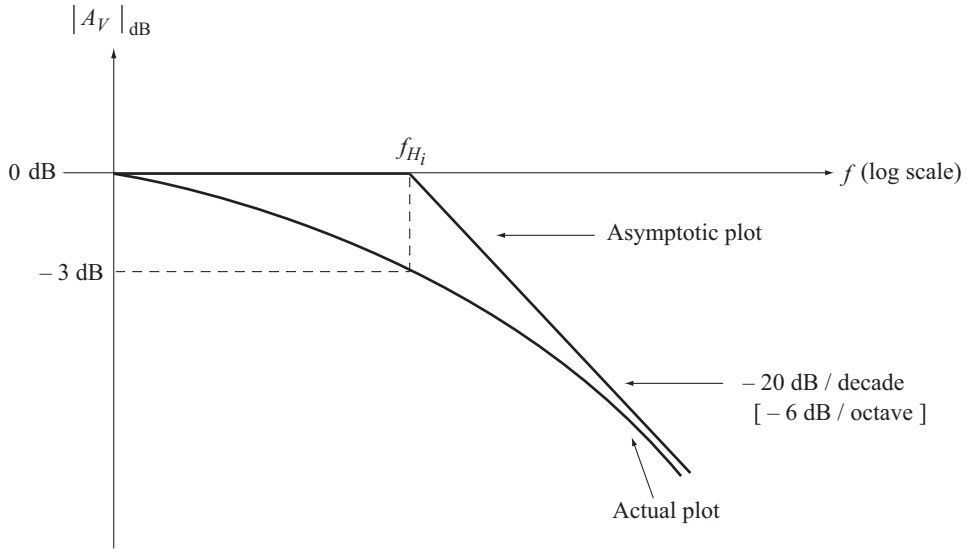


Fig. 4.31 Bode plot of equation (4.63)

Note that due to C_i, the voltage gain decreases at the rate of 20 dB / decade or 6 dB / octave in the high frequency region.

Upper Cut-off Frequency due to Output Capacitance C_o

To find the upper cut-off frequency due to output capacitance C_o, we consider the output circuit of Fig. 4.28 which is shown in Fig. 4.32.

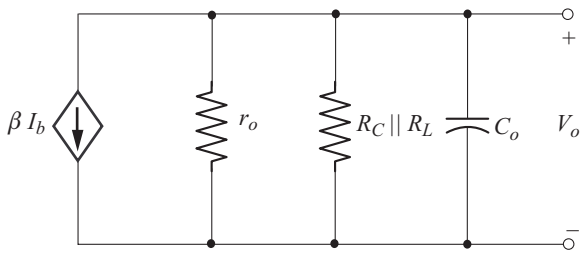


Fig. 4.32 Output ac equivalent circuit

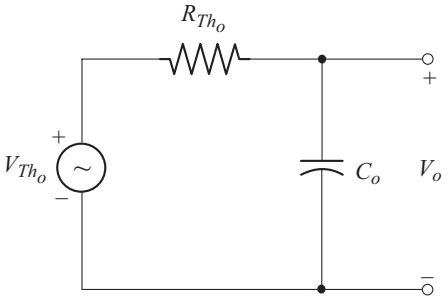


Fig. 4.33 Simplified output ac equivalent circuit

The current source βI_b along with the resistors r_o and $R_C \| R_L$ can be converted into its equivalent voltage source as shown in Fig. 4.33.

$$R_{Th_o} = r_o \| R_C \| R_L \tag{4.64}$$

$$V_{Th_o} = [-\beta I_b] [r_o \| R_C \| R_L] \tag{4.65}$$

Using the procedure given in the previous section we can deduce the following relations for the circuit of Fig. 4.33.

The output voltage as a function of frequency is

$$|V_o| = \frac{|V_{Th_o}|}{\sqrt{1+\left[\frac{R_{Th_o}}{X_{C_o}}\right]^2}} \tag{4.66}$$

where $$X_{C_o} = \frac{1}{2\pi f C_o} \tag{4.67}$$

The output voltage in the mid band is

$$|V_o|_{\text{mid}} \approx |V_{Th_o}| \tag{4.68}$$

The upper 3dB cutoff frequency due to C_o is

$$f_{H_o} = \frac{1}{2\pi R_{Th_o} C_o} \tag{4.69}$$

and the magnitude of voltage gain is

$$|A_V| = \frac{1}{\sqrt{1+\left[\frac{f}{f_{H_o}}\right]^2}} \tag{4.70}$$

Figure 4.34 shows the bode plot of Equation (4.70).

Note that due to C_o, the voltage gain decreases at the rate of 20 dB/decade or 6 dB/octave.

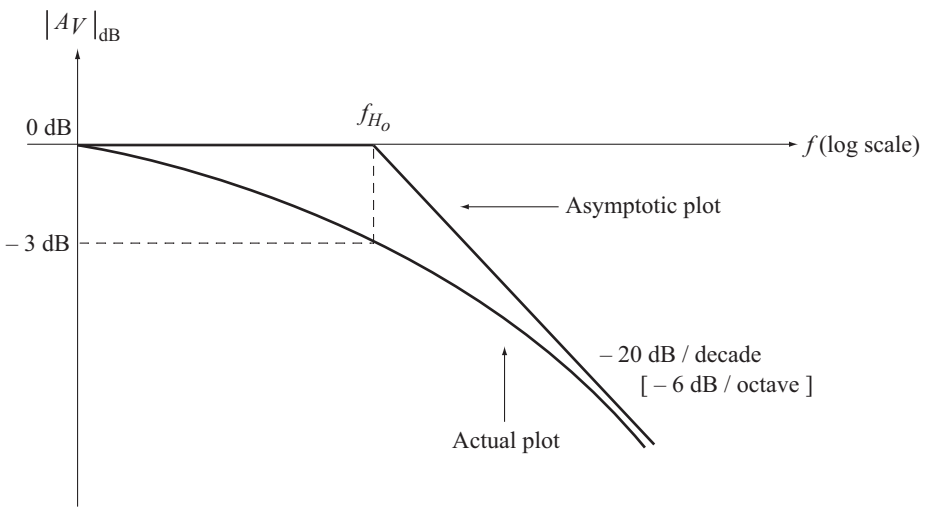


Fig. 4.34 Bode plot of equation (4.70)

Combined Effect of C_i and C_o on High Frequency Response

- The input capacitance C_i defines the upper cut-off frequency f_{H_i}
- The output capacitance C_o, defines another upper cut-off frequency f_{H_o}
- The lowest of these two frequencies will be taken as the overall upper-cutoff frequency.
- If the variation of h_{fe} with frequency is considered then the actual cut-off frequency may be lower than f_{H_i} or f_{H_o}.

4.5.2 Variation of h_{fe} (or β) with Frequency

Figure 4.35 shows the hybrid-π high frequency small signal model of BJT. Detailed explanation of this model is given in section 3.17 of Chapter 3.

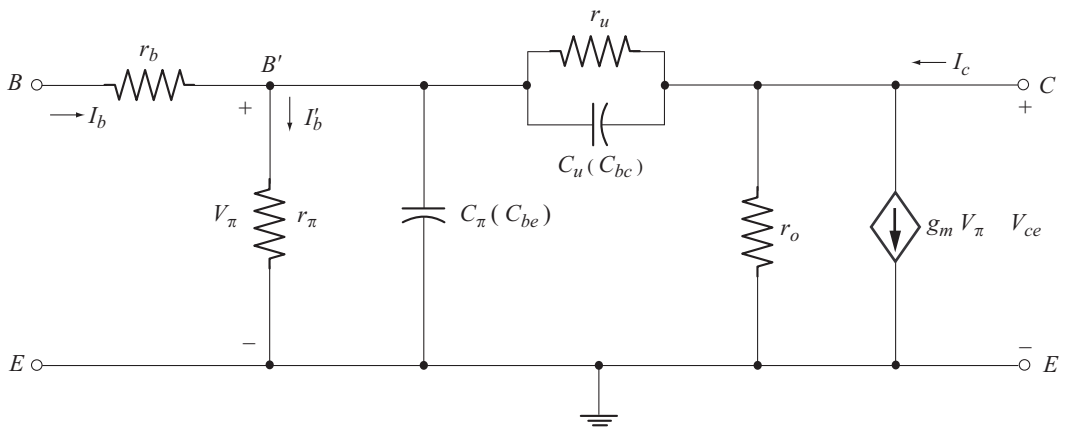


Fig. 4.35 Hybrid-π high frequency small signal model of BJT

The base-emitter input capacitance C_π (C_{be}) and the base-collector depletion capacitance C_u (C_{bc}) makes the short circuit current gain h_{fe} to vary with frequency in the high frequency region.

4.5.3 Expression for h_{fe} as a Function of Frequency

To simplify the analysis we make the following reasonable approximations:

- r_b is typically a few tens of ohms. Hence it can be treated as short circuit.
- r_u is typically a few tens of mega ohms. Hence it can be treated as open circuit.

To find the short circuit current gain, we short the output terminals. As a result r_o gets short circuited. The resulting circuit is shown in Fig. 4.36.

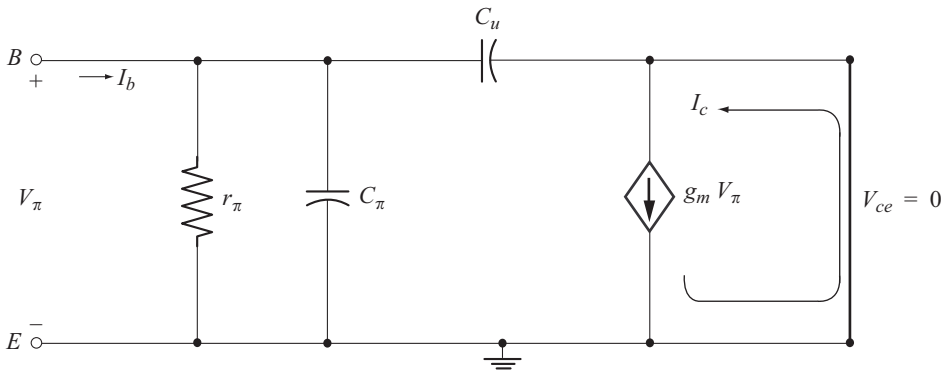


Fig. 4.36 Circuit to find short circuit current gain

Short circuit current gain is

$$h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce}=0} \tag{4.71}$$

The current $g_m V_\pi$ flows into the short circuit.

$$\therefore \quad I_c = g_m V_\pi \tag{4.72}$$

To find I_b, let us consider the input circuit of Fig. 4.36 which is shown in Fig. 4.37.

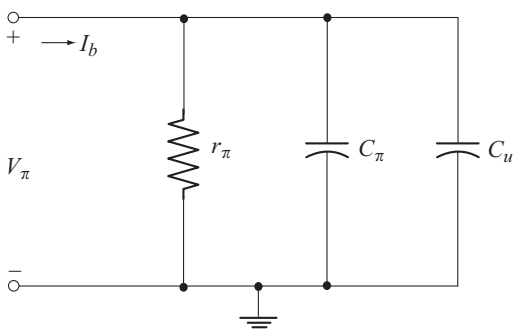


Fig. 4.37 Circuit to find I_b

Let
$$Z = r_\pi \parallel \frac{1}{j\,\omega\,[C_\pi + C_u]} \tag{4.73}$$

$$Z = \frac{r_\pi}{1 + j\,\omega\, r_\pi [C_\pi + C_u]}$$

Now
$$V_\pi = I_b Z$$

$$V_\pi = \frac{I_b r_\pi}{1 + j\,\omega\, r_\pi [C_\pi + C_u]} \tag{4.74}$$

Substituting Equation (4.74) in Equation (4.72) we have

$$I_c = \frac{g_m r_\pi I_b}{1 + j\,\omega\, r_\pi \left[C_\pi + C_u\right]}$$

Now
$$h_{fe} = \frac{I_c}{I_b} = \frac{g_m r_\pi}{1 + j\,2\,\pi f\, r_\pi \left[C_\pi + C_u\right]} \tag{4.75}$$

Let
$$f_\beta = \frac{1}{2\,\pi\, r_\pi \left[C_\pi + C_u\right]} \tag{4.76}$$

Using Equation (4.76) in Equation (4.75) we have

$$h_{fe} = \frac{g_m r_\pi}{1 + j\left[\frac{f}{f_\beta}\right]} \tag{4.77}$$

$$|h_{fe}| = \frac{g_m r_\pi}{\sqrt{1 + \left[\frac{f}{f_\beta}\right]^2}} \tag{4.78}$$

In the mid band, $f \ll f_\beta$. As a result $\left[\frac{f}{f_\beta}\right]^2 \ll 1$

From Equation (4.78) we have

$$|h_{fe}|_{\text{mid}} = g_m r_\pi = h_{fe\,\text{mid}} \tag{4.79}$$

$h_{fe\,\text{mid}}$ is also denoted by β_{mid}

Using Equation (4.79) in Equation (4.78) we have

$$|h_{fe}| = \frac{h_{fe\,\text{mid}}}{\sqrt{1 + \left[\frac{f}{f_\beta}\right]^2}} \tag{4.80}$$

Equation (4.80) gives the variation of $|h_{fe}|$ with frequency.

- As the frequency increases, $\left[\frac{f}{f_\beta}\right]^2$ increases and hence $|h_{fe}|$ decreases.
- When $f = f_\beta$

$$|h_{fe}| = \frac{h_{fe\,\text{mid}}}{\sqrt{2}} = \frac{\beta_{\text{mid}}}{\sqrt{2}}$$

Note that f_β defines the upper 3-dB cut-off point for the short circuit current gain h_{fe} . f_β is also denoted by $f_{h_{fe}}$. Now Equation (4.76) can be written as

$$f_\beta = f_{h_{fe}} = \frac{1}{2\pi r_\pi \left[C_\pi + C_u\right]} \tag{4.81}$$

Using $r_\pi = \beta r_e = \beta_{\text{mid}} r_e$ we have

$$f_\beta = f_{h_{fe}} = \frac{1}{2\pi \beta_{\text{mid}} r_e \left[C_\pi + C_u\right]} \tag{4.82}$$

f_β is called the β cut-off frequency. f_β is also the bandwidth for the short circuit current gain h_{fe}.

Figure 4.38 shows the variation of $|h_{fe}|$ with frequency. Note that $|h_{fe}|$ decreases from its mid band value $h_{fe\,\text{mid}}$ with a slope of 20 dB/decade or 6 dB/octave.

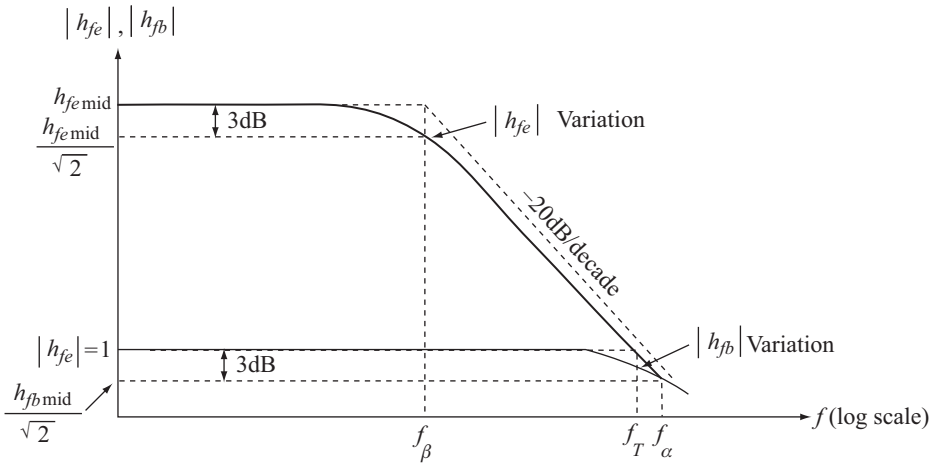


Fig. 4.38 Plot of $|h_{fe}|$ and $|h_{fb}|$ versus frequency in the high-frequency region

4.5.4 Expression for the gain-band width product [f_T]

The gain-band width product, f_T is the frequency at which $|h_{fe}| = 1$ or $|h_{fe}|_{\text{dB}} = 0$ dB.

Substituiting this condition in Equation (4.80) we have

$$\left.\frac{h_{fe\,\text{mid}}}{\sqrt{1+\left[\frac{f}{f_\beta}\right]}}\right|_{f=f_T} = 1$$

$$\frac{h_{fe\,\text{mid}}}{\sqrt{1+\left[\frac{f_T}{f_\beta}\right]^2}} = 1 \tag{4.83}$$

Since $f_T \gg f_\beta$,

$$\left[\frac{f_T}{f_\beta}\right]^2 \gg 1$$

$$\therefore \quad \sqrt{1+\left[\frac{f_T}{f_\beta}\right]^2} \approx \frac{f_T}{f_\beta}$$

Using this relation in Equation (4.83) we have

$$\frac{h_{fe\,\text{mid}}}{\left[\frac{f_T}{f_\beta}\right]} = 1$$

or
$$f_T = h_{fe\,\text{mid}}\, f_\beta = \beta_{\text{mid}}\, f_\beta \tag{4.84}$$

Note that $h_{fe\,\text{mid}}$ is the midband short circuit current gain and f_β is the bandwidth.
For this reason f_T is called the gain-bandwidth product.
Substituting Equation (4.82) into Equation (4.84) we have

$$f_T = \beta_{\text{mid}} \cdot \frac{1}{2\,\pi\,\beta_{\text{mid}}\, r_e [C_\pi + C_u]}$$

$$f_T = \frac{1}{2\,\pi\, r_e [C_\pi + C_u]} \tag{4.85}$$

4.5.5 Expression for α Cut-off Frequency [f_α]

Figure 4.38 also shows the plot of $|h_{fb}|$ versus frequency. It is important to note that $h_{fb\,\text{mid}} = 1$, since the short circuit current gain in CB configuration is unity.

α cut-off frequency, f_α is the frequency at which $|h_{fb}|$ drops to $\frac{h_{fb\ \text{mid}}}{\sqrt{2}}$. It is also frequency at which $|h_{fe}|$ drops to $\frac{1}{\sqrt{2}}$. Using this condition in Equation (4.78), it can be shown that

$$f_\beta = f_\alpha [\,1 - \alpha\,] \tag{4.86}$$

where
$$\alpha = \alpha_{\text{mid}} = h_{fb\,\text{mid}} \tag{4.87}$$

Example 4.13

Consider the circuit of Example 4.5 with the same parameter values. Calculate the following

(a) f_{H_i} and f_{H_o}

(b) f_β and f_T

Take C_π (C_{be}) = 35 pF $\quad C_u$ (C_{bc}) = 5 pF $\quad C_{ce}$ = 1 pF $\quad C_{Wi}$ = 6 pF $\quad C_{Wo}$ = 10 pF.

Solution

$$\left.\begin{aligned} r_e &= 29.1\ \Omega \\ A_V &= -99.28 \end{aligned}\right\} \quad \text{From example 4.5}$$

(a)

$$f_{H_i} = \frac{1}{2\pi R_{Th_i} C_i}$$

$$R_{Th_i} = R_S \,||\, R_1 \,||\, R_2 \,||\, R_i'$$

$$R_i' = \beta r_e = (100)\,(29.1\ \Omega) = 2.91\ \text{k}\Omega$$

$$R_{Th_i} = 1\ \text{k}\Omega \,||\, 39\ \text{k}\Omega \,||\, 10\ \text{k}\Omega \,||\, 2.91\ \text{k}\Omega = 0.68\ \text{k}\Omega$$

$$C_i = C_{Wi} + C_{be} + C_{Mi}$$

$$= 6\ \text{pF} + 35\ \text{pF} + [\,1 - (-98.28)\,]\,5\ \text{pF} = 537.4\ \text{pF}$$

$$f_{H_i} = \frac{1}{2\pi\,[0.68\ \text{k}\Omega][537.4\ \text{pF}]} = 435.52\ \text{kHz}$$

$$f_{H_o} = \frac{1}{2\pi R_{Th_o} C_o}$$

$$R_{Th_o} = r_o \,||\, R_C \,||\, R_L = \infty \,||\, 4\ \text{k}\Omega \,||\, 10\ \text{k}\Omega = 2.857\ \text{k}\Omega$$

$$C_o = C_{Wo} + C_{ce} + C_{Mo}$$

$$= 10\ \text{pF} + 1\ \text{pF} + \left[1 - \frac{1}{-98.28}\right] 5\ \text{pF} = 16.05\ \text{pF}$$

$$f_{H_o} = \frac{1}{2\pi\,[2.857\,\text{k}\Omega]\,[16.05\,\text{pF}]} = 3.47\ \text{MHz}$$

(b)

$$f_\beta = \frac{1}{2\pi\,\beta_{\text{mid}}\,r_e\,[C_\pi + C_u]}$$

$$\beta_{\text{mid}} = \beta = 100$$

$$f_\beta = \frac{1}{2\pi(100)[29.1\ \Omega][35\ \text{pF} + 5\ \text{pF}]} = 1.367\ \text{MHz}$$

$$f_T = \beta_{\text{mid}}\, f_\beta = (100)\,(1.367\ \text{MHz}) = 136.7\ \text{MHz}$$

Example 4.14

For the circuit of Example 4.8 with the same parameter values, calculate the following

(a) f_{H_i} and f_{H_o}

(b) f_β and f_T

Take $C_{Wi} = 7$ pF $\quad C_{Wo} = 11$ pF $\quad C_{bc} = 5$ pF $\quad C_{be} = 20$ pF $\quad C_{ce} = 10$ pF.

Solution

$$\left.\begin{aligned} r_e &= 8.02\ \Omega \\ A_V &= -246.88 \end{aligned}\right\} \quad \text{From example 4.8}$$

(a)

$$f_{H_i} = \frac{1}{2\pi R_{Th_i} C_i}$$

$$R_{Th_i} = R_S \parallel R_B \parallel R_i'$$

$$R_i' = \beta r_e = (100)(8.02\ \Omega) = 802\ \Omega$$

$$R_{Th_i} = 0.6\ \text{k}\Omega \parallel 500\ \text{k}\Omega \parallel 802\ \Omega = 342.98\ \Omega$$

$$C_i = C_{Wi} + C_{be} + C_{Mi}$$

$$= 7\ \text{pF} + 20\ \text{pF} + [1 - (-246.88)]\ 5\ \text{pF}$$

$$= 1.266\ \text{nF}$$

$$f_{H_i} = \frac{1}{2\pi[342.98\ \Omega][1.266\ \text{nF}]} = 366.53\ \text{kHz}$$

$$f_{H_o} = \frac{1}{2\pi R_{Th_o} C_o}$$

$$R_{Th_o} = r_o \parallel R_C \parallel R_L$$

$$= \infty \parallel 3.3\ \text{k}\Omega \parallel 5\ \text{k}\Omega$$

$$= 1.987\ \text{k}\Omega$$

$$C_o = C_{Wo} + C_{ce} + C_{Mo}$$

$$= 11\ \text{pF} + 10\ \text{pF} + \left[1 - \frac{1}{-246.88}\right] 5\ \text{pF}$$

$$= 26.02\ \text{pF}$$

$$f_{H_o} = \frac{1}{2\pi[1.987\ \text{k}\Omega][26.02\ \text{pF}]} = 3.07\ \text{MHz}$$

(b)

$$f_\beta = \frac{1}{2\pi \beta_{\text{mid}}\ r_e\ [C_{be} + C_{bc}]}$$

$$= \frac{1}{2\pi\ [100]\ [8.02\ \Omega]\ [20\ \text{pF} + 5\ \text{pF}]}$$

$$= 7.93\ \text{MHz}$$

$$f_T = \beta_{\text{mid}}\ f_\beta$$

$$= (100)\ (7.93\ \text{MHz}) = 793\ \text{MHz}$$

Example 4.15

Consider the circuit of Example 4.9 with the same parameter values. Calculate the following

(a) f_{H_i} and f_{H_o}

(b) f_β and f_T

Take $C_{Wi} = 7$ pF $\quad C_{Wo} = 10$ pF $\quad C_{bc} = 15$ pF $\quad C_{be} = 25$ pF $\quad C_{ce} = 12$ pF.

Solution

$$\left.\begin{aligned} r_e &= 23.21\ \Omega \\ Z_b &= 146.6\ \text{k}\Omega \end{aligned}\right\} \text{ From example 4.9}$$

(a)
$$f_{H_i} = \frac{1}{2\pi R_{Th_i} C_i}$$

$$R_{Th_i} = R_S \,||\, R_1 \,||\, R_2 \,||\, R_i'$$

But $\quad R_i' = Z_b \quad$ [since configuration is CC]

$$R_{Th_i} = 1\ \text{k}\Omega \,||\, 120\ \text{k}\Omega \,||\, 33\ \text{k}\Omega \,||\, 146.6\ \text{k}\Omega$$
$$= 956.5\ \Omega$$

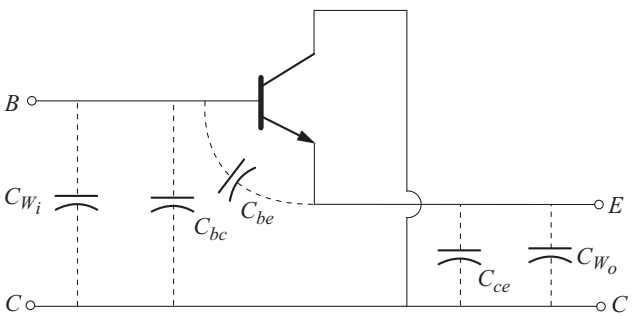


Fig.A

From Fig(A)

$$C_i = C_{Wi} + C_{bc} + C_{be}$$
$$= 7\ \text{pF} + 15\ \text{pF} + 25\ \text{pF}$$
$$= 47\ \text{pF}$$

$$f_{H_i} = \frac{1}{2\pi[956.5\ \Omega]\,[47\ \text{pF}]}$$

$$= 3.54\ \text{MHz}$$

$$f_{H_o} = \frac{1}{2\pi R_{Th_o} C_o}$$

$$R_{Th_o} = R_E \| R_L \| r_e$$
$$= 2\ \text{k}\Omega \| 5\ \text{k}\Omega \| 23.21\Omega$$
$$= 22.83\ \Omega$$

From Fig A

$$C_o = C_{Wo} + C_{ce}$$
$$= 10\ \text{pF} + 12\ \text{pF} = 22\ \text{pF}$$
$$f_{H_o} = \frac{1}{2\pi(22.83\ \Omega)(22\ \text{pF})} = 316.87\ \text{MHz}$$

(b)
$$f_\beta = \frac{1}{2\pi\beta_{\text{mid}}\, r_e\, [C_{be} + C_{bc}]}$$
$$= \frac{1}{2\pi(100)(23.21\ \Omega)[25\ \text{pF} + 15\,\text{pF}]}$$
$$= 1.714\ \text{MHz}$$
$$f_T = \beta_{\text{mid}}\, f_\beta = (\ 100\ )\ (\ 1.714\ \text{MHz}\ ) = 171.4\ \text{MHz}$$

Example 4.16

For the circuit of Example 4.10 with the same parameter values calculate the following

(a) f_{H_i} and f_{H_o}

(b) f_β and f_T

Take $C_{Wi} = 10$ pF $C_{Wo} = 10$ pF $C_{bc} = 18$ pF $C_{be} = 24$ pF $C_{ce} = 12$ pF.

Solution

$r_e = 9.09\ \Omega$ (From example 4.10)

(a)
$$f_{H_i} = \frac{1}{2\,\pi\, R_{Th_i}\, C_i}$$
$$R_{Th_i} = R_S \| R_E \| R_i'$$
$R_i' = r_e$ [since configuration is CB]
$$R_{Th_i} = 120\ \Omega \| 1.5\ \text{k}\Omega \| 9.09\ \Omega = 8.4\ \Omega$$

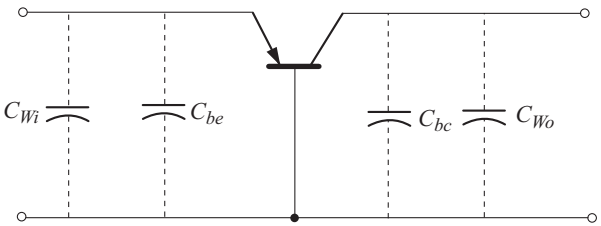


Fig. A

From Fig. A

$$C_i = C_{W_i} + C_{be} = 10 \text{ pF} + 24 \text{ pF} = 34 \text{ pF}$$

$$f_{H_i} = \frac{1}{2\pi(8.4\ \Omega)(34 \text{ pF})} = 557.26 \text{ MHz}$$

$$f_{H_o} = \frac{1}{2\,\pi\, R_{Th_o} C_o}$$

$$R_{Th_o} = r_o \,||\, R_C \,||\, R_L$$
$$= \infty \,||\, 3\ \text{k}\Omega \,||\, 4.7\ \text{k}\Omega$$
$$= 1.83\ \text{k}\Omega$$

$$C_o = C_{bc} + C_{W_o} \qquad [\text{ see Fig A }]$$
$$= 18 \text{ pF} + 10 \text{ pF} = 28 \text{ pF}$$

$$f_{H_o} = \frac{1}{2\pi\ (1.83\ \text{k}\Omega)(28 \text{ pF})} = 3.1 \text{ MHz}$$

(b)

$$f_\beta = \frac{1}{2\pi\,\beta_{\text{mid}}\, r_e [C_{be} + C_{bc}]}$$

$$= \frac{1}{2\pi\ [75]\,[9.09\ \Omega]\,[24 \text{ pF} + 18 \text{ pF}]}$$

$$= 5.55 \text{ MHz}$$

$$f_T = \beta_{\text{mid}}\, f_\beta = (75)\,(5.55 \text{ MHz})$$
$$= 416.25 \text{ MHz}$$

Exercise Problems

4.1 The following data is available for an amplifier

$P_i = 100$ W $\quad P_o = 50$ W $\quad V_i = 100$ V $\quad R_o = 20\ \Omega$

Calculate (a) Power gain in *dB* (b) Voltage gain in *dB*.

Hint: $A_{P\,(dB)} = 10 \log_{10} [P_o / P_i]$ $\quad A_{V\,(dB)} = 20 \log_{10} [V_o / V_i]$

$$P_o = \frac{V_o^2}{R_L} = \frac{V_o^2}{R_o} \qquad P_i = \frac{V_i^2}{R_i}$$

4.2 Two voltage measurements made across the same resistance are $V_1 = 20$ V and $V_2 = 100$ V. Calculate

(a) Power gain in dB of the second reading over the first reading

(b) Voltage gain

Hint: $R_i = R_o$

4.3 If the applied ac power to a system is 5 μW at 100 mV and the output power is 48 W, calculate

(a) Power gain in dB
(b) Voltage gain in dB if $R_L = 40\ k\Omega$
(c) Input impedance
(d) Output impedance

4.4 An amplifier is required to deliver 50 W to a 16Ω loud speaker. Calculate

(a) The input power required if the power gain is 20 dB
(b) The input Voltage required if the amplifier voltage gain is 40 dB.

4.5 The total decibel Voltage gain of a three stage system is 120 dB. The second stage has twice the decibel voltage gain of the first and the third has 2.7 times the decibel gain of the first. Calculate

(a) The decibel voltage gain of each stage
(b) The voltage gain of each stage and the overall voltage gain

Hint: $A_V = A_{V_1} \cdot A_{V_2} \cdot A_{V_2}$

$A_{V\,(dB)} = A_{V_1\,(dB)} + A_{V_2\,(dB)} + A_{V_3\,(dB)}$

Chapter 5

General Amplifiers

When the amplification from a single stage amplifier is not sufficient for a particular purpose, or when the input or output impedance is not of suitable magnitude for the intended application, two or more amplifier stages are connected in cascade. The cascade of CE and CB stages is called cascode amplifier. This chapter discusses cascaded stages, cascode amplifier, current mirror and current sources. Analysis of transistor configurations using the approximate and the complete hybrid model has also been considered.

5.1 CASCADED SYSTEMS

When the amplification from a single stage amplifier is not sufficient for a particular purpose or when the input or output impedance is not of suitable magnitude for the intended application, two or more amplifier stages may be connected in cascade: i.e., the output of a given stage is connected to the input of the next stage. Such an arrangement is called multistage amplifier. Figure 5.1 shows three amplifier stages connected in cascade. The two port system approach is very much useful in the analysis of cascaded systems.

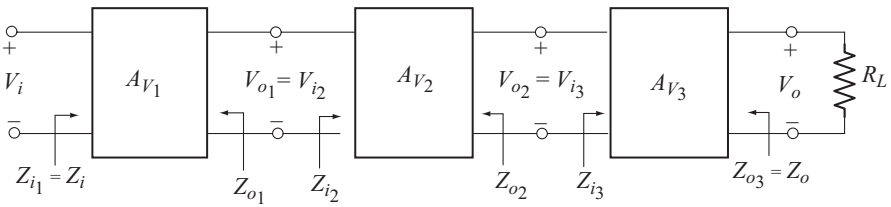


Fig. 5.1 *Cascaded amplifiers*

It is important to note that, the input impedance of a given stage loads the output of the preceeding stage. Thus the voltage gains A_{V_1}, A_{V_2} and A_{V_3} are the loaded voltage gains whose values can be calculated using the corresponding no load gains. Also for the cascaded system, the input impedance is that of the first stage and the output impedance is that of the last stage.

i.e., $Z_i = Z_{i_1}$ and $Z_o = Z_{o_3}$

Since the output of one stage is connected as input to the next stage,

$$V_{i_2} = V_{o_1} \text{ and } V_{i_3} = V_{o_2}$$

The total or the overall voltage gain of the cascaded system can be obtained as follows:

$$A_{V_T} = \frac{V_o}{V_i}$$

$$A_{V_T} = \frac{V_o}{V_{i_3}} \cdot \frac{V_{i_3}}{V_{i_2}} \cdot \frac{V_{i_2}}{V_i}$$

Using $V_{i_3} = V_{o_2}$ and $V_{i_2} = V_{o_1}$ we have

$$A_{V_T} = \frac{V_o}{V_{i_3}} \cdot \frac{V_{o_2}}{V_{i_2}} \cdot \frac{V_{o_1}}{V_i}$$

$$= A_{V_3} \cdot A_{V_2} \cdot A_{V_1}$$

or $$A_{V_T} = A_{V_1} \cdot A_{V_2} \cdot A_{V_3} \tag{5.1}$$

where $$A_{V_1} = \frac{V_{o_1}}{V_{i_1}} = \text{Loaded voltage gain of stage 1}$$

$$A_{V_2} = \frac{V_{o_2}}{V_{i_2}} = \text{Loaded voltage gain of stage 2}$$

$$A_{V_3} = \frac{V_{o_3}}{V_{i_3}} = \text{Loaded voltage gain of stage 3}$$

For *n* cascaded amplifier stages, the total voltage gain is given by

$$A_{V_T} = A_{V_1} \cdot A_{V_2} \cdot A_{V_3} \cdots A_{V_n} \tag{5.2}$$

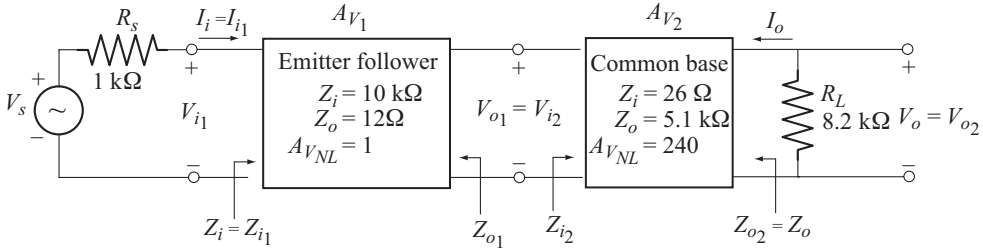
The total current gain is given by

$$A_{I_T} = -A_{V_T} \frac{Z_{i_1}}{R_L} \tag{5.3}$$

Example 5.1

For the cascaded arrangement shown below, determine

(a) The loaded gain for each stage.
(b) The total gain for the system, A_V and A_{V_S}.
(c) The total current gain for the system.
(d) The total gain for the system if the emitter-follower configuration were removed.
(e) The phase relation ship between V_o and V_i.



Solution

(a) For the emitter-follower, the load is Z_{i_2},

$$A_{V_1} = \frac{V_{0_1}}{V_{i_1}} = \frac{Z_{i_2}}{Z_{i_2} + Z_{o_1}} A_{V_{NL}} = \frac{26\Omega}{26\Omega + 12\Omega} = 0.684$$

For the common-base configuration,

$$A_{V_2} = \frac{V_o}{V_{i_2}} = \frac{R_L}{R_L + Z_{o_2}} A_{V_{NL}}$$

$$= \frac{8.2\text{k}\Omega}{8.2\text{k}\Omega + 5.1\text{k}\Omega} (240) = 147.97$$

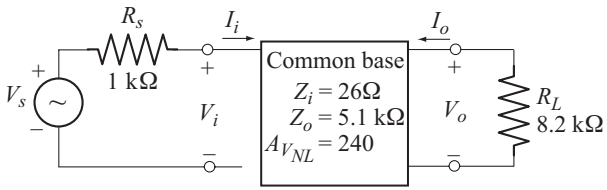
(b) The total voltage gain is

$$A_{V_T} = A_{V_1} A_{V_2} = (0.684)\ (147.97) = 101.20$$

$$A_{V_S} = \frac{Z_{i_1}}{Z_{i_1} + R_S} A_{V_T} = \frac{10\text{k}\Omega}{10\text{k}\Omega + 1\text{k}\Omega} (101.20) = 92$$

(c)
$$A_{I_T} = -A_{V_T} \frac{Z_{i_1}}{R_L} = -(101.20)\ \frac{10\text{k}\Omega}{8.2\text{k}\Omega} = -123.41$$

(d) With out emitter-follower, the arrangement is as shown below.



$$A_V = \frac{V_o}{V_i} = \frac{R_L}{Z_o + R_L} A_{V_{NL}}$$

$$= \frac{8.2\text{k}\Omega}{5.1\text{k}\Omega + 8.2\text{k}\Omega} (240)$$

$$= 147.97$$

$$A_{V_S} = \frac{V_o}{V_s} = \frac{V_o}{V_i}\frac{V_i}{V_s}$$

$$= A_V \frac{Z_i}{R_s + Z_i} = (147.97)\ \frac{26\Omega}{1\text{k}\Omega + 26\Omega} = 3.75$$

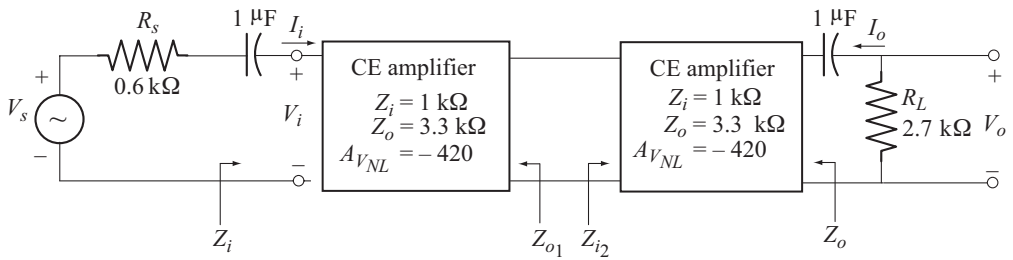
(e) Both emitter-follower and common-base stage introduces zero degree phase shift. Hence V_o and V_i are in phase.

Note : When the emitter-follower is removed, the voltage gain falls from 92 to 3.75. This is due to the very low input impedance of CB stage. Emitter-follower matches the low input impedance of CB stage with the high source resistance R_S.

Example 5.2

For the cascaded arrangement shown below calculate

(a) The loaded voltage gain of each stage
(b) The total gain of the system, A_V and A_{V_S}
(c) The loaded current gain of each stage
(d) The total current gain of the system
(e) How Z_i is affected by the second stage and R_L
(f) How Z_o is affected by the first stage and R_s
(g) The phase relation ship between V_o and V_i



Solution

(a) The load on first stage is Z_{i_2}

$$A_{V_1} = \frac{Z_{i_2}}{Z_{o_1} + Z_{i_2}}\ A_{V_{NL}} = \frac{1\text{k}\Omega}{3.3\text{k}\Omega + 1\text{k}\Omega}\ (-420) = -97.67$$

$$A_{V_2} = \frac{R_L}{Z_o + R_L}\ A_{V_{NL}} = \frac{2.7\text{k}\Omega}{3.3\text{k}\Omega + 2.7\text{k}\Omega}\ (-420) = -189$$

(b) The total voltage gain is

$$A_{V_T} = A_{V_1} A_{V_2} = (-97.67)\ (-189) = 18.45 \times 10^3$$

$$A_{V_s} = \frac{Z_i}{R_s + Z_i}\ A_{V_T}$$

$$= \frac{1\text{k}\Omega}{0.6\text{k}\Omega + 1\text{k}\Omega}\,(18.45 \times 10^3) = 11.53 \times 10^3$$

(c) $$A_{I_1} = -A_{V_1}\frac{Z_i}{Z_{i_2}} \quad [\text{Since load on first stage is } Z_{i_2}]$$

$$= -(-97.67)\,\frac{1\text{k}\Omega}{1\text{k}\Omega} = 97.67$$

$$A_{I_2} = -A_{V_2}\,\frac{Z_{i_2}}{R_L} = -(-189)\,\frac{1\text{k}\Omega}{2.7\text{k}\Omega} = 70$$

(d) Total current gain is

$$A_{I_T} = A_{I_1} \cdot A_{I_2} = (97.67)\,(70) = 6.84 \times 10^3$$

(e) Z_i is unaffected by the second stage and R_L

(f) Z_o is unaffected by the first stage and R_S

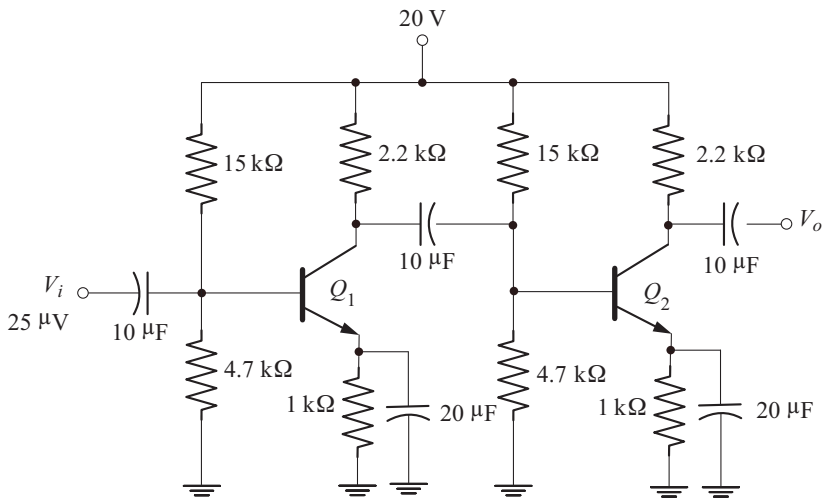
(g) Each CE stage introduces a phase shift of 180º. Hence the phase shift between V_o and V_i is 360° or 0º. i.e., V_o and V_i are in phase.

Example 5.3

For the BJT cascade amplifier shown below

(a) Calculate the dc bias voltages and collector current for each stage.
(b) Calculate the voltage gain of each stage, the overall voltage gain and the output voltage.
(c) Repeat part (b) with a 10 kΩ load applied to the second stage.
(d) Calculate the input impedance of the first stage and the output impedance of the second stage.

Take $\beta = 200$ for both transistors.



Solution

(a) Since R_1, R_2, R_E, R_C and β are same for both the transistors, the dc bias voltages and currents are identical in both the stages.

Check for $\beta R_E \geq 10\, R_2$

$$\beta R_E = (200)\,(1\ \text{k}\Omega) = 200\ \text{k}\Omega$$
$$10\, R_2 = (10)\,(4.7\ \text{k}\Omega) = 47\ \text{k}\Omega$$

Since $\beta R_E > 10\, R_2$, We can use approximate analysis.

$$V_B = \frac{V_{CC}\, R_2}{R_1 + R_2} = \frac{(20\,\text{V})(4.7\,\text{k}\Omega)}{15\,\text{k}\Omega + 4.7\,\text{k}\Omega} = 4.77\ \text{V}$$
$$V_E = V_B - V_{BE} = 4.77\ \text{V} - 0.7\ \text{V} = 4.07\ \text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{4.07\,\text{V}}{1\,\text{K}\Omega} = 4.07\ \text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{4.07\,\text{mA}} = 6.39\ \Omega$$
$$I_B = \frac{I_E}{1+\beta} = \frac{4.07\,\text{mA}}{201} = 20.25\ \mu\text{A}$$
$$I_C = \beta I_B = (200)\,(20.25\ \mu\text{A}) = 4.05\ \text{mA}$$
$$V_C = V_{CC} - I_C\, R_C$$
$$= 20\ \text{V} - (4.05\ \text{mA})\,(2.2\ \text{k}\Omega) = 11.09\ \text{V}$$
$$V_{CE} = V_C - V_E = 11.09\ \text{V} - 4.07\ \text{V} = 7.02\ \text{V}$$

(b) Load on the first stage is

$$R_{L_1} = R_C \,\|\, Z_{i_2}$$
$$Z_{i_2} = R_1 \,\|\, R_2 \,\|\, \beta\, r_e$$
$$= 15\ \text{k}\Omega \,\|\, 4.7\ \text{k}\Omega \,\|\, (200)\,(6.39\ \Omega) = 0.942\ \text{k}\Omega$$
$$R_{L_1} = 2.2\ \text{k}\Omega \,\|\, 0.942\ \text{k}\Omega = 0.659\ \text{k}\Omega$$
$$A_{V_1} = -\frac{R_{L_1}}{r_e} = -\frac{0.659\,\text{k}\Omega}{6.39\,\Omega} = -103.13$$

Since second stage is unloaded, its voltage gain is

$$A_{V_{2\,(NL)}} = -\frac{R_C}{r_e} = -\frac{2.2\,\text{k}\Omega}{6.39\,\Omega} = -344.28$$

Overall Voltage gain is

$$A_{V_{T\,(NL)}} = A_{V_1}\, A_{V_{2\,(NL)}} = (-103.13)\,(-344.28) = 35.5 \times 10^3$$
$$V_o = A_{V_{T\,(NL)}}\, V_i = (35.5 \times 10^3)\,(25\ \mu\text{V}) = 887.5\ \text{mV}$$

(c) The overall voltage gain with $R_L = 10\ \text{k}\Omega$ is

$$A_{V_T} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o} A_{V_{T(NL)}}$$

But $$Z_o = R_C = 2.2\ \text{k}\Omega$$

$$A_{V_T} = \frac{10\,\text{k}\Omega}{10\,\text{k}\Omega + 2.2\,\text{k}\Omega} (35.5 \times 10^3) = 29.09 \times 10^3$$

$$V_o = A_{V_T} V_i = (29.09 \times 10^3)\ (25\ \mu\text{V}) = 727.25\ \text{mV}$$

(d) Input impedance of the first stage is

$$Z_{i_1} = Z_i = R_1 \parallel R_2 \parallel \beta r_e = 0.942\ \text{k}\Omega \qquad \text{(same as } Z_{i_2}\text{)}$$

Output impedance of second stage is

$$Z_{o_2} = Z_o = R_C = 2.2\ \text{k}\Omega$$

Note: If the two stages are not identical then dc analysis has to be carried out separately and their r_e values are different.

◆ 5.2 CASCODE CONNECTION

In cascode connection the output of CE stage drives the input of CB stage as shown in Fig. 5.2. The cascode connection has low input capacitance, which is an advantage at high frequencies such as VHF and UHF. At these higher frequencies, the input capacitance becomes a limiting factor on the voltage gain. With a cascode amplifier, the low input capacitance allows the circuit to amplify higher frequencies than are possible with only a CE amplifier.

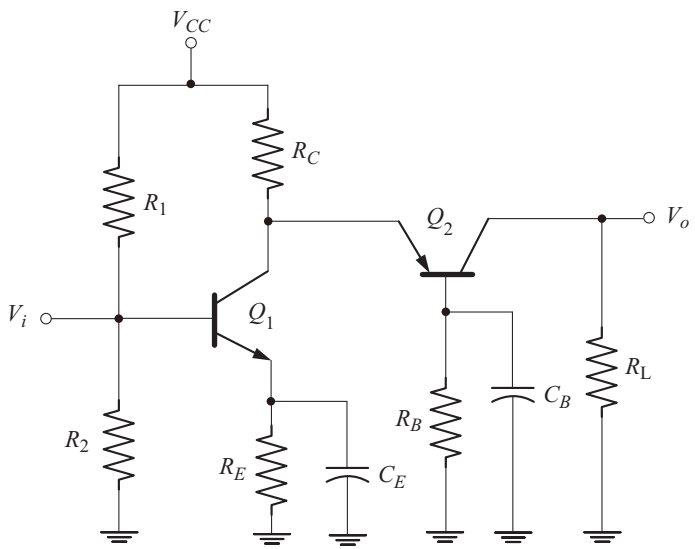


Fig. 5.2 Cascode configuration

Cascode connection has high input impedance (provided by CE) and high output impedance (provided by CB). The CB stage provides an excellent high frequency response.

Due to direct coupling between CE and CB stages, the dc bias current for Q_2 is obtained from the collector node of Q_2. R_B is used to limit the bias current of Q_2. For ac operation, R_B is shorted out by C_B. Thus the base of Q_2 will be at ground potential for ac operation, which is essential for CB configuration.

The low input impedance of CB stage loads the output of CE stage. Thus the voltage gain of CE stage is very low. A large voltage gain is provided by the CB stage, thus the overall voltage gain is high with a good input impedance level.

An alternate cascode configuration is shown in Fig .5.3. In this circuit Q_1 is in CE configuration and Q_2 in CB configuration. For ac operation, C_2 shorts the base of Q_2 to ground. Note that both Q_1 and Q_2 are npn transistors.

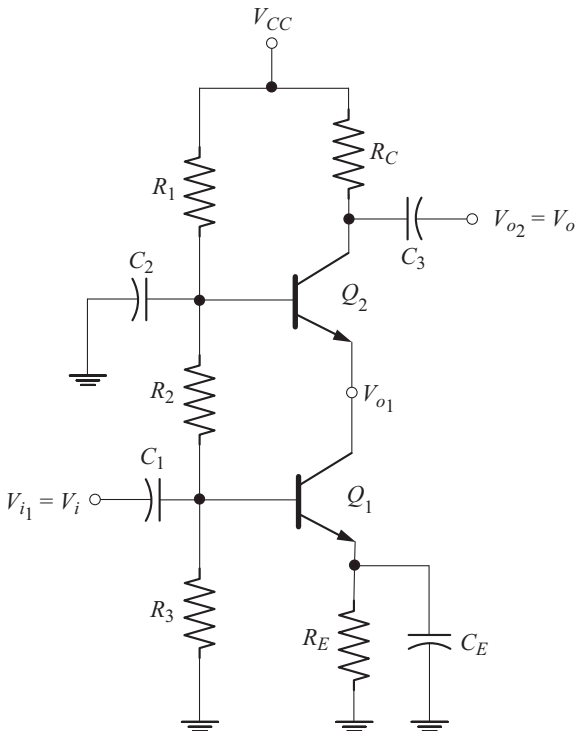


Fig. 5.3 Alternate cascode connection

Example 5.4

For the cascode connection of Fig. 5.3 the followings data are available:

$R_1 = 6.8\ \text{k}\Omega$ $R_2 = 5.6\ \text{k}\Omega$ $R_3 = 4.7\ \text{k}\Omega$

$R_C = 1.8\ \text{k}\Omega$ $R_E = 1.1\ \text{k}\Omega$ $V_{CC} = 18\ \text{V}$

$\beta_1 = \beta_2 = 200$ $V_i = 10\ \text{mV}$

(a) Calculate the dc bias voltages V_{B_1}, V_{B_2}, V_{C_2}

(b) Calculate the no load voltage gain and the output voltage $V_{o_2} = V_o$

(c) Calculate the voltage gain with a load of 10 kΩ connected to the second stage and the output voltage V_o

(d) Input and output impedances

Solution

(a) DC voltage at the base of Q_1 is

$$V_{B_1} = \frac{R_3}{R_1 + R_2 + R_3} V_{CC}$$

$$= \frac{4.7\,\text{k}\Omega}{6.8\,\text{k}\Omega + 5.6\,\text{k}\Omega + 4.7\,\text{k}\Omega} (18\text{ V}) = 4.9\text{ V}$$

$$V_{E_1} = V_{B_1} - V_{BE} = 4.9\text{ V} - 0.7\text{ V} = 4.2\text{ V}$$

$$I_{E_1} \approx I_{C_1} = \frac{V_{E_1}}{1.1\,\text{k}\Omega} = \frac{4.2\,\text{V}}{1.1\,\text{k}\Omega} = 3.82\text{ mA}$$

Note that the emitter current of Q_2 is also the collector current of Q_1

$$\therefore \quad I_{E_2} = I_{C_1} = 3.82\text{ mA}$$

Since $I_{E_1} = I_{E_2}$, the dynamic resistance r_e is the same for both the transistor.

$$r_e = \frac{26\,\text{mV}}{3.82\,\text{mA}} = 6.8\ \Omega$$

Voltage on the base of Q_2 is

$$V_{B_2} = \frac{R_3 + R_2}{R_1 + R_2 + R_3} V_{CC}$$

$$= \frac{4.7\,\text{k}\Omega + 5.6\,\text{k}\Omega}{6.8\,\text{k}\Omega + 5.6\,\text{k}\Omega + 4.7\,\text{k}\Omega} (18\text{ V}) = 10.\ 84\text{ V}$$

$$I_{C_2} = \frac{V_{CC} - V_{C_2}}{R_C}$$

$$\Rightarrow \quad V_{C_2} = V_{CC} - I_{C_2} R_C = 18\text{ V} - (3.82\text{ mA})\,(1.8\text{ k}\Omega) = 11.124\text{ V}$$

(b) The load on the transistor Q_1 is the input impedance of the Q_2. Since Q_2 is in the CB configuration, $R_C = r_e$ for Q_1.

$$A_{V_1} = -\frac{R_C}{r_e} = -\frac{r_e}{r_e} = -1$$

For the second stage (CB)

$$A_{V_2} = \frac{R_C}{r_e} = \frac{1.8\,\text{k}\Omega}{6.8\,\Omega} = 264.7$$

Overall no load voltage gain is

$$A_{V_{T(NL)}} = A_{V_1} \cdot A_{V_2} = (-1)\,(264.7) = -264.7$$
$$V_o = A_{V_{T(NL)}}\, V_i = (-264.7)\,(10\text{ mV}) = -2.647\text{ V}$$

Note that CE stage has a small voltage gain of unity and CB stage providing a larger voltage gain of 264.7.

(c) With $R_L = 10\text{ k}\Omega$

$$A_{V_1} = -1 \qquad \text{(same as before)}$$
$$A_{V_2} = \frac{R_C \| R_L}{r_e} = \frac{(1.8\text{k}\Omega) \| (10\text{k}\Omega)}{6.8\Omega} = 224.33$$
$$A_{V_T} = A_{V_1} \cdot A_{V_2}$$
$$= -224.33$$
$$V_o = A_{V_T}\, V_i = (-224.33)\,(10\text{ mV}) = -2.243\text{ V}$$

(d) The input impedance is given by the input impedance of CE stage.

$$Z_i = \beta\, r_e = (200)\,(6.8\ \Omega) = 1.36\text{ k}\Omega$$

The output impedance is given by that of CB stage

$$Z_o = R_C = 1.8\text{ k}\ \Omega$$

◆ 5.3 DARLINGTON CONNECTION

A Darlington connection is a very popular connection of two transistors for operation as one super beta transistor. The composite transistor acts as a single unit with a current gain equal to the product of the current gains of individual transistors. Figure 5.4 shows the Darlington connection which is also called the Darlington pair.

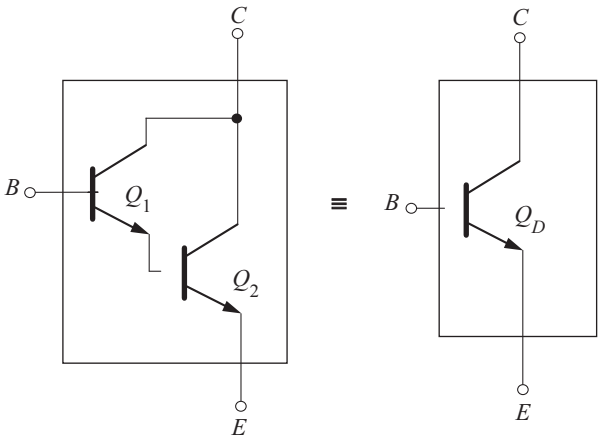


Fig. 5.4 Darlington connection

If β_1 and β_2 are the current gains of Q_1 and Q_2 respectively, the current gain of Darlington connection is

$$\beta_D = \beta_1 \beta_2 \tag{5.4}$$

If the two transistors are matched so that $\beta_1 = \beta_2 = \beta$, the Darlington connection provides a current gain of

$$\beta_D = \beta^2 \tag{5.5}$$

For instance if $\beta_1 = \beta_2 = 200$, the overall current gain is

$$\beta_D = (200)^2 = 40{,}000$$

A Darlington transistor connection acts as a single transistor with a large current gain, typically a few thousand.

Darlington connection is available as a single package containing two BJTs internally connected as a Darlington transistor. The device provides three terminals, base, emitter and collector for external connection. For instance the 2N 6725 is a Darlington transistor with a current gain of 25,000 and a collector current of 200 mA. As another example, the TIP 102 is a power Darlington transistor with a current gain of 1000 at a collector current of 3A.

◆ 5.4 DC BIAS OF DARLINGTON CIRCUIT

A Darlington circuit with biasing arrangement is shown in Fig. 5.5. The current gain of the Darlington transistor is β_D which is very high.

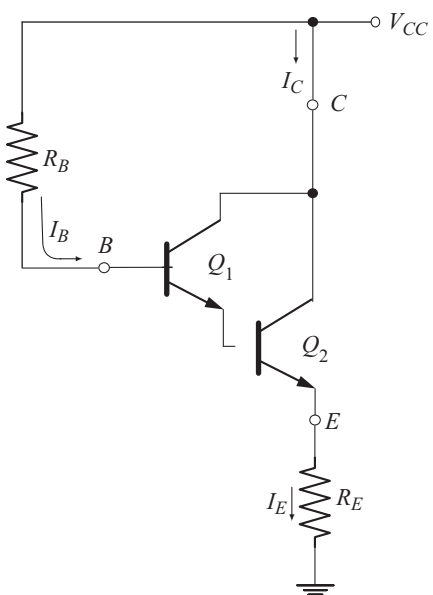


Fig. 5.5 DC bias of Darlington circuit

Applying KVL to the base-emitter circuit we have

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \tag{5.6}$$

$$I_E = (1+\beta_D) I_B \tag{5.7}$$

Using Equation (5.7) in (5.6) and solving for I_B we have

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta_D) R_E} \tag{5.8}$$

It should be noted that, V_{BE} is the drop for two base-emitter junctions which is typically in the range 1.4 V to 1.8 V.

$$I_E = (1+\beta_D) I_B \approx \beta_D I_B \quad [\text{Since } \beta_D \text{ is very high.}] \tag{5.9}$$

The dc voltages are

$$V_E = I_E R_E \tag{5.10}$$

$$V_B = V_{BE} + V_E \tag{5.11}$$

5.5 DARLINGTON EMITTER-FOLLOWER

Figure 5.6 shows the circuit of Darlington emitter-follower. The ac input signal V_i is coupled to the base of the Darlington transistor through the input coupling capacitor C_1. The ac output voltage V_o is taken at the emitter through the output coupling capacitor C_2.

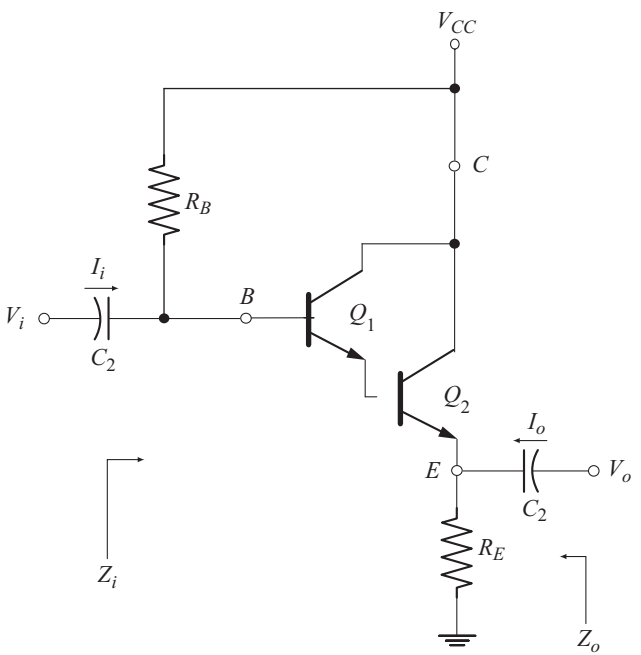


Fig. 5.6 Darlington emitter-follower

The ac equivalent circuit of Darlington emitter-follower is shown in Fig. 5.7. The Darlington transistor is replaced by

(a) an input resistance r_i between base and emitter terminals
(b) a controlled current source $\beta_D I_b$ between the collector and the emitter terminals.

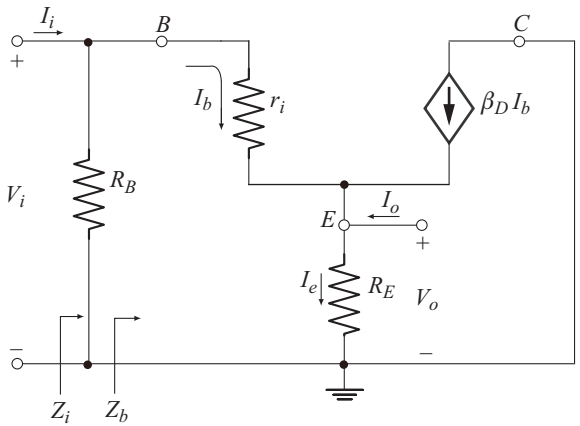


Fig. 5.7 AC equivalent circuit of Darlington emitter follower

AC Input Impedance (Z_i)

Applying KVL to the input circuit of Fig. 5.7 we have

$$V_i = I_b r_i + I_e R_E$$

Using $I_e = (1 + \beta_D) I_b$, we have

$$V_i = I_b r_i + (1 + \beta_D) R_E I_b$$

$$Z_b = \frac{V_i}{I_b} = r_i + (1 + \beta_D) R_E \tag{5.12}$$

Since β_D is very high, $$Z_b \approx \beta_D R_E \tag{5.13}$$

$$Z_i = \frac{V_i}{I_i} = R_B \parallel Z_b \tag{5.14}$$

AC Current Gain (A_I)

$$A_I = \frac{I_o}{I_i} = \frac{I_o}{I_b} \cdot \frac{I_b}{I_i}$$

But $$I_o = I_e$$

$$\therefore \quad A_I = \frac{I_e}{I_b} \cdot \frac{I_b}{I_i} \tag{5.15}$$

$$I_e = (1 + \beta_D) I_b \approx \beta_D I_b$$

$$\Rightarrow \qquad \frac{I_e}{I_b} = \beta_D \tag{5.16}$$

Applying KCL to the input circuit we have

$$I_i = \frac{V_i}{R_B} + I_b$$

Using $V_i = I_b Z_b$ we get

$$I_i = I_b \left[\frac{Z_b}{R_B} + 1\right] = I_b \left[\frac{Z_b + R_B}{R_B}\right]$$

$$\Rightarrow \qquad \frac{I_b}{I_i} = \frac{R_B}{Z_b + R_B} \tag{5.17}$$

Using Equations (5.16) and (5.17) in Equation (5.15) we have

$$A_I = \beta_D \frac{R_B}{Z_b + R_B} \tag{5.18}$$

Substituting for Z_b from Equation (5.13), we get

$$A_I = \frac{\beta_D R_B}{R_B + \beta_D R_E} \tag{5.19}$$

AC Voltage Gain (A_V)

Refer the circuit of Fig. 5.7

$$V_o = I_e R_E$$
$$= [1 + \beta_D] I_b R_E$$

From Equation (5.12) we have

$$V_i = I_b [r_i + (1 + \beta_D) R_E]$$

Now

$$A_V = \frac{V_o}{V_i} = \frac{I_b [1 + \beta_D] R_E}{I_b [r_i + (1 + \beta_D) R_E]}$$

$$A_V = \frac{[1 + \beta_D] R_E}{r_i + [1 + \beta_D] R_E} \tag{5.20}$$

Since $(1 + \beta_D) R_E \gg r_i$

$$A_V \approx \frac{(1 + \beta_D) R_E}{[1 + \beta_D] R_E} = 1 \tag{5.21}$$

AC Output Impedance (Z_o)

To determine the ac output impedance we apply the following steps to the circuit of Fig. 5.7

(a) V_i is reduled to zero i.e. it is replaced by short circuit equivalent

(b) a voltage source V is connected between the output terminals.

The resulting circuit is shown in Fig. 5.8. Now the output impedance is given by

$$Z_o = \frac{V}{I} \tag{5.22}$$

where I is the current driven by the voltage source into the output terminals.

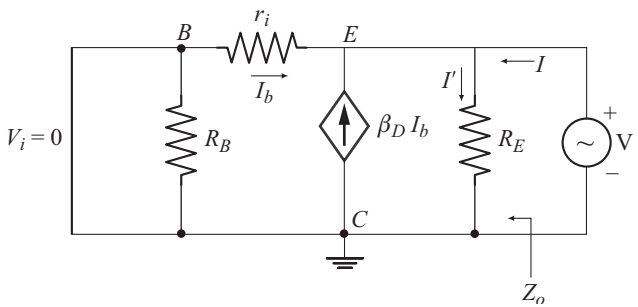


Fig. 5.8 Circuit to find Z_o

The circuit of Fig. 5.8 is redrawn in Fig. 5.9.

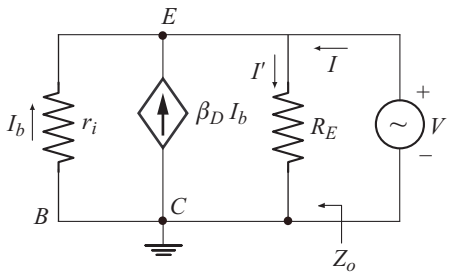


Fig. 5.9 Simplified circuit to find Z_o

Applying KCL at the emitter node we have

$$I_b + \beta_D I_b - I' + I = 0 \tag{5.23}$$

But $$I_b = \frac{-V}{r_i} \quad \text{and} \quad I' = \frac{V}{R_E}$$

Using these relations in Equation (5.23) we get

$$-\frac{V}{r_i} + \beta_D \left(-\frac{V}{r_i}\right) - \frac{V}{R_E} + I = 0$$

$$\left[\frac{1}{r_i}+\frac{1}{R_E}+\frac{\beta_D}{r_i}\right] V = I$$

$$Z_o = \frac{V}{I} = \frac{1}{\frac{1}{r_i}+\frac{1}{R_E}+\frac{\beta_D}{r_i}}$$

$$Z_o = \frac{1}{\frac{1}{r_i}+\frac{1}{R_E}+\frac{1}{(r_i/\beta_D)}} \tag{5.24}$$

Z_o can be interpreted as the parallel combination of r_i, R_E and $\frac{r_i}{\beta_D}$

$$\therefore \quad Z_o = r_i \| R_E \| \frac{r_i}{\beta_D} \tag{5.25}$$

Since $\frac{r_i}{\beta_D}$ is very much smaller than r_i and R_E we have

$$Z_o \approx \frac{r_i}{\beta_D} \tag{5.26}$$

5.5.1 Important Characteristics of Darlington Emitter-follower

The important characteristics of Darlington emitter-follower are:

- Very high current gain.
- Very high input impedance.
- Very low output impedance.
- Approximately unity voltage gain.
- Input and output voltages are in phase.

5.5.2 Applications of Darlington Emitter-follower

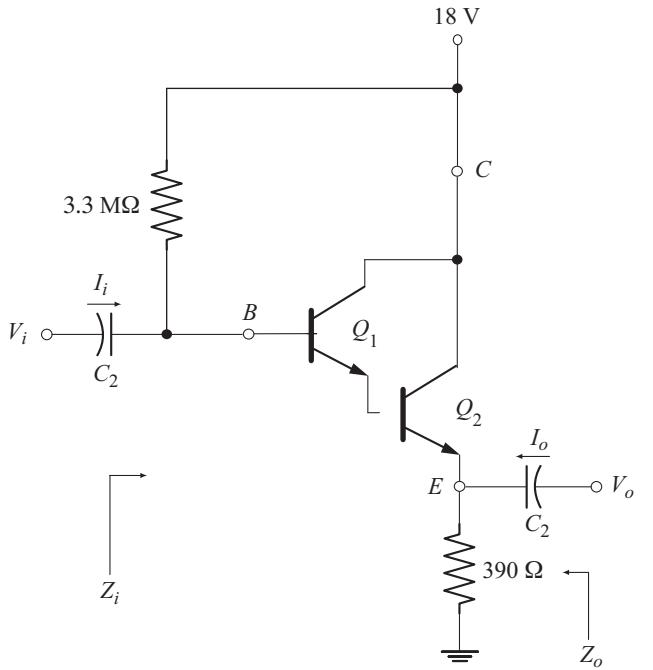
Darlington emitter-follower is a very popular configuration due to the attractive features listed above. Its important applications are:

- Buffer to connect a voltage source of high impedance to a load of low impedance.
- High current driver.
- Current amplifier.

Example 5.5

For the Darlington emitter-follower shown below:

(a) Calculate the dc bias voltages V_B, V_E, V_C and currents I_B and I_C.
(b) Calculate the input and output impedances.
(c) Determine the voltage and current gains.
(d) The ac output voltage for V_i = 120 mV.



Solution

(a)

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}$$

$$= \frac{18\,\text{V} - 1.6\,\text{V}}{3.3\,\text{M}\Omega + (8000)(390\Omega)} = 2.55\ \mu\text{A}$$

$$I_E = I_{E_2} \approx I_{C_2} = \beta_D I_B$$

$$= (8000)\ (2.55\ \mu\text{A}) = 20.4\ \text{mA}$$

$$V_E = I_E R_E = (20.4\ \text{mA})\ (390\ \Omega) = 7.96\ \text{V}$$

$$V_B = V_{BE} + V_E = 1.6\ \text{V} + 7.96\ \text{V} = 9.56\ \text{V}$$

Since the collector is directly tied to V_{CC}, the collector voltage equals the dc supply voltage V_{CC}.

$$\therefore \quad V_C = V_{CC} = 18\ \text{V}$$

(b)

$$Z_b = r_i + (1 + \beta_D)\, R_E$$

$$= 5\ \text{k}\Omega + (8001)\ (390\ \Omega) = 3.13\ \text{M}\Omega$$

$$Z_i = R_B \,\|\, Z_b = 3.3\ \text{M}\Omega \,\|\, 3.13\ \text{M}\Omega = 1.6\ \text{M}\Omega$$

$$Z_o = r_i \,\|\, R_E \,\|\, \frac{r_i}{\beta_D}$$

$$= 5\ \text{k}\Omega \parallel 390\ \Omega \parallel \frac{5\text{k}\Omega}{8000} = 0.625\ \Omega$$

(c)
$$A_V = \frac{R_E(1+\beta_D)}{r_i + R_E(1+\beta_D)}$$

$$= \frac{(390\Omega)(8001)}{5\text{k}\Omega + (390\Omega)(8001)} = 0.998$$

$$A_I = \frac{\beta_D R_B}{R_B + \beta_D R_E}$$

$$= \frac{(8000)(3.3\text{M}\Omega)}{3.3\text{M}\Omega + (8000)(390\Omega)} = 4112.15$$

(d)
$$V_o = A_V V_i = (0.998)\ (120\ \text{mV})$$

$$= 119.76\ \text{mV}$$

5.6 FEEDBACK PAIR

Figure 5.10 shows the feedback pair connection which is a two-transistor circuit that operates like the Darlington circuit. It is also called the complementary Darlington since it uses an npn and a pnp transistor. The collector current of Q_1 is the base current of Q_2.

If the pnp transistor has a current gain of β_1 and the npn output transistor has a current gain of β_2 the feedback pair acts like a single pnp transistor with a current gain of $\beta_1\beta_2$.

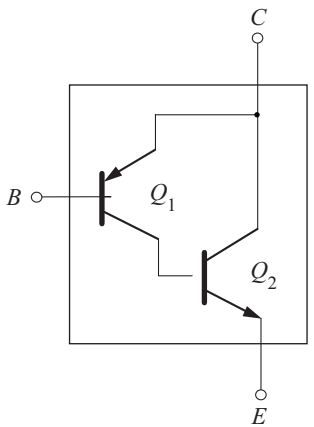


Fig. 5.10 Feedback pair connection

5.7 DC BIAS OF FEEDBACK PAIR

Figure 5.11 shows the biasing arrangement for feedback pair.

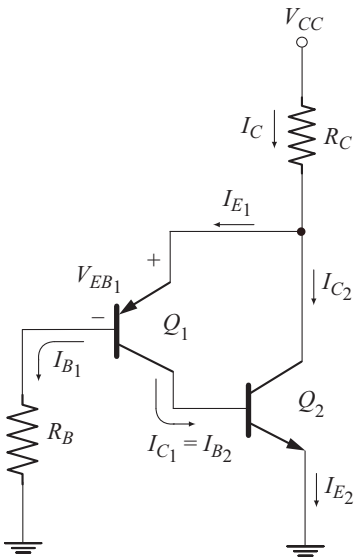


Fig . 5.11 DC biasing of feedback pair

Applying KVL to the base-emitter circuit of Q_1 we have

$$V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B = 0$$

Using $I_C = \beta_1 \beta_2 I_{B_1}$, we have

$$V_{CC} - \beta_1 \beta_2 I_{B_1} R_C - V_{EB_1} - I_{B_1} R_B = 0$$

$$I_{B_1} = \frac{V_{CC} - V_{EB_1}}{R_B + \beta_1 \beta_2 R_C} \tag{5.27}$$

The collector current of Q_1 is the base current of Q_2.

$$\therefore \quad I_{C_1} = I_{B_2} = \beta_1 I_{B_1} \tag{5.28}$$

The collector current of Q_2 is

$$I_{C_2} = \beta_2 I_{B_2} = \beta_1 \beta_2 I_{B_1} \approx I_{E_2} \tag{5.29}$$

The current thought R_C is

$$\begin{aligned} I_C &= I_{E_1} + I_{C_2} \\ &\approx I_{C_1} + I_{C_2} \\ &\approx I_{C_2} \end{aligned} \tag{5.30}$$

Since $I_{C_2} \gg I_{C_1}$

5.8 AC OPERATION OF FEEDBACK PAIR

The ac input signal V_i is coupled to the base of Q_1 through the input coupling capacitor C_1 as shown in Fig. 5.12. The ac output signal V_o is taken at the collector of Q_2 through the output coupling capacitor C_2.

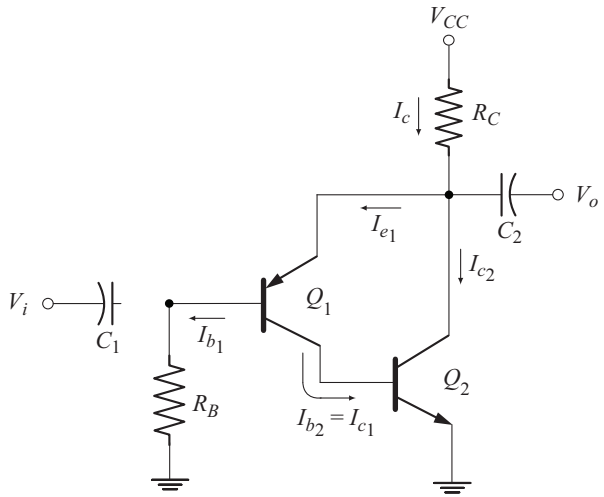


Fig. 5.12 AC operation of feedback pair

Figure 5.13 shows the ac equivalent circuit of feedback pair. For the ease of analysis the ac equivalent circuit is redrawn as shown in Fig. 5.14. It is important to note that, same ac model is used for both *pnp* and *npn* transistors. The actual current directions are investigated when ever necessary.

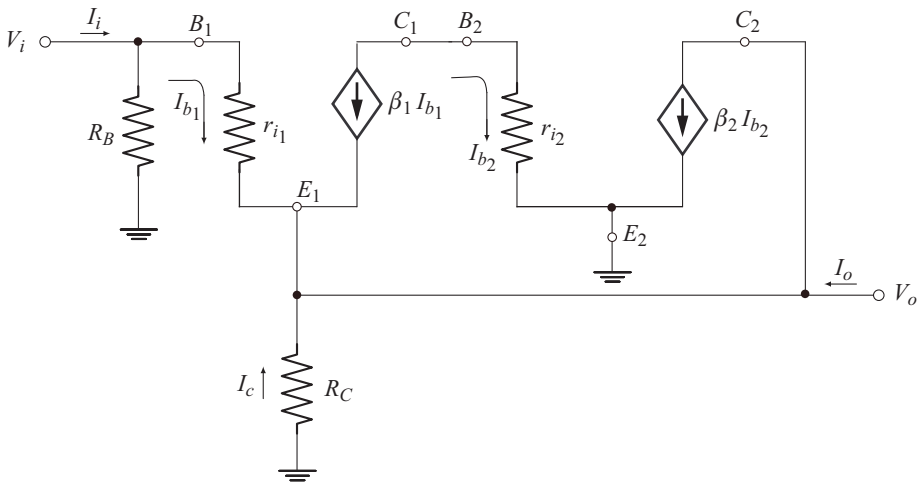


Fig. 5.13 AC equivalent circuit of feedback pair

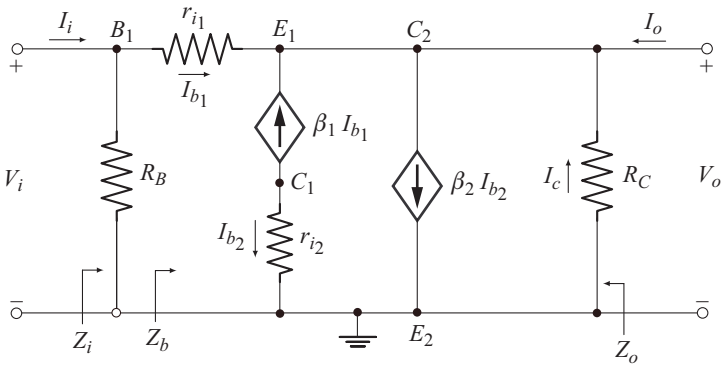


Fig. 5.14 AC equivalent circuit redrawn

AC Input Impedance (Z_i)

Writing KVL to the outer path of Fig. 5.14 we have

$$V_i - I_{b_1} r_{i_1} + I_c R_C = 0 \tag{5.31}$$

From the circuit of Fig. 5.12

$$I_c = I_{e_1} + I_{c_2}$$

$$I_{c_2} = \beta_2 I_{b_2} \quad \text{and} \quad I_{e_1} = (1 + \beta_1) I_{b_1} \approx \beta_1 I_{b_1}$$

Now $$I_c = \beta_2 I_{b_2} + \beta_1 I_{b_1}$$

But $$\beta_2 I_{b_2} \gg \beta_1 I_{b_1}$$

$\therefore$ $$I_c \approx \beta_2 I_{b_2}$$

But $$I_{b_2} = I_{c_1} = \beta_1 I_{b_1}$$

So that $$I_c = \beta_1 \beta_2 I_{b_1}$$

Since I_c and I_{b_1} are in opposite directions, it is appropriate to write

$$I_c = -\beta_1 \beta_2 I_{b_1} \tag{5.32}$$

Using this relation in Equation (5.31) we have

$$V_i = I_{b_1} r_{i_1} + I_{b_1} \beta_1 \beta_2 R_C$$

$\therefore$ $$Z_b = \frac{V_i}{I_{b_1}} = r_{i_1} + \beta_1 \beta_2 R_C \tag{5.33}$$

$$Z_i = R_B \parallel Z_b \tag{5.34}$$

AC Current Gain (A_I)

$$A_I = \frac{I_o}{I_i} = \frac{I_o}{I_{b_1}} \cdot \frac{I_{b_1}}{I_i} \tag{5.35}$$

But $$I_o = -I_c$$

$\therefore$ From Equation (5.32), $$\frac{I_o}{I_{b_1}} = \frac{-I_c}{I_{b_1}} = \beta_1 \beta_2 \quad (5.36)$$

Applying KCL at the node B_1 of Fig. 5.14 we have

$$I_i = I_{b_1} + \frac{V_i}{R_B}$$

Using $V_i = I_{b_1} Z_b$ we have

$$I_i = I_{b_1}\left[1 + \frac{Z_b}{R_B}\right]$$

$$\frac{I_i}{I_{b_i}} = \frac{R_B + Z_b}{R_B}$$

or $$\frac{I_{b_1}}{I_i} = \frac{R_B}{R_B + Z_b} \quad (5.37)$$

Using Equations (5.36) and (5.37) in Equation (5.35) we have

$$A_I = \frac{I_o}{I_i} = \beta_1 \beta_2 \frac{R_B}{R_B + Z_b} \quad (5.38)$$

AC *Voltage Gain* (A_V)

$$V_o = I_c R_c$$

Substituting for I_c from Equation (5.32) we have

$$V_o = \beta_1 \beta_2 I_{b_1} R_C \quad \text{[Taking only magnitude]} \quad (5.39).$$

From Equation (5.31) we have

$$V_i - I_{b_1} r_{i_1} - V_o = 0$$

$$\Rightarrow \quad I_{b_1} = \frac{V_i - V_o}{r_{i_1}}$$

Using this relation in Equation (5.39) we get

$$V_o = \beta_1 \beta_2 R_C \left[\frac{V_i - V_o}{r_{i_1}}\right]$$

$$V_o = \frac{\beta_1 \beta_2 R_C}{r_{i_1}} V_i - \frac{\beta_1 \beta_2 R_C}{r_{i_1}} V_o$$

$$V_o\left[1 + \frac{\beta_1 \beta_2 R_C}{r_{i_1}}\right] = V_i\left[\frac{\beta_1 \beta_2 R_C}{r_{i_1}}\right]$$

$$A_V = \frac{V_o}{V_i} = \left[\frac{\beta_1 \beta_2 R_C}{r_{i_1} + \beta_1 \beta_2 R_C}\right] \tag{5.40}$$

AC Output Impedance (Z_o)

The circuit to find Z_o is shown in Fig. 5.15, which is obtained by reducing V_i to zero and connecting an ac source of voltage V between the output terminals in the circuit of Fig. 5.14.

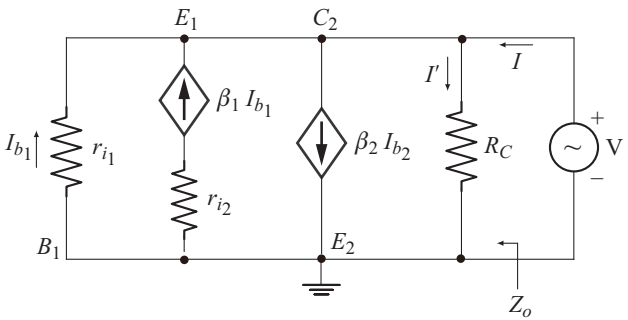


Fig. 5.15 Circuit to find Z_o

Summing all the currents at the node C_2, we have

$$I_{b_1} + \beta_1 I_{b_1} - \beta_2 I_{b_2} - I' + I = 0 \tag{5.41}$$

$$I_{b_1} = -\frac{V}{r_{i_1}} \quad \text{and} \quad I' = \frac{V}{R_C}$$

$$I_{b_2} = I_{c_1} = \beta_1 I_{b_1}$$

I_{b_1} is the base current of *pnp* transistor and I_{b_2} is that of *npn* transistor. Thus taking direction into consideration we have

$$I_{b_2} = -\beta_1 I_{b_1} = -\beta_1 \left[\frac{-V}{r_{i_1}}\right] = \frac{\beta_1 V}{r_{i_1}}$$

Using these relations in Equation (5.41) we have

$$\frac{-V}{r_{i_1}} - \beta_1 \frac{V}{r_{i_1}} - \beta_1 \beta_2 \frac{V}{r_{i_1}} - \frac{V}{R_C} + I = 0$$

$$V\left[\frac{1}{r_{i_1}} + \frac{\beta_1}{r_{i_1}} + \frac{\beta_1 \beta_2}{r_{i_1}} + \frac{1}{R_C}\right] = I$$

$$Z_o = \frac{V}{I} = \frac{1}{\frac{1}{r_{i_1}} + \frac{\beta_1}{r_{i_1}} + \frac{\beta_1 \beta_2}{r_{i_1}} + \frac{1}{R_C}}$$

or
$$Z_o = \frac{1}{\frac{1}{r_{i_1}} + \frac{1}{(r_{i_1}/\beta_1)} + \frac{1}{(r_{i_1}/\beta_1\beta_2)} + \frac{1}{R_C}} \tag{5.42}$$

From Equation (5.42), Z_o can be interpreted as the parallel combination of r_{i_1}, $\frac{r_{i_1}}{\beta_1}$, $\frac{r_{i_1}}{\beta_1\beta_2}$ and R_C.

i.e
$$Z_o = r_{i_1} \| \frac{r_{i_1}}{\beta_1} \| \frac{r_{i_1}}{\beta_1\beta_2} \| R_C \tag{5.43}$$

Since $\frac{r_{i_1}}{\beta_1\beta_2}$ is the smallest of all, we can take

$$Z_o \approx \frac{r_{i_1}}{\beta_1\beta_2} \tag{5.44}$$

Example 5.6

For the feedback pair of Fig. 5.12 the following data are available:

$R_B = 2\ \text{M}\Omega$ $R_C = 100\ \Omega$ $\beta_1 = 140$ $\beta_2 = 180$
$V_{CC} = 18\ \text{V}$ $V_i = 120\ \text{mV}$ $r_{i_1} = 4\ \text{k}\Omega$

(a) Calculate the dc bias currents and Voltages.
(b) Calculate Z_i and Z_o
(c) Calculate A_V and A_I
(d) Determine V_o

Solution

(a)
$$I_{B_1} = \frac{V_{CC} - V_{EB_1}}{R_B + \beta_1\beta_2 R_C}$$
$$= \frac{18\,\text{V} - 0.7\,\text{V}}{2\,\text{M}\Omega + (140)(180)(100\,\Omega)} = 3.83\ \mu\text{A}$$
$$I_{B_2} = I_{C_1} = \beta_1 I_{B_1} = (140)\ (3.83\ \mu\text{A}) = 0.536\ \text{mA}$$
$$I_{C_2} = \beta_2 I_{B_2} = (180)\ (0.536\ \text{mA}) = 96.48\ \text{mA}$$
$$I_C = I_{E_1} + I_{C_2} \approx I_{C_1} + I_{C_2}$$
$$= 0.536\ \text{mA} + 96.48\ \text{mA} = 97.01\ \text{mA}$$
$$V_{CC} = I_C R_C + V_{CE_2}$$
$$V_{CE_2} = V_{o\,(dc)} = V_{CC} - I_C R_C$$
$$= 18\ \text{V} - (97.01\ \text{mA})\ (100\ \Omega)$$
$$= 8.29\ \text{V} \qquad \text{[DC output voltage]}$$

Also $V_{CC} = I_C R_C - V_{EB_1} + V_{B_1}$

$V_{B_1} = V_{CC} - I_C R_C - V_{EB_1}$

or $V_{B_1} = V_{i\,(dc)} = V_{o\,(dc)} - V_{EB_1} = 8.29\text{ V} - 0.7\text{ V}$

$= 7.59\text{ V}$ [DC input voltage]

(b) $Z_b = r_{i_1} + \beta_1 \beta_2 R_C$

$= 4\text{ k}\Omega + (140)\,(180)\,(100\ \Omega) = 2.524\text{ M}\Omega$

$Z_i = R_B \parallel Z_b = 2\text{ M}\Omega \parallel 2.524\text{ M}\Omega = 1.12\text{ M}\Omega$

$$Z_o = r_{i_1} \parallel \frac{r_{i_1}}{\beta_1} \parallel \frac{r_{i_1}}{\beta_1 \beta_2} \parallel R_C$$

$$= 4\text{ k}\Omega \parallel \frac{4\text{k}\Omega}{140} \parallel \frac{4\text{k}\Omega}{(140)(180)} \parallel 100\ \Omega = 0.158\ \Omega$$

(c) $$A_V = \frac{\beta_1 \beta_2 R_C}{\beta_1 \beta_2 R_C + r_{i_1}}$$

$$= \frac{(140)(180)(100\Omega)}{(140)(180)(100\Omega) + 4\text{k}\Omega} = 0.9984$$

$$A_I = \beta_1 \beta_2 \frac{R_B}{R_B + Z_b}$$

$$= (140)\,(180)\,\frac{2\text{M}\Omega}{2\text{M}\Omega + 2.254\text{M}\Omega}$$

$= 11.85 \times 10^3$

(d) $V_o = A_V V_i\,(0.9984)\,(120\text{ mV}) = 119.81\text{ mV}$

◆ 5.9 CURRENT MIRROR CIRCUIT

Integrated circuit amplifiers are biased using current mirror circuits, which provide a constant current. The constant current is obtained from an output circuit, which is the reflection or mirror of a constant current developed on one side of the circuit. Figure 5.16 shows the circuit of a current mirror.

The circuit consists of two matched or identical transistors, Q_1 and Q_2, operating at the same temperature, with their base and emitter terminals tied together. The base emitter voltage is therefore the same in two transistors.

The transistor Q_1 is connected as a diode by shorting its collector to base. When the supply Voltage V_{CC} is applied, the base-emitter junction of Q_1 is forward biased and a reference current I_X is established. We can think of V_{BE} as being the result of I_X. The same V_{BE} is applied to the base emitter junction of Q_2. Since the two transistors are identical, the collector current of Q_2 will be the mirror of the reference current I_X.

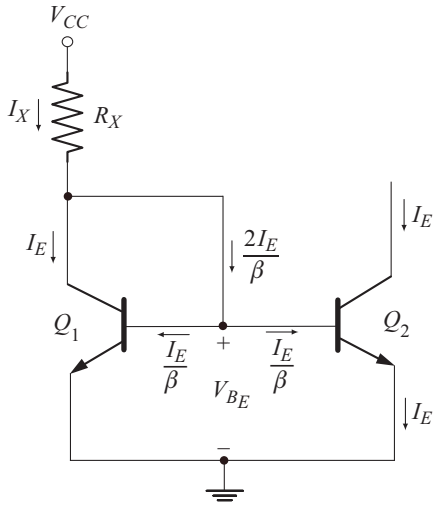


Fig. 5.16 Current mirror circuit

Mathematical Analysis

The base currents of Q_1 and Q_2 are given by

$$I_B = \frac{I_E}{1+\beta}$$

$$\approx \frac{I_E}{\beta}$$

The collector current of each transistor is

$$I_C \approx I_E$$

The current I_X, through the resistor R_X is

$$I_X = I_E + \frac{2I_E}{\beta}$$

$$= \left[1+\frac{2}{\beta}\right] I_E$$

$$= \frac{\beta+2}{\beta} I_E$$

$$I_X \approx I_E \tag{5.45}$$

$$I_X = \frac{V_{CC}-V_{BE}}{R_X} \approx \frac{V_{CC}}{R_X} = \text{constant} \tag{5.46}$$

$$[\text{Since } V_{BE} << V_{CC}]$$

Note that I_X is mirrored in the collector of Q_2.

5.9.1 Current Mirror with High Output Impedance

Figure 5.17 shows the circuit of current mirror with high output impedance. Transistor Q_2 is diode connected. The base emitter voltage is the same for both Q_1 and Q_2.

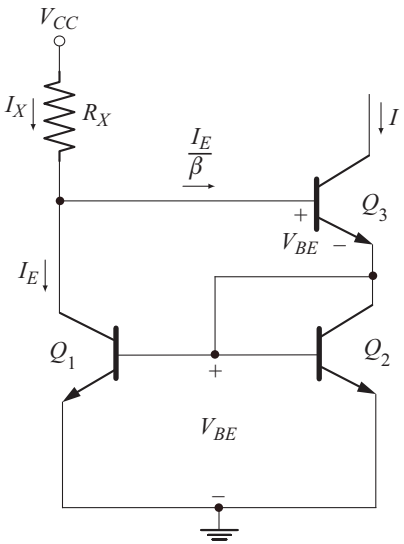


Fig. 5.17 Current mirror circuit with higher output impedance

$$I_X = \frac{V_{CC} - 2V_{BE}}{R_X} \approx \frac{V_{CC}}{R_X} = \text{constant} \tag{5.47}$$

If Q_1 and Q_2 are well matched, their collector currents are equal.

$$\therefore \qquad I \approx I_E \tag{5.47}$$

Now the base current of Q_3 is approximately $\frac{I_E}{\beta}$.

Summing the currents at the collector node of Q_1

$$I_X = I_E + \frac{I_E}{\beta} \approx I_E$$

$$\text{We find that} \qquad I \approx I_E \approx I_X \approx \frac{V_{CC}}{R_X} \tag{5.48}$$

Note that the current I is a mirrored value of the constant current I_X.

5.9.2 Current Mirror using JFET

Figure 5.18 shows the current mirror circuit using junction field effect transistor (JFET). JFET operates in the saturation region providing a constant current I_{DSS} since its gate and drain terminals are tied together.

The collector current of diode connected transistor Q_1 is I_{DSS}. Q_1 and Q_2 are driven by the same base-emitter voltages. If the two transistors are identical, they carry the same collector current. Thus I equals I_{DSS}.

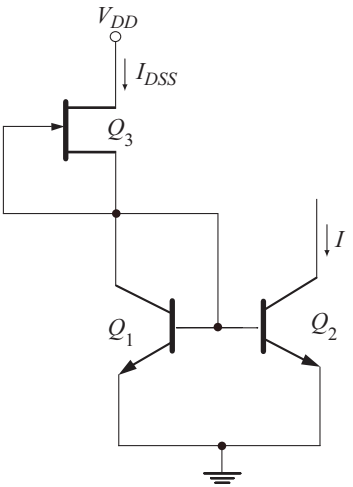
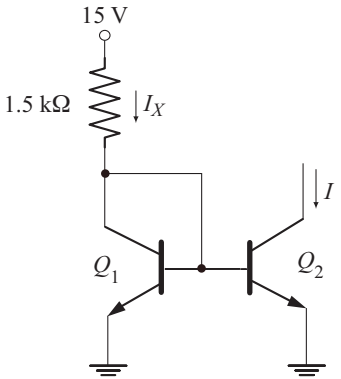


Fig. 5.18 Current mirror using JFET

Example 5.7

Calculate the mirrored current I in the circuit shown below. Take $\beta = 200$ for both the transistors.



Solution

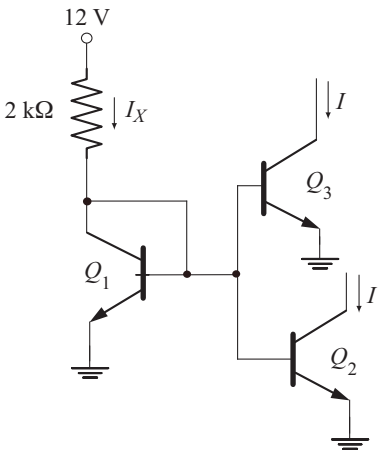
$$I = I_X = \frac{V_{CC} - V_{BE}}{R_X}$$

$$= \frac{15\,\text{V} - 0.7\,\text{V}}{1.5\,\text{k}\Omega}$$

$$= 9.53\ \text{mA}$$

Example 5.8

Calculate the current I through each of the transistor Q_2 and Q_3 shown below.



Solution

I_X equals the sum of collector current of Q_1 and the base currents of Q_1, Q_2 and Q_3

$$\therefore \quad I_X = I_E + 3\,I_B$$

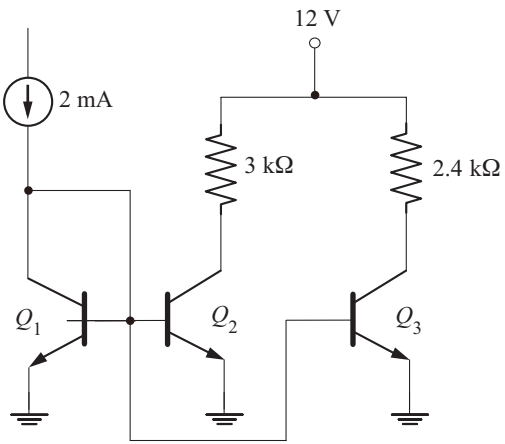
$$= I_E + 3\,\frac{I_E}{\beta} = I_E\left[\frac{\beta+3}{\beta}\right]$$

$$I_X \approx I_E \approx I$$

$$I_X = I = \frac{V_{CC} - V_{BE}}{R_X} = \frac{12\,\text{V} - 0.7\,\text{V}}{2\,\text{k}\Omega} = 5.65\ \text{mA}$$

Example 5.9

Calculate the collector currents of Q_2 and Q_3. Take $\beta = 250$ for all transistors.



Solution

The collector current of Q_1 is 2 mA. Since the base-emitter voltages of Q_1, Q_2 and Q_3 are same, a constant current of 2 mA is mirrored in the collectors of Q_2 and Q_3.

◆ 5.10 CURRENT SOURCE CIRCUITS

A practical current source is represented by a source current in parallel with its source resistance. An ideal current source has infinite source resistance. A good practical current source has large source resistance. Figure 5.19 (a) and 5.19 (b) shows the representation of practical and ideal current sources.

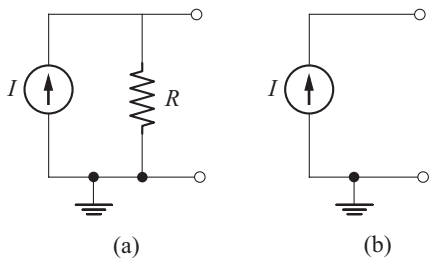


Fig. 5.19 (a) Practical current source (b) Ideal current source

An ideal current source provides a constant current independent of the load connected to it. Constant current sources with very high output resistance finds numerous applications in electronics. Constant-current circuits can be built using BJTs, FETs and a combination of these devices.

◆ 5.11 BJT CONSTANT-CURRENT SOURCE

Figure 5.20 shows a constant-current source using *npn* transistor. The combination of R_1 and R_2 forms a voltage divider between $-V_{EE}$ and ground.

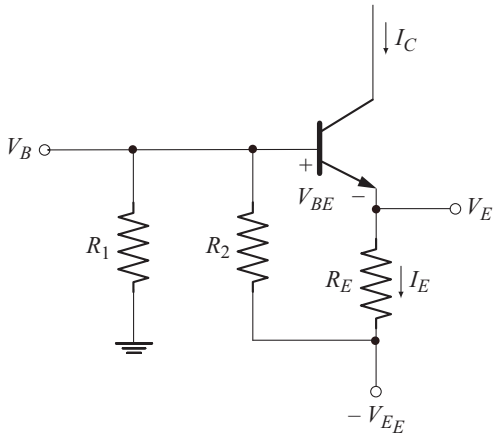


Fig. 5.20 BJT constant-current source

Neglecting base current, the base voltage with respect to ground, using voltage division rule is given by

$$V_B = (-V_{EE})\frac{R_1}{R_1+R_2} \tag{5.49}$$

$$V_{BE} = V_B - V_E$$

$$\Rightarrow \quad V_E = V_B - V_{BE} \tag{5.50}$$

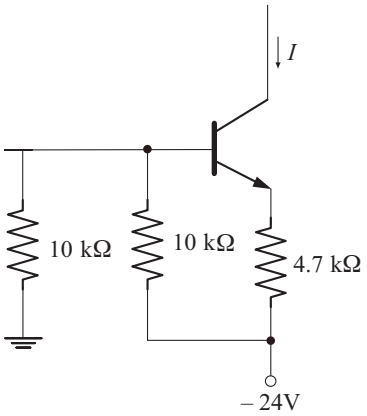
$$I_E = \frac{V_E-(-V_{EE})}{R_E} = \frac{V_E+V_{EE}}{R_E} \approx I_C \tag{5.51}$$

I_C is the constant current provided by the circuit of Fig. 5.20.

The main draw back of this circuit is that I_C depends on V_{BE} (since V_E contains V_{BE} term) which is temperature dependent. Thus I_C varies with temperature. An improved constant current source which uses zener diode in place of R_2 is discussed in the next section.

Example 5.10

Calculate the constant current I in the circuit shown below. Take $\beta = 100$.



Solution

$$V_B = (-V_{EE})\frac{R_1}{R_1+R_2}$$

$$= (-24\text{ V})\frac{10\text{k}\Omega}{10\text{k}\Omega+10\text{k}\Omega} = -12\text{ V}$$

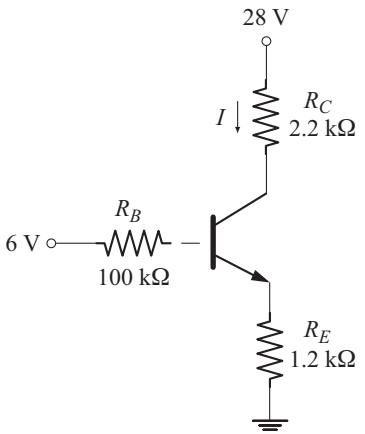
$$V_E = V_B - 0.7\text{ V} = -12\text{ V} - 0.7\text{ V} = -12.7\text{ V}$$

$$I = I_E = \frac{V_E-(-V_{EE})}{R_E}$$

$$= \frac{-12.7\text{V}+24\text{V}}{4.7\text{k}\Omega} = 2.4\text{ mA}$$

Example 5.11

Calculate the current I in the circuit shown below. Take $\beta = 120$.



Solution

$$I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta)R_E} = \frac{6\,\text{V} - 0.7\,\text{V}}{100\,\text{k}\Omega + (121)(1.2\,\text{k}\Omega)} = 21.62\ \mu\text{A}$$

$$I = I_C = \beta\, I_B = (120)\ (21.\ 62\ \mu\text{A}) = 2.59\ \text{mA}$$

5.12 BJT CONSTANT-CURRENT SOURCE USING ZENER DIODE

An improved BJT constant current source using zener diode is shown in Fig. 5.21.

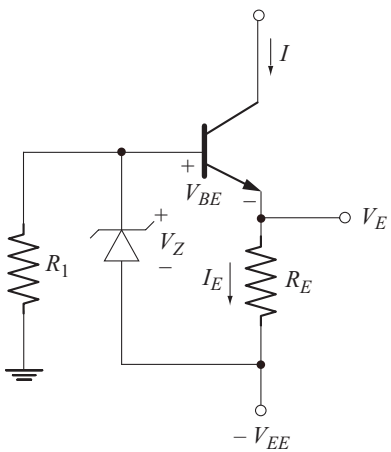


Fig. 5.21 Constant-current source using zener diode

Applying KVL to the base-emitter circuit we have

$$V_Z - V_{BE} - I_E R_E = 0$$

$$I_E = \frac{V_Z - V_{BE}}{R_E} \approx I \tag{5.52}$$

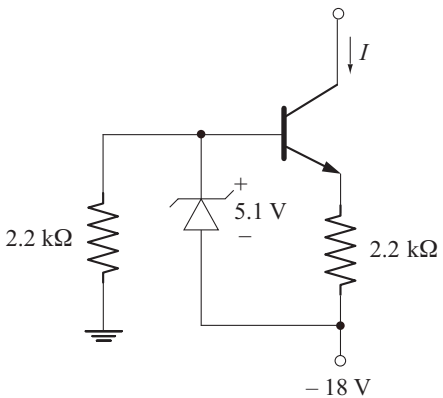
Usually $V_Z \gg V_{BE}$

$$\therefore \quad I \approx I_E = \frac{V_Z}{R_E} \tag{5.53}$$

Note that the current I depends on V_Z and R_E which are both constants. Hence I is essentially a constant current. Also the current I is independent of the supply voltage V_{EE}.

Example 5.12

Calculate the constant current I in the circuit shown below. Take $\beta = 200$.



Solution

$$I \approx I_E = \frac{V_Z - V_{BE}}{R_E} = \frac{5.1\text{V} - 0.7\text{V}}{2.2\text{k}\Omega} = 2\text{ mA}$$

5.13 ANALYSIS OF TRANSISTOR CONFIGURATIONS USING APPROXIMATE HYBRID MODEL

In Chapter 3 we have analysed the various transistor configurations using the r_e model. Now let us proceed to analyse the same using the approximate hybrid model. Figure 5.22 shows the approximate CE hybrid model and the approximate CB hybrid model is shown in Fig. 5.23.

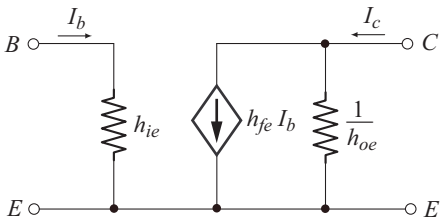


Fig. 5.22 Approximate CE hybrid model

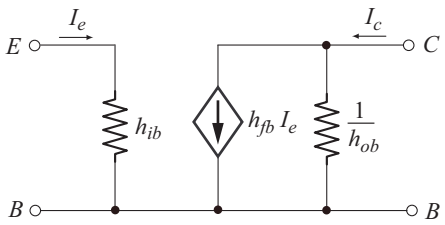


Fig. 5.23 Approximate CB hybrid model

Before starting the analysis, let us recall the relation between the parameters of r_e model and the hybrid model, which has been discussed in Chapter 3.

$$h_{ie} = \beta r_e \qquad h_{fe} = \beta \qquad h_{oe} = \frac{1}{r_o} \qquad \text{[For CE configuration]}$$

$$h_{fb} = -\alpha \qquad h_{ib} = r_e \qquad \text{[For CB configuration]}$$

The approximate hybrid model is very similar in structure to that used with the r_e model. Therefore, all the results derived for the transistor configurations in Chapter 3 using r_e model can be readily applied for the analysis using the hybrid model by simply replacing the parameters of r_e model with their equivalent hybrid parameters.

◆ 5.14 COMMON-EMITTER FIXED BIAS CONFIGURATION

Figure 5.24 shows the circuit of common-emitter configuration using fixed bias. Its small signal ac equivalent circuit using approximate hybrid model is shown in Fig. 5.25.

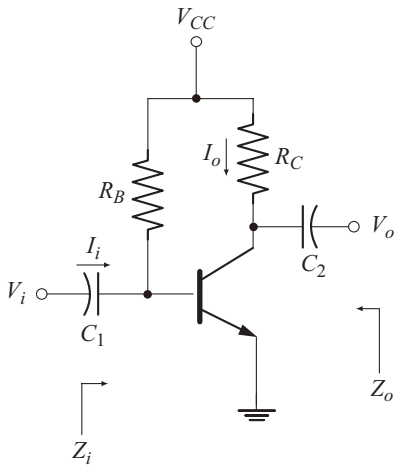


Fig. 5.24 CE fixed bias configuration

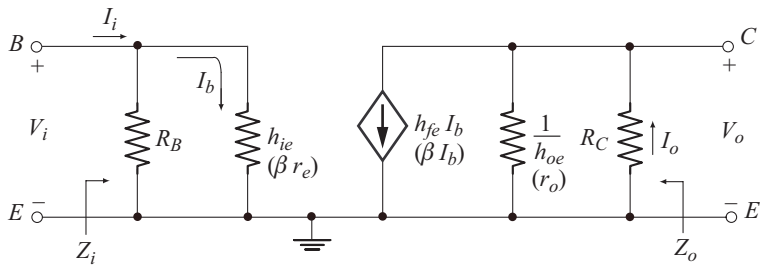


Fig. 5.25 *AC equivalent circuit*

The ac equivalent circuit of Fig. 5.25 is an exact replica of the circuit given in Fig. 3.36 in section 3.18 of Chapter 3. Applying the same procedure we obtain the following results.

- $$Z_i = R_B \parallel h_{ie} = R_B \parallel \beta\, r_e \tag{5.54}$$

- $$Z_i \approx h_{ie} = \beta\, r_e \quad [\text{If } R_B \gg h_{ie}] \tag{5.55}$$

- $$Z_o = \frac{1}{h_{oe}} \parallel R_C = r_o \parallel R_C \tag{5.56}$$

- $$A_V = -\frac{h_{fe}\left[r_o \parallel R_C\right]}{h_{ie}}$$
$$= -\frac{r_o \parallel R_C}{r_e} \tag{5.57}$$

- $$A_I = -A_V \frac{Z_i}{R_C} \tag{5.58}$$

For $\dfrac{1}{h_{oe}} \geq 10\, R_C \equiv r_o \geq 10\, R_C$

- $$Z_o \approx R_C \tag{5.59}$$

- $$A_V \approx -\frac{h_{fe} R_C}{h_{ie}} = -\frac{R_C}{r_e} \tag{5.60}$$

- $$A_I \approx -h_{fe} = -\beta \quad [\text{Taking } Z_i \approx h_{ie} = \beta\, r_e] \tag{5.61}$$

◆ 5.15 COMMON-EMITTER CONFIGURATION USING VOLTAGE DIVIDER BIAS

Figure 5.26 shows common-emitter configuration using voltage divider bias. The results of previous section can also be applied to this circuit. The only change is that R_B has to be replaced by $R_1 \parallel R_2$.

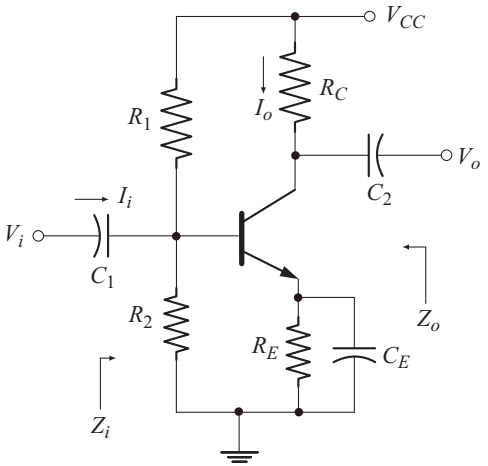


Fig. 5.26 CE Voltage divider bias configuration

Example 5.13

The following data are available for the amplifier circuit of Fig. 5.26.

$R_1 = 68\ \text{k}\Omega$ $R_2 = 12\ \text{k}\Omega$ $R_C = 2.2\ \text{k}\Omega$ $R_E = 1.2\ \text{k}\Omega$
$V_{CC} = 18\ \text{V}$ $h_{fe} = 180$ $h_{ie} = 2.75\ \text{k}\Omega$ $h_{oe} = 25\ \mu\text{S}$

(a) Calculate Z_i and Z_o
(b) Calculate A_V and A_I
(c) Determine r_e and compare βr_e with h_{ie}.

Solution

(a)

$$Z_i = R_1 \parallel R_2 \parallel h_{ie}$$

$$R_1 \parallel R_2 = R' = 68\ \text{k}\Omega \parallel 12\ \text{k}\Omega = 10.2\ \text{k}\Omega$$

$$Z_i = 10.2\ \text{k}\Omega \parallel 2.75\ \text{k}\Omega = 2.17\ \text{k}\Omega$$

$$Z_o = \frac{1}{h_{oe}} \parallel R_C = R'_C$$

$$\frac{1}{h_{oe}} = \frac{1}{25\,\mu\text{s}} = 40\ \text{k}\Omega$$

$$Z_o = 40\ \text{k}\Omega \parallel 2.2\ \text{k}\Omega = 2.09\ \text{k}\Omega$$

(b)

$$A_V = -\frac{h_{fe} R'_C}{h_{ie}}$$

$$= -\frac{(180)\ (2.09\ \text{k}\Omega)}{2.75\ \text{k}\Omega} = -136.8$$

$$A_I = -\frac{A_V Z_i}{R_C} = -\frac{(-136.8)(2.17\,\text{k}\Omega)}{2.2\,\text{k}\Omega}$$
$$= 134.93$$

(c) Check for $\beta R_E \geq 10 R_2$

$$\beta = h_{fe} = 180$$
$$\beta R_E = (180)\,(1.2\ \text{k}\Omega) = 216\ \text{k}\Omega$$
$$10 R_2 = (10)\,(12\ \text{k}\Omega) = 120\ \text{k}\Omega$$

Since $\beta R_E > 10 R_2$, we can use approximate analysis.

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{18\ \text{V}(12\ \text{k}\Omega)}{68\ \text{k}\Omega + 12\ \text{k}\Omega} = 2.7\ \text{V}$$
$$V_E = V_B - V_{BE} = 2.7\ \text{V} - 0.7\ \text{V} = 2\ \text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{2\ \text{V}}{1.2\ \text{k}\Omega} = 1.67\ \text{mA}$$
$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.67\ \text{mV}} = 15.56\Omega$$
$$\beta r_e = (180)\,(15.56\Omega) = 2.8\ \text{k}\Omega$$

Note that βr_e is nearly equal to h_{ie}.

◆ 5.16 CE-EMITTER BIAS CONFIGURATION WITH UNBYPASSED R_E

Figure 5.27 shows the CE emitter bias configuration with unbypassed R_E. The small signal ac equivalent circuit using approximate hybrid model is shown in Fig. 5.28. To simplify the analysis $\frac{1}{h_{oe}}$ is treated as an open circuit.

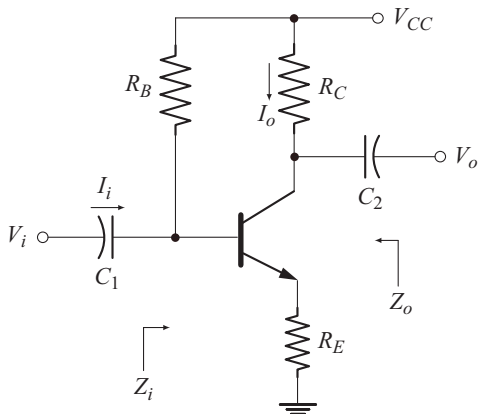


Fig. 5.27 Emitter bias configuration with un bypassed R_E

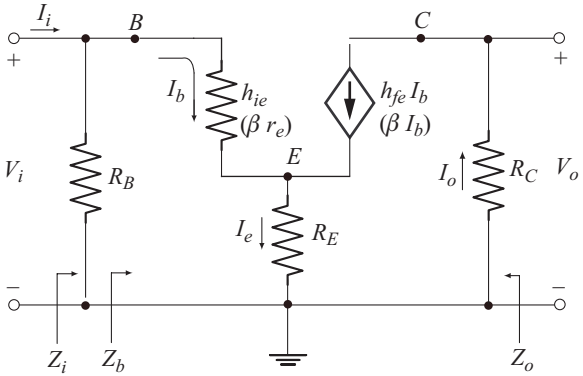


Fig. 5.28 Small signal ac equivalent circuit

The ac equivalent circuit of Fig. 5.28 is an exact duplicate of the circuit given in Fig. 3.45 in section 3.20 of Chapter 3. Applying the same procedure we obtain the following results.

- $$Z_b = h_{ie} + (1 + h_{fe})\, R_E = \beta\, r_e + (1 + \beta)\, R_E \tag{5.62}$$
- $$Z_i \approx R_B \,\|\, Z_b \tag{5.63}$$
- $$A_V = -\frac{h_{fe}\, R_C}{h_{ie} + (1 + h_{fe}) R_E} \tag{5.64}$$
- $$A_I = -A_V \frac{Z_i}{R_C} \tag{5.65}$$
- $$Z_o = R_C \tag{5.66}$$

Using the approximations

$$1 + h_{fe} \approx h_{fe} \equiv 1 + \beta \approx \beta$$

$$h_{fe}\, R_E \gg h_{ie} \equiv \beta\, R_E \gg \beta\, r_e \quad \text{we get}$$

- $$Z_b \approx h_{fe}\, R_E = \beta\, R_E \tag{5.67}$$
- $$A_V \approx -\frac{R_C}{R_E} \tag{5.68}$$

Example 5.14

For the amplifier circuit of Fig. 5.27 the following data are available.

$R_B = 330\ \text{k}\Omega$ $R_E = 1\ \text{k}\Omega$ $R_C = 3.3\ \text{k}\Omega$ $V_{CC} = 12\ \text{V}$
$h_{fe} = 120$ $h_{ie} = 2\ \text{k}\Omega$ $h_{oe} = 20\ \text{mA/V}$

(a) Calculate Z_i and Z_o
(b) Calculate A_V and A_I
(c) Determine V_o if $V_i = 100$ mV

Solution

(a)
$$Z_b = h_{ie} + (1 + h_{fe})\, R_E$$
$$= 2\ \text{k}\Omega + (121)\ (1\ \text{k}\Omega\ ) = 123\ \text{k}\Omega$$
$$Z_i = R_B \parallel Z_b = 330\ \text{k}\Omega\ \parallel 123\ \text{k}\Omega = 89.6\ \text{k}\Omega$$
$$Z_o = R_C = 3.3\ \text{k}\Omega$$

(b)
$$A_V = -\frac{h_{fe}\, R_C}{h_{ie} + (1 + h_{fe})\, R_E}$$
$$= -\frac{(120)(3.3\,\text{k}\Omega)}{2\,\text{k}\Omega + (121)(1\,\text{k}\Omega)} = -3.22$$
$$A_I = -\frac{A_V\, Z_i}{R_C} = -\frac{(-3.22)(89.6\ \text{k}\Omega)}{3.3\ \text{k}\Omega} = 87.43$$

(c)
$$V_o = A_V\, V_i = (-3.22)\ (100\ \text{mV}) = -322\ \text{mV}$$

◆ 5.17 EMITTER FOLLOWER CONFIGURATION

Figure 5.29 shows the circuit of emitter follower. The small signal ac equivalent circuit of emitter follower using approximate hybrid model is shown in Fig. 5.30. For simplicity h_{oe} is not included in the model.

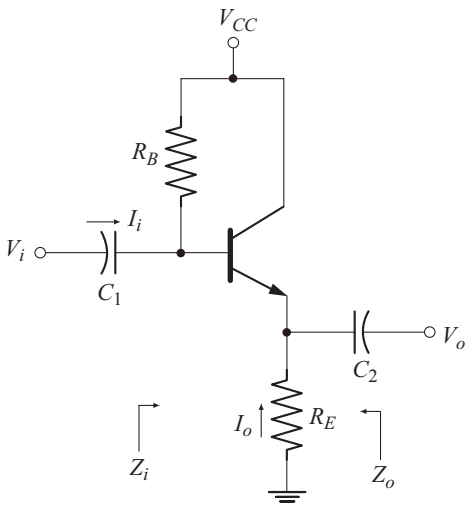


Fig. 5.29 Emitter-follower configuration

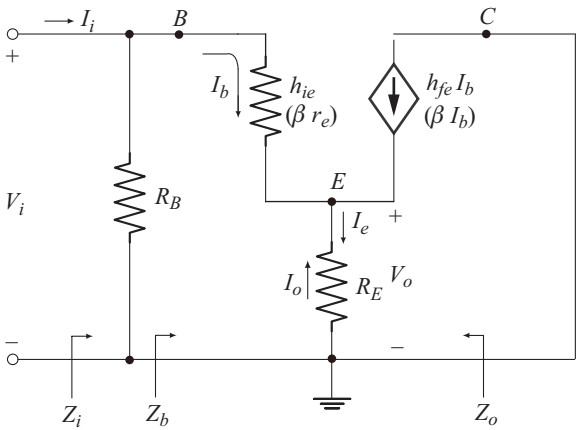


Fig. 5.30 Small signal ac equivalent circuit of emitter follower

$$Z_b = h_{ie} + (1 + h_{fe})\, R_E = \beta\, r_e + (1 + \beta)\, R_E \tag{5.69}$$

$$\approx h_{fe}\, R_E = \beta\, R_E \tag{5.70}$$

$$Z_i = Z_b \,||\, R_B \tag{5.71}$$

$$Z_o = R_E \,||\, \frac{h_{ie}}{1 + h_{fe}} = R_E \,||\, r_e \tag{5.72}$$

$$\approx \frac{h_{ie}}{h_{fe}} = r_e \tag{5.73}$$

$$A_V = \frac{\left(1 + h_{fe}\right) R_E}{h_{ie} + \left(1 + h_{fe}\right) R_E} \tag{5.74}$$

$$\approx \frac{h_{fe}\, R_E}{h_{ie} + h_{fe}\, R_E} \tag{5.75}$$

$$= \frac{R_E}{r_e + R_E} \approx 1 \tag{5.76}$$

$$A_I \approx - \frac{A_V\, Z_i}{R_C} \tag{5.77}$$

5.18 COMMON-BASE CONFIGURATION

Figure 5.31 shows the circuit of common base configuration. Its small signal ac equivalent circuit using approximate hybrid model is shown in Fig. 5.32. Again for simplicity h_{ob} is not included in the model.

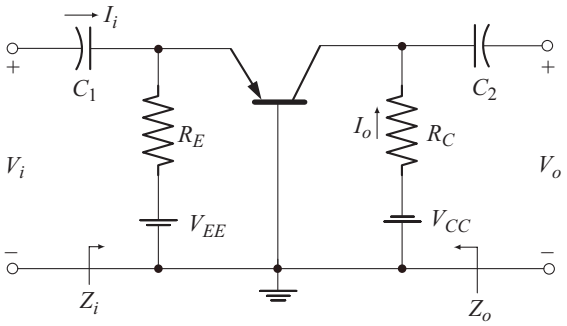


Fig. 5.31 Common-base configuration

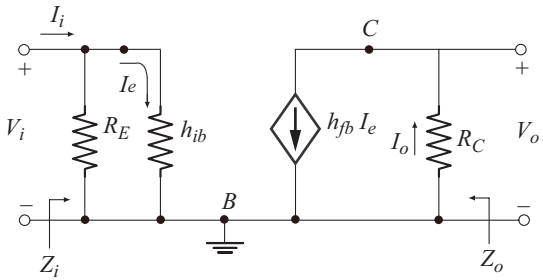


Fig. 5.32 Small signal ac equivalent circuit of CB configuration

Using the procedure given in section 3.27 of Chapter 3 we obtain the following results.

- $$Z_i = R_E \,||\, h_{ib} = R_E \,||\, r_e \approx r_e$$
- $$Z_o = R_C$$
- $$A_V = -\frac{h_{fb}\, R_C}{h_{ib}} = \frac{\alpha\, R_C}{r_e}$$
- $$A_I = -h_{fb} = \alpha$$

5. 19 ANALYSIS OF GENERAL TRANSISTOR CONFIGURATION USING THE COMPLETE HYBRID EQUIVALENT MODEL

So for we have analyzed all the three transistor configurations by substituting the relevant approximate hybrid model in the ac equivalent circuit. In this section we are analyzing the transistor amplifier using the general complete hybrid equivalent model, which has all the four parameters h_i, h_f, h_r and h_o. The results can be modified for the specific transistor configuration by replacing the general hybrid parameters with the appropriate hybrid parameters of transistor configuration under consideration.

We begin our analysis by writing the transistor amplifier as a two port network, driven by a source V_S of internal resistance R_S and driving a load R_L as shown in Fig. 5.33.

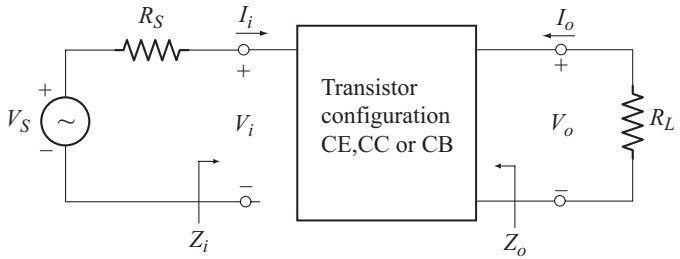


Fig. 5.33 Two-port system

Let us replace the transistor by its general, complete hybrid equivalent model as shown in Fig. 5.34.

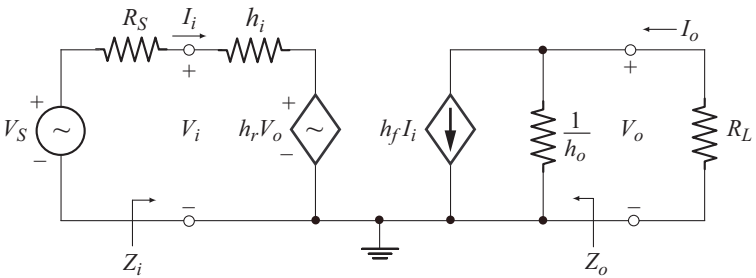


Fig. 5.34 Small signal ac equivalent circuit using the complete hybrid equivalent modes

Current Gain **[A_I]**

The current gain is defined by

$$A_I = \frac{I_o}{I_i} \tag{5.78}$$

Applying KCL to the output circuit we have

$$I_o = h_f I_i + h_o V_o$$

Using $V_o = -I_o R_L$ we get

$$I_o = h_f I_i + h_o(-I_o R_L)$$

$$I_o[1 + h_o R_L] = h_f I_i$$

$$A_I = \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L} \tag{5.79}$$

Input Impedance **[Z_i]**

Applying KVL to the input circuit of Fig. 5.34 we have

$$V_i - I_i h_i - h_r V_o = 0$$

$$V_i = I_i h_i + h_r [-I_o R_L] \tag{5.80}$$

But $$A_I = \frac{I_o}{I_i} \quad \Rightarrow \quad I_o = A_I I_i$$

Using this relation in Equation (5.80) we get

$$V_i = I_i h_i - h_r A_I R_L I_i$$

Now $$Z_i = \frac{V_i}{I_i} = h_i - h_r A_I R_L \tag{5.81}$$

Substituting for A_I from Equation (5.79) we have

$$Z_i = h_i - \frac{h_f h_r R_L}{1 + h_o R_L} \tag{5.82}$$

***Voltage Gain* [A_V]**

$$V_o = -I_o R_L$$

$$V_i = I_i Z_i$$

Now $$A_V = \frac{V_o}{V_i} = \frac{-I_o R_L}{I_i Z_i}$$

or $$A_V = -\frac{A_I R_L}{Z_i} \tag{5.83}$$

From Equation (5.82)

$$Z_i = \frac{h_i + \left(h_i h_o - h_f h_r\right) R_L}{1 + h_o R_L}$$

And from Equation (5.79)

$$A_I = \frac{h_f}{1 + h_o R_L}$$

Using these relations in Equation (5.83) we obtain

$$A_V = \frac{-h_f R_L}{1 + h_o R_L} \cdot \frac{1 + h_o R_L}{h_i + (h_i h_o - h_f h_r) R_L}$$

$$A_V = \frac{-h_f R_L}{h_i + (h_i h_o - h_f h_r) R_L} \tag{5.84}$$

***Output Impedance* [Z_o]**

To find the output impedance, V_S is reduced to zero and a voltage source V is connected between the output terminals after removing R_L as shown in Fig. 5.35.

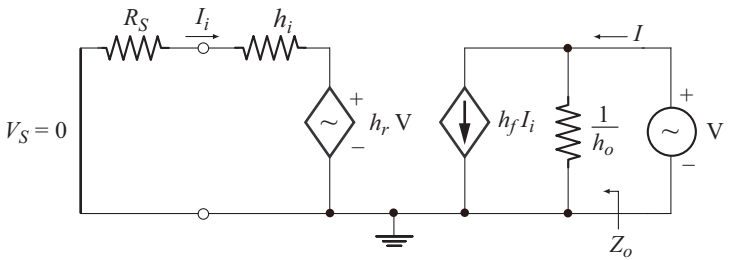


Fig. 5.35 Circuit to find Z_o

Applying KCL to the output circuit we have

$$\mathrm{I} = h_f I_i + h_o \mathrm{V} \tag{5.85}$$

Writing KVL equation to the input circuit

$$-I_i(R_S + h_i) - h_r \mathrm{V} = 0$$

$$I_i = \frac{-h_r \mathrm{V}}{R_S + h_i}$$

Using this relation in Equation (5.85) we have

$$I = -\frac{h_f h_r \mathrm{V}}{R_S + h_i} + h_o \mathrm{V}$$

$$\frac{I}{V} = \frac{1}{Z_o} = h_o - \frac{h_f h_r}{R_S + h_i} \tag{5.86}$$

$$Z_o = \frac{1}{h_o - \left[h_f h_r / (R_S + h_i)\right]} \tag{5.87}$$

$$\text{If } R_s = 0, \qquad Z_o = \frac{1}{h_o - \left[h_f h_r / h_i\right]} \tag{5.88}$$

Example 5.15

For the circuit shown, using the complete hybrid equivalent model.

(a) Calculate Z_i' and Z_i

(b) Determine Z_o (including R_C) and Z_o' (without R_C)

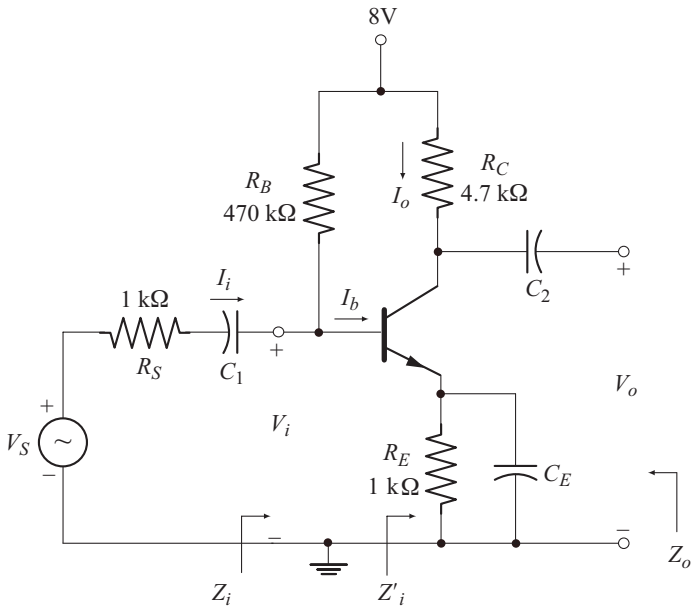
(c) Calculate $A_I = \frac{I_o}{I_i}$ and $A_I' = \frac{I_o}{I_b}$

(d) Calculate A_V and A_{V_S}

(e) Repeat all calculations using approximate hybrid model and compare the results.

The hybrid parameters are

$$h_{ie} = 1.6\ \text{k}\Omega \quad h_{fe} = 110 \quad h_{re} = 2 \times 10^{-4} \quad h_{oe} = 20\ \mu\text{A/V}$$



Solution

The transistor is in CE configuration. Therefore in the general hybrid model of Fig. 5.40, we have to replace h_i, h_f, h_r and h_o by h_{ie}, h_{fe}, h_{re} and h_{oe} respectively.

The small signal ac equivalent circuit using the complete hybrid model is shown in Fig. A.

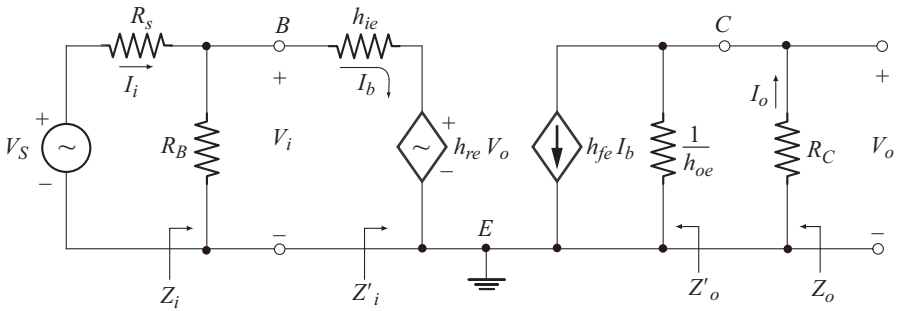


Fig. A

To obtain the correct results, it is important to compare the circuits of Fig. 5.34 and Fig. A and appropriately use the results obtained in section 5.19.

(a) *Input Impedance* [Z_i]

From Equation (5.82)

$$Z_i = h_{ie} - \frac{h_{fe}\,h_{re}\,R_L}{1+h_{oe}\,R_L}$$

Derivation of Z_i does not include R_B. Hence in the present context the input impedance given by the above equation is Z_i' as indicated in Fig. A.

$$\text{Also} \qquad R_L = R_C$$

$$\therefore \qquad Z_i' = \frac{V_i}{I_b} = h_{ie} - \frac{h_{fe}\, h_{re}\, R_C}{1 + h_{oe}\, R_C} \tag{A}$$

$$= 1.6\ \text{k}\Omega - \frac{(110)\left(2\times10^{-4}\right)(4.7\ \text{k}\Omega)}{1 + \left(20\times10^{-6}\right)(4.7\ \text{k}\Omega)} = 1.51\ \text{k}\Omega$$

Input impedance taking R_B into account is

$$Z_i = \frac{V_i}{I_i} = R_B \parallel Z_i' = 470\ \text{k}\Omega \parallel 1.51\ \text{k}\Omega = 1.51\ \text{k}\Omega.$$

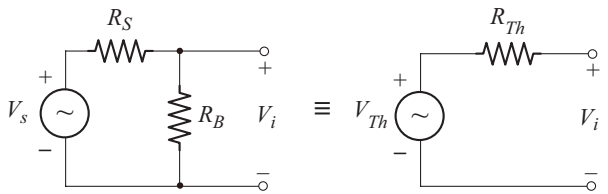
[For voltage divider bias, $R_B = R_1 \parallel R_2$]

(b) *Output Impedance*

From Equation (5.87)

$$Z_o = \frac{1}{h_{oe} - \left[\dfrac{h_{fe}\, h_{re}}{R_s + h_{ie}}\right]}$$

In the present situation the output impedance given by the above equation is Z_o'. Also R_S should be replaced by the Thevenin resistance R_{Th} of the circuit comprising of V_S, R_S and R_B which is shown below.



$$R_{Th} = R_S \parallel R_B = 1\ \text{k}\Omega \parallel 470\ \text{k}\Omega = 0.998\ \text{k}\Omega \quad [\textbf{If } \boldsymbol{R_S = 0,\ R_{Th} = 0}]$$

$$Z_o' = \frac{1}{h_{oe} - \left[\dfrac{h_{fe}\, h_{re}}{R_{Th} + h_{ie}}\right]} \tag{B}$$

$$Z_o' = \frac{1}{20\times10^{-6} - \left[\dfrac{(110)(2\times10^{-4})}{0.998\ \text{k}\Omega + 1.6\ \text{k}\Omega}\right]} = 86.72\ \text{k}\Omega$$

The output impedance taking R_C into account is

$$Z_o = Z_o' \parallel R_C = 86.72\ \text{k}\Omega \parallel 4.7\ \text{k}\Omega = 4.46\ \text{k}\Omega$$

(c) Current Gain

From Equation (5.79)

$$A_I = \frac{I_o}{I_i} = \frac{h_{fe}}{1+h_{oe}\,R_L}$$

In the present situation the current gain given by the above equation is $A_I' = \frac{I_o}{I_b}$. also $R_L = R_C$.

$$A_I' = \frac{I_o}{I_b} = \frac{h_{fe}}{1+h_{oe}\,R_C} \qquad \text{(C)}$$

$$= \frac{110}{1+(20\times10^{-6})(4.7\ \text{k}\Omega)} = 100.55$$

$$A_I = \frac{I_o}{I_i} = \frac{I_o}{I_b}\cdot\frac{I_b}{I_i} = (100.55)\,\frac{I_b}{I_i}$$

Applying current division rule in the input circuit of Fig. A we have

$$I_b = \frac{I_i\,R_B}{R_B+Z_i'}$$

$$\frac{I_b}{I_i} = \frac{R_B}{R_B+Z_i'} = \frac{470\ \text{k}\Omega}{470\ \text{k}\Omega+1.51\ \text{k}\Omega} = 0.997$$

Now $A_I = (100.55)\,(0.997) = 100.25$

(e) *Voltage Gain*

$$A_V = \frac{V_o}{V_i} = \frac{-I_o\,R_C}{I_i\,Z_i} = -\frac{A_I\,R_C}{Z_i} \qquad \text{(D)}$$

$$= -\frac{(100.25)(4.7\ \text{k}\Omega)}{1.51\ \text{k}\Omega} = -312$$

$$A_{V_S} = \frac{V_o}{V_S} = \frac{V_o}{V_i}\cdot\frac{V_i}{V_S} = A_V\,\frac{V_i}{V_S} \qquad \text{(E)}$$

Using voltage division rule in the circuit of Fig (B) we have

$$\frac{V_i}{V_S} = \frac{Z_i}{Z_i+R_S}$$

$$= \frac{1.51\ \text{k}\Omega}{1.51\ \text{k}\Omega+1\ \text{k}\Omega}$$

$$= 0.602$$

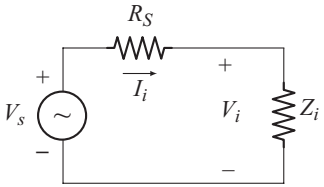


Fig B

Now $A_{V_S} = (-312)(0.602)$

$= -187.82$ [**If** $\boldsymbol{R_S = 0, A_{V_S} = A_V}$]

(e) To obtain the results using approximate hybrid model, we have to substitute $h_{re} = 0$ in Equations (A) to (E).

From Equation (A), with $h_{re} = 0$

$$Z_i' = h_{ie} = 1.6\ \text{k}\Omega$$

$$Z_i = R_B \| h_{ie}$$

$$= 470\ \text{k}\Omega \| 1.6\ \text{k}\Omega = 1.595\ \text{k}\Omega$$

From Equation (B)

$$Z_o' = \frac{1}{h_{oe}} = \frac{1}{20\times10^{-6}\ \text{℧}} = 50\ \text{k}\Omega$$

$$Z_o = Z_o' \| R_C = 50\ \text{k}\Omega \| 4.7\ \text{k}\Omega = 4.29\ \text{k}\Omega$$

$$A_I = A_I \approx h_{fe} = 110$$

$$A_V = -\frac{A_I R_C}{Z_i} = -\frac{(110)(4.7\,\text{k}\Omega)}{1.595\,\text{k}\Omega} = -324.14$$

$$A_{V_S} = A_V \frac{Z_i}{Z_i + R_S}$$

$$= (-324.14)\left[\frac{1.595\ \text{k}\Omega}{1.595\ \text{k}\Omega + 1\ \text{k}\Omega}\right]$$

$$= -199.23$$

The following table compares the results obtained using exact and approximate hybrid models.

Parameter	*Exact model*	*Approximate model*
Z_i	1.51 kΩ	1.595 kΩ
Z_o	4.46 kΩ	4.29 kΩ
A_I	100.25	110
A_V	– 312	– 324.14

Note:

- A similar procedure can be used for CC [emitter follower] and CB configurations.
- If CE parameters are given, CB and CC parameters can be obtained using the conversion equations given in section 3.16.1 of Chapter 3.

Example 5.16

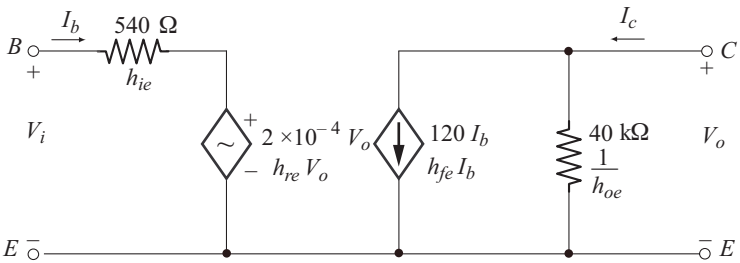
Given $\beta = 120, \quad r_e = 4.5\ \Omega, \quad r_o = 40\ \text{k}\Omega, \quad h_{re} = 2 \times 10^{-4}$

(a) Sketch the complete hybrid model
(b) Sketch the approximate hybrid model
(c) Sketch r_e model

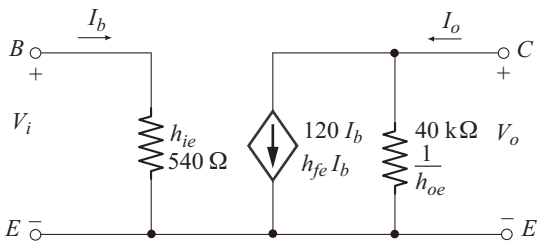
Solution

$$h_{ie} = \beta r_e = (120)\,(4.5\ \Omega) = 540\ \Omega$$
$$h_{fe} = \beta = 120$$
$$h_{oe} = \frac{1}{r_o} = \frac{1}{40\,\text{k}\Omega} = 25\ \mu\text{℧}$$

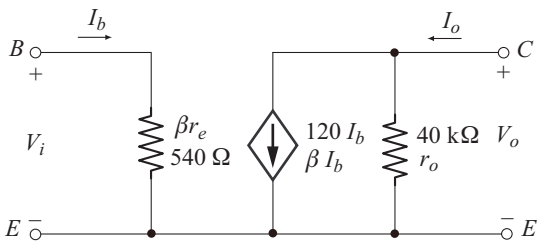
(a) Complete hybrid model



(b) Approximate hybrid model



(c) r_e model



Note that the r_e model and the approximate hybrid model are identical except for the difference in symbols.

Example 5.17

For the circuit shown below, using the complete hybrid model:

(a) Calculate Z_i and Z'_i

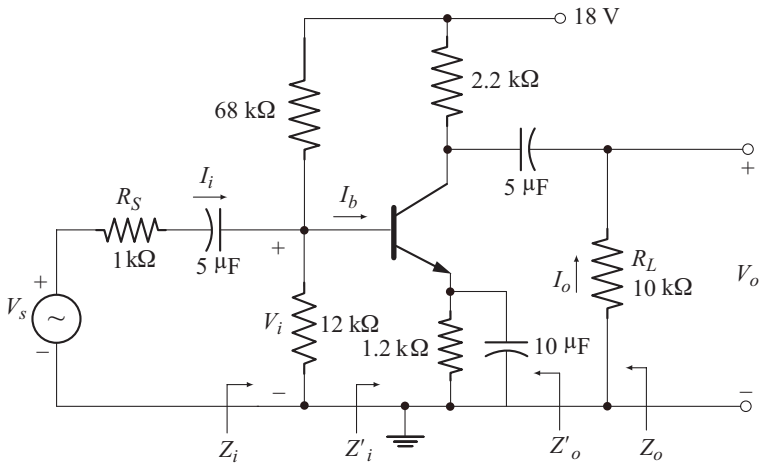
(b) Calculate Z_o and Z'_o

(c) Determine $A_I = I_o/I_i$ and $A'_I = I_o/I_b$

(d) Determine A_V and A_{V_S}

The hybrid parameter values of the transistor are:

$$h_{fe} = 180 \quad h_{ie} = 2.75\ \text{k}\Omega \quad h_{oe} = 25\ \mu\text{S} \quad h_{re} = 2 \times 10^{-4}$$



Solution

The circuit contains both R_C and R_L. Hence it is better to derive the results and then calculate their numerical values. The small signal equivalent circuit using the complete hybrid model is shown in Fig. A.

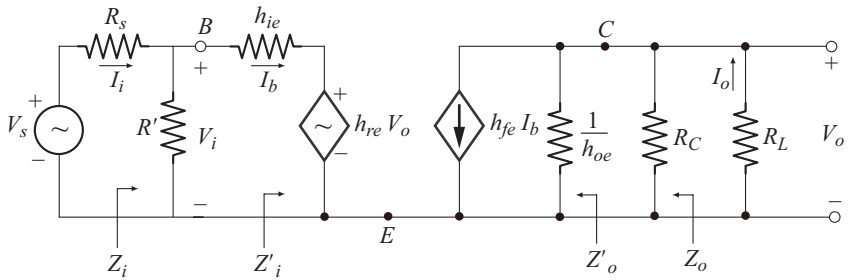


Fig. A

$$R' = R_1 \,||\, R_2 = 68\ \text{k}\Omega \,||\, 12\ \text{k}\Omega = 10.2\ \text{k}\Omega$$

(a) Input Impedance

Applying KVL to the input circuit we have

$$V_i = h_{ie} I_b + h_{re} V_o \qquad \text{(A)}$$

Let $$R = \frac{1}{h_{oe}} \| R_C \| R_L$$

$$R = 40\ \text{k}\Omega \| 2.2\ \text{k}\Omega \| 10\ \text{k}\Omega = 1.73\ \text{k}\Omega$$

The simplified output circuit is shown in Fig. B.

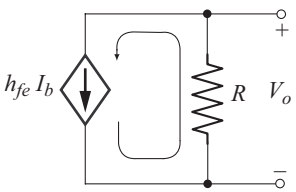


Fig B

From the circuit of Fig. B.

$$V_o = -h_{fe} I_b R$$

Using this relation in Equation (A) we have

$$V_i = h_{ie} I_b - h_{fe} h_{re} R I_b$$

Now $$Z'_i = \frac{V_i}{I_b} = h_{ie} - h_{fe} h_{re} R \qquad \text{(B)}$$

$$= 2.75\ \text{k}\Omega - (180)(2 \times 10^{-4})(1.73\ \text{k}\Omega)$$

$$= 2.69\ \text{k}\Omega$$

$$Z_i = \frac{V_i}{I_i} = R' \| Z'_i = 10.2\ \text{k}\Omega \| 2.69\ \text{k}\Omega = 2.13\ \text{k}\Omega$$

(b) *Output Impedance*

Z'_o does not include R_C. Hence

$$Z'_o = \frac{1}{h_{oe} - \dfrac{h_{fe} h_{re}}{R_{Th} + h_{ie}}}$$

$$R_{Th} = R' \| R_S = 10.2\ \text{k}\Omega \| 1\ \text{k}\Omega = 0.91\ \text{k}\Omega$$

$$Z'_o = \frac{1}{25 \times 10^{-6} - \dfrac{(180)(2 \times 10^{-4})}{0.91\text{k}\Omega + 2.75\text{k}\Omega}} = 65.95\ \text{k}\Omega$$

$$Z_o = Z'_o \| R_C = 65.95\ \text{k}\Omega \| 2.2\ \text{k}\Omega = 2.14\ \text{k}\Omega$$

(c) *Current Gain*

Applying KCL to the output circuit of Fig. A we have

$$I_o = h_{fe} I_b + h_{oe} V_o + \frac{V_o}{R_C}$$

Using $V_o = -I_o R_L$, we get

$$I_o = h_{fe} I_b + h_{oe} (-I_o R_L) + \frac{(-I_o R_L)}{R_C}$$

$$I_o \left[1 + h_{oe} R_L + \frac{R_L}{R_C}\right] = h_{fe} I_b$$

Now
$$A_I' = \frac{I_o}{I_b} = \frac{h_{fe}}{1 + h_{oe} R_L + \frac{R_L}{R_C}} \qquad \text{(C)}$$

$$= \frac{180}{1 + (25 \times 10^{-6})(10\,\text{k}\Omega) + \left[\frac{10\,\text{k}\Omega}{2.2\,\text{k}\Omega}\right]}$$

$$= 31.06$$

$$A_I = \frac{I_o}{I_i} = A_I' \cdot \frac{Z_i'}{R' + Z_i'}$$

$$= (31.06)\ \frac{2.69\,\text{k}\Omega}{10.2\,\text{k}\Omega + 2.69\,\text{k}\Omega}$$

$$= 6.48$$

(d) *Voltage Gain*

$$A_V = \frac{V_o}{V_i} = \frac{-I_o R_L}{I_i Z_i}$$

$$= -A_I \cdot \frac{R_L}{Z_i} = -(6.42)\ \frac{10\,\text{k}\Omega}{2.13\,\text{k}\Omega}$$

$$= -30.14$$

$$A_{Vs} = A_V \cdot \frac{Z_i}{Z_i + R_s}$$

$$= (-30.14)\ \frac{2.13\,\text{k}\Omega}{2.13\,\text{k}\Omega + 1\,\text{k}\Omega}$$

$$= -20.51$$

Note: The same procedure can be used to analyze CC and CB amplifiers with R_L.

Exercise Problems

5.1 A CE fixed bias amplifier with by passed R_E has $R_C = 1.5$ kΩ, $R_B = 390$ kΩ, $R_E = 1.2$ kΩ, $h_{fe} = 120$ kΩ, $h_{ie} = 2$ kΩ, $h_{oe} = 20$ μS. Calculate Z_i, Z_o, A_V and A_I.

5.2 Repeat previous problem with unbypassed R_E.

5.3 An emitter follower using fixed bias has $R_B = 470$ kΩ, $R_E = 1$ kΩ, $h_{fe} = 120$ kΩ, $h_{ie} = 2$ kΩ and $h_{oe} = 20$ μS. Calculate Z_i, Z_o, A_V and A_I.

5.4 A CB configuration has $R_E = 1.5$ kΩ, $R_C = 2.2$ kΩ, $h_{ib} = 10$ kΩ, $h_{fb} = -0.996$ and $h_{ob} = 0.4$ μS. Calculate Z_i, Z_o, A_V and A_I.

5.5 Repeat Exercise 5.3, if $R_S = 1$ kΩ and $R_L = 10$ kΩ.

Chapter 6

FEEDBACK AMPLIFIERS

Negative feedback is used to stabilise the amplifier against variations in component values and parameters of the active devices used in the circuit. Negative feedback reduces distortion, reduces noise output, improves frequency response and improves input and output resistances. All these advantages are obtained at the cost of transfer gain. This chapter discusses the effect of negative feedback on various amplifier parameters. Analysis of practical feedback amplifiers has also been discussed.

6.1 CLASSIFICATION OF AMPLIFIERS

Amplifiers can be classified based on the magnitude of the input and output impedances as follows:

1. Voltage amplifiers
2. Current amplifiers
3. Transconductance amplifiers
4. Transresistance amplifiers

6.1.1 Voltage Amplifier

As the name implies, a voltage amplifier provides an output voltage proportional to the input voltage. Ideally, the proportionality constant is independent of the source and the load resistances. The equivalent circuit of the voltage amplifier is shown in Fig. 6.1.

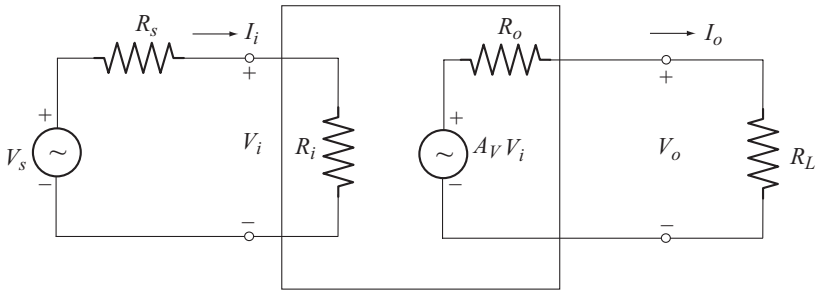


Fig. 6.1 Equivalent circuit of voltage amplifier

Observe in Fig. 6.1, that the voltage amplifier is driven by a voltage source V_s of internal resistance R_s. The output is represented by a voltage source $A_V V_i$ in series with output resistance R_o across which the load R_L is connected. R_i represents the input resistance of the amplifier.

Using voltage division rule at the input we have

$$V_i = \frac{V_s R_i}{R_s + R_i}$$

or

$$V_i = \frac{V_s}{1 + \left[\frac{R_s}{R_i}\right]} \tag{6.1}$$

It is desirable that the entire source voltage be available at the input terminals of the amplifier

i.e., $V_i \approx V_s$

From Equation (6.1) we find that, the above condition is satisfied if

$$\frac{R_s}{R_i} \ll 1$$

$$\Rightarrow \quad R_i \gg R_s \tag{6.2}$$

i.e., The voltage amplifier must be designed with very large input resistance. Ideally $R_i = \infty$.

Using voltage division rule at the output we have

$$V_o = \frac{A_V V_i R_L}{R_o + R_L}$$

or

$$V_o = \frac{A_V V_i}{1 + \left[\frac{R_o}{R_L}\right]} \tag{6.3}$$

It is desirable that the entire amplified voltage be available across the load

i.e., $V_o \approx A_V V_i$ (6.4)

From Equation (6.3) we find that , the above condition is satisfied if

$$\frac{R_o}{R_L} \ll 1$$

$$\Rightarrow \quad R_o \ll R_L \tag{6.5}$$

i.e., the voltage amplifier must be designed with very low output resistance. Ideally $R_o = 0$.

Now we conclude the following:

A good voltage amplifier must have a very large input resistance and a very low output resistance. Ideally $R_i = \infty$ and $R_o = 0$.

From Equation (6.4) we have

$$A_V = \frac{V_o}{V_i} \tag{6.6}$$

A_V is called the open loop voltage gain or voltage gain without feedback.

6.1.2 Current Amplifier

A current amplifier provides an output current proportional to the input current. Ideally, the proportionality constant is independent of the source and load resistances. The equivalent circuit of the current amplifier is shown in Fig. 6.2.

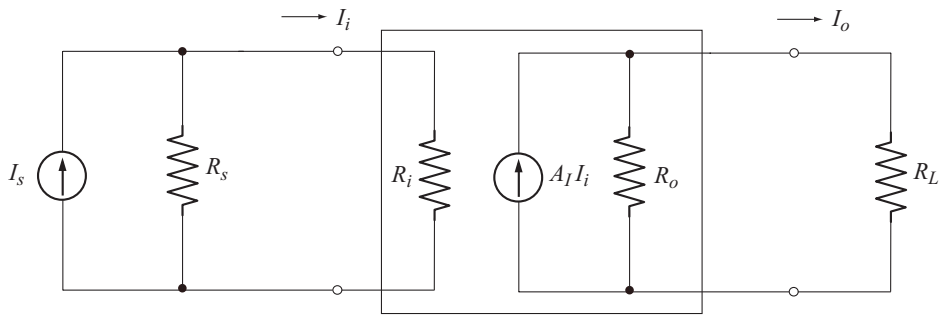


Fig. 6.2 Equivalent circuit of current amplifier

Observe that, the current amplifier is driven by a current source I_s of source resistance R_s. The output is also represented by a current source $A_I I_i$ in parallel with output resistance R_o. R_i represents the input resistance of the amplifier.

Using current division rule at the input we have

$$I_i = \frac{I_s R_s}{R_s + R_i}$$

$$I_i = \frac{I_s}{1 + \left[\frac{R_i}{R_s}\right]} \tag{6.7}$$

It is desirable to have the entire source current to flow into R_i

i.e., $$I_i \approx I_s$$

From Equation (6.7) we find that, the above condition is satisfied when

$$\frac{R_i}{R_s} \ll 1$$

$$\Rightarrow \quad R_i \ll R_s \tag{6.8}$$

i.e., The current amplifier must be designed with very low input resistance. Ideally $R_i = 0$.

Using current division rule at the output we have

$$I_o = \frac{A_I I_i R_o}{R_o + R_L}$$

or

$$I_o = \frac{A_I I_i}{1 + \frac{R_L}{R_o}} \tag{6.9}$$

It is desirable to have the entire amplified current to flow into R_L.

i.e., $$I_o \approx A_I I_i \tag{6.10}$$

From Equation (6.9) we find that, the above requirement is satisfied, when

$$\frac{R_L}{R_o} \ll 1$$

$$\Rightarrow \quad R_o \gg R_L \tag{6.11}$$

i.e., The current amplifier must be designed with very high output resistance. Ideally $R_o = \infty$.

Now we conclude the following:

A good current amplifier must have a very low input resistance and a very high output resistance. Ideally $R_i = 0$ and $R_o = \infty$.

From Equation (6.10) we have

$$A_I = \frac{I_o}{I_i} \tag{6.12}$$

A_I is called the open loop current gain or current gain without feedback.

6.1.3 Transconductance Amplifier

A transconductance amplifier provides an output current proportional to the input voltage. Ideally the proportionality constant is independent of the source and load resistances. Since, the output is a current and the input is a voltage, the proportionality constant has the unit of conductance and hence this arrangement is called a transconductance amplifier or voltage to current converter. The equivalent circuit of the transconductance amplifier is shown in Fig. 6.3.

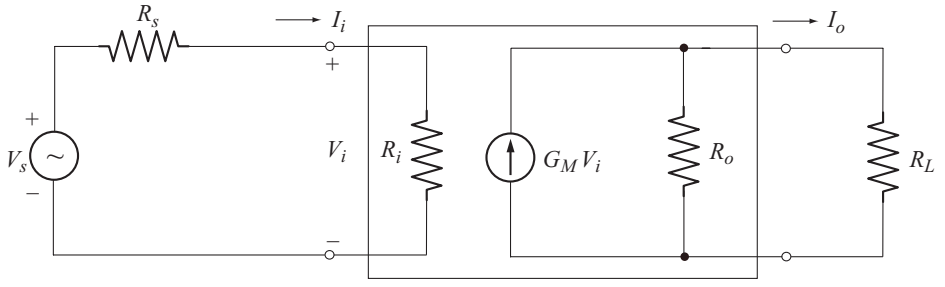


Fig. 6.3 Equivalent circuit of transconductance amplifier

Observe that, the amplifier is driven by a voltage source V_s of source resistance R_s. The output is represented by a current source $G_M V_i$ in parallel with output resistance R_o. R_i represents the input resistance of the amplifier.

Using voltage division rule at the input we have

$$V_i = \frac{V_s R_i}{R_s + R_i}$$

or

$$V_i = \frac{V_s}{1 + \left[\frac{R_s}{R_i}\right]} \tag{6.13}$$

It is desirable that the entire source voltage be available at the input terminals of the amplifier.

i.e., $$V_i \approx V_s$$

From Equation (6.13) we find that, the above requirement is met with if

$$\frac{R_s}{R_i} \ll 1$$

$$\Rightarrow \quad R_i \gg R_s \tag{6.14}$$

i.e., The transconductance amplifier must be designed with very high input resistance. Ideally $R_i = \infty$.

Using current division rule at the output we have

$$I_o = \frac{G_M V_i R_o}{R_o + R_L}$$

or

$$I_o = \frac{G_M V_i}{1 + \left[\frac{R_L}{R_o}\right]} \tag{6.15}$$

It is desirable that, the entire output current $G_M V_i$ to flow into R_L.

i.e., $$I_o \approx G_M V_i \tag{6.16}$$

From Equation (6.15) we find that, the above requirement is satisfied when

$$\frac{R_L}{R_o} \ll 1$$

$$\Rightarrow \quad R_o \gg R_L \tag{6.17}$$

i.e., The transconductance amplifier must be designed with very high output resistance. Ideally $R_o = \infty$.

Now we conclude the following:

A good transconductance amplifier must have very high input and output resistances. Ideally $R_i = \infty$ and $R_o = \infty$.

From Equation (6.16) we have

$$G_M = \frac{I_o}{V_i} \tag{6.18}$$

G_M is called the open loop transconductance or the transconductance without feedback.

6.1.4 Transresistance Amplifier

A transresistance amplifer provides an output voltage proportional to the input current. Ideally the proportionality constant is independent of the source and load resistances. Since the output is a voltage and the input is a current, the proportionality constant has the unit of resistance and hence this arrangement is called a transresistance amplifier or current to voltage converter. The equivalent circuit of the transresistance amplifier is shown in Fig. 6.4.

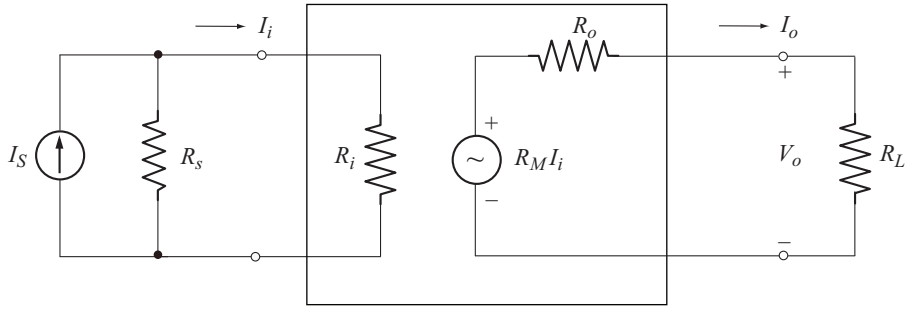


Fig. 6.4 Equivalent circuit of transresistance amplifier

Observe that, the amplifier is driven by a current source I_s of source resistance R_s. The output is represented by a voltage source $R_M\ I_i$ in series with output resistance R_o. R_i represents the input resistance of the amplifier.

Using current division rule at the input we have

$$I_i = \frac{I_s R_s}{R_s + R_i}$$

or

$$I_i = \frac{I_s}{1 + \dfrac{R_i}{R_s}} \tag{6.19}$$

It is desirable to have the entire source current to flow into R_i.

i.e., $$I_i \approx I_s$$

From Equation (6.19) we find that, the above requirement is met with when

$$\frac{R_i}{R_s} \ll 1$$

$$\Rightarrow \quad R_i \ll R_s \tag{6.20}$$

i.e., The transresistance amplifier must be designed with a very low input resistance. Ideally $R_i = 0$.

Using voltage division rule at the output we have

$$V_o = \frac{R_M I_i R_L}{R_o + R_L}$$

or
$$V_o = \frac{R_M I_i}{1 + \frac{R_o}{R_L}} \tag{6.21}$$

It is desirable that, the entire output voltage $R_M I_i$ be available across the load

i.e., $$V_o \approx R_M I_i \tag{6.22}$$

From Equation (6.21) we find that, the above requirement is satisfied when

$$\frac{R_o}{R_L} \ll 1$$

$$\Rightarrow \quad R_o \ll R_L \tag{6.23}$$

i.e., The transresistance amplifier must be designed with very low output resistance. Ideally $R_o = 0$.

Now we conclude the following:

A good transresistance amplifier must have very low input and output resistances. Ideally $R_i = 0$ and $R_o = 0$.

From Equation (6.22) we have

$$R_M = \frac{V_o}{I_i} \tag{6.24}$$

R_M is called the open loop transresistance or the transresistance without feedback.

The results are summarised in Table 6.1 for ideal amplifiers.

Table 6.1 Summary of ideal amplifier characteristics

Parameter	*Voltage amplifier*	*Current amplifier*	*Transconductance amplifier*	*Transresistance amplifier*
Input resistance R_i	∞	0	∞	0
Output resistance R_o	0	∞	∞	0

6.2 FEEDBACK CONCEPT

Several characteristics of the amplifier such as input resistance, output resistance, linearity and band width can be improved by incorporating negative feedback. This can be achieved by feeding

back a part of the output into the input. Such amplifiers are called *feedback amplifier*s. The block diagram of a typical feedback amplifier is shown in Fig. 6.5.

The basic configuration consists of five blocks as shown in Fig. 6.5.

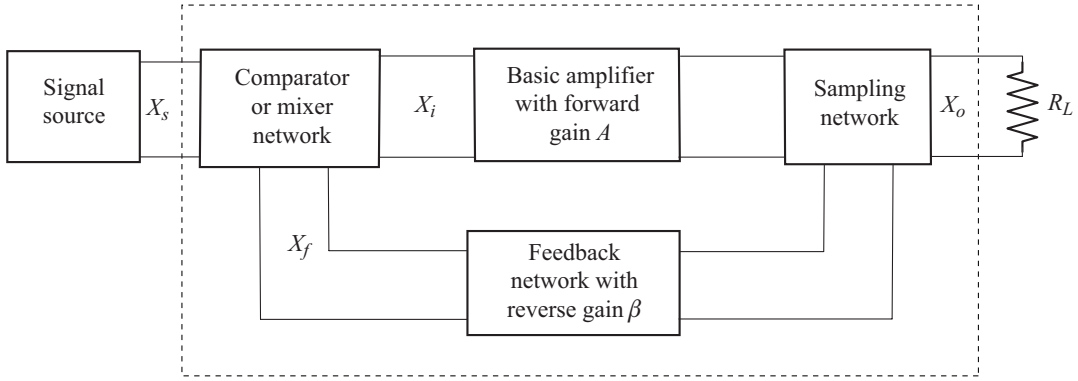


Fig. 6.5 Block diagram of a typical feedback amplifier
X_s : Signal source
X_f : Feedback signal
X_i : Input signal to the basic amplifier
X_o : Output signal

Signal Source Block

The signal source is either a voltage source or a current source depending on the type of amplifier as classified in Section 6.1. A voltage source is represented by a signal source V_s in series with a source resistance R_s, commonly known as Thevenin's representation. A current source is represented by a signal source I_s in parallel with a source resistance R_s, commonly known as Norton's representation. These representations are shown in Fig. 6.6.

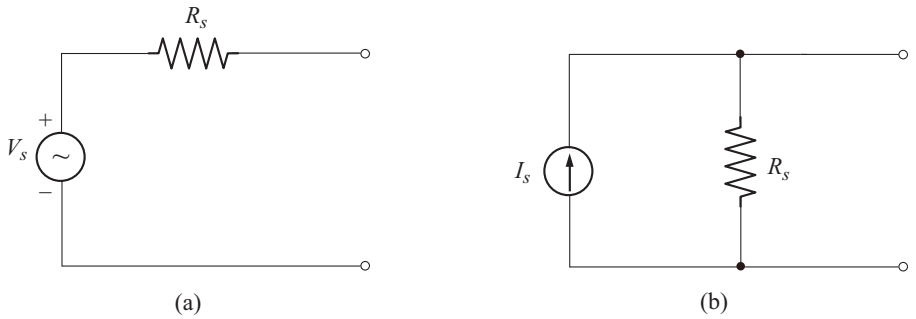


Fig. 6.6 Signal source representation
(a) Thevenin's representation of voltage source
(b) Norton's representation of current sourcce

Comparator or Mixing Block

This block essentially combines the source signal with the feedback signal. The output of the mixer is $X_i = X_s - X_f$. Depending upon the nature of the signal source and the feedback signal there could be either series mixing or shunt mixing. When the source and the feedback signals are both voltages, series mixing is used. If these are both currents, shunt mixing is used. The type of mixing is independent of the output signal being sampled to be feedback.

For instance, an output voltage could be sampled and fedback as an input current or an output current could be sampled and fedback as an input voltage. For example, in the transconductance amplifier, the input is a voltage, whereas the output is a current. Obviously, since the input is a voltage source, only series mixing is possible. Thus, the sampled output current must be converted to a voltage to facilitate series mixing. The schemes for series mixing and shunt mixing are shown in Fig. 6.7.

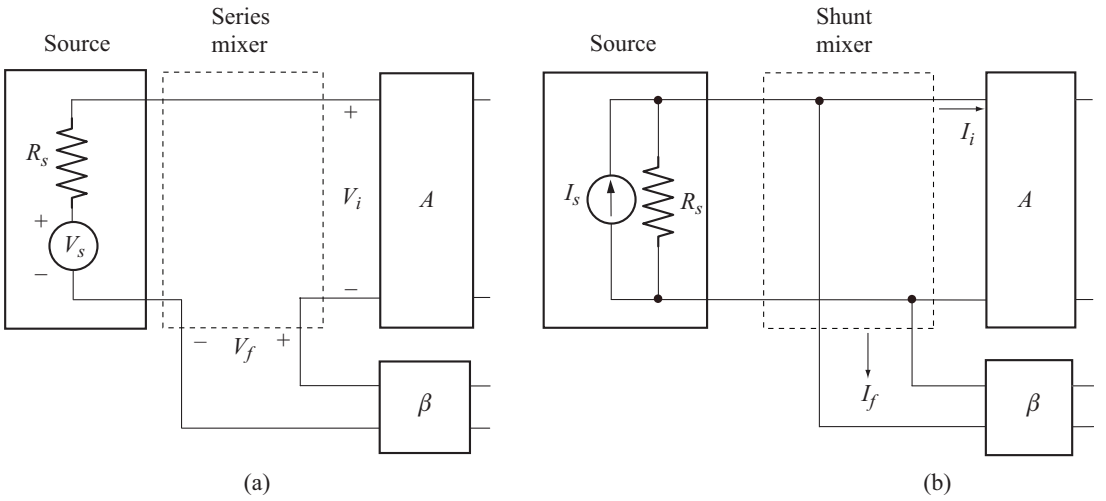


Fig. 6.7 Mixer Block
(a) Series Mixing
(b) Shunt Mixing

Basic Amplifier Block

The basic amplifier block is shown in Fig. 6.8.

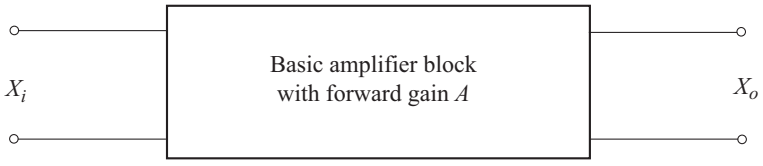


Fig. 6.8 Basic amplifier block

The ratio of the output signal to the input signal of the basic amplifier is represented by A and it is called the transfer gain without feedback or open loop transfer gain or simply open loop gain. It is given by

$$A = \frac{X_o}{X_i} \tag{6.25}$$

A depends on the type of amplifier the block represents.

If it represents a voltage amplifier, then

$$X_i = V_i \quad \text{and} \quad X_o = V_o$$

$$\therefore \quad A = A_V = \frac{V_o}{V_i} \tag{6.26}$$

If the block represents a current amplifier, then

$$X_i = I_i \quad \text{and} \quad X_o = I_o$$

$$A = A_I = \frac{I_o}{I_i} \tag{6.27}$$

Finally if the block represents a transconductance amplifier, then

$$X_i = V_i \quad \text{and} \quad X_o = I_o$$

$$A = G_M = \frac{I_o}{V_i} \tag{6.28}$$

Finally if the block represents a transresistance amplifier, then

$$X_i = I_i \quad \text{and} \quad X_o = V_o$$

$$A = R_M = \frac{V_o}{I_i} \tag{6.29}$$

Though G_M and R_M are not strictly amplifications since the units of output and input are not the same, the quantities A_V, A_I, G_M and R_M are referred to as the transfer gain of the basic amplifier without taking any feedback into consideration. Thus, A represents one of the quantities A_V, A_I, G_M or R_M depending on the type of transfer.

A_f refers to the transfer gain of the amplifier with feedback. A_f is defined as the ratio of the output signal of the amplifier to its input signal. With reference to Fig. 6.5,

$$A_f = \frac{X_o}{X_s} \tag{6.30}$$

for a basic voltage amplifier,

$$A_{Vf} = \frac{V_o}{V_s} \tag{6.31}$$

for a basic current amplifier,

$$A_{If} = \frac{I_o}{I_s} \tag{6.32}$$

for a basic transconductance amplifier,

$$G_{Mf} = \frac{I_o}{V_s} \tag{6.33}$$

while for a basic transresistance amplifier,

$$R_{Mf} = \frac{V_o}{I_s} \tag{6.34}$$

Sampling Network

It is used to sample the output signal of the basic amplifier. The feedback network is connected in parallel with the output terminals when voltage is to be sampled as shown in Fig. 6.9(a). The feedback network is connected in series with the output terminals when current is to be sampled as shown in Fig. 6.9 (b).

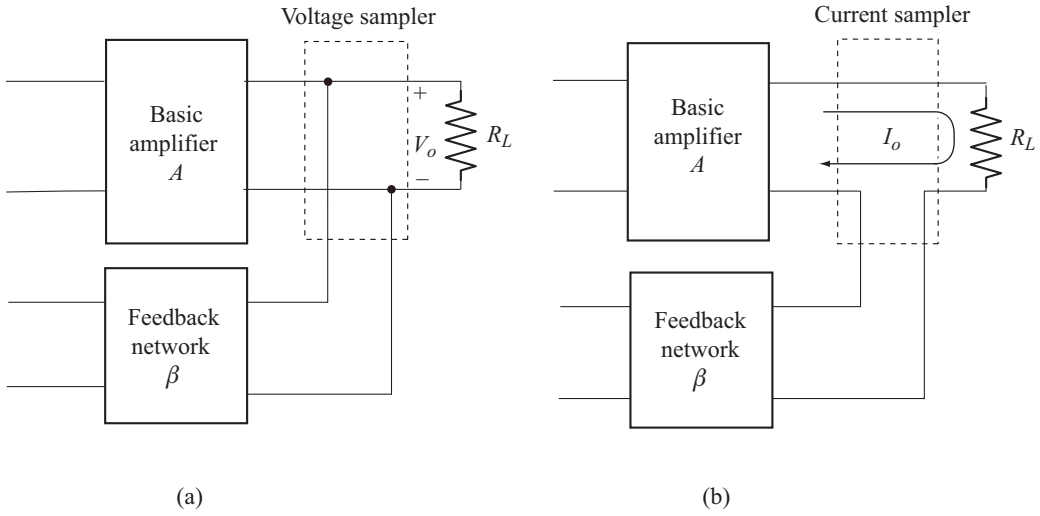


Fig. 6.9 Sampling network
(a) Voltage sampling (b) Current sampling

Feedback Network

This is a passive two-port network configured using passive elements such as resistors, inductors and capacitors. More often, the feedback network is simply a resistive network.

The ratio of the output signal to the input signal of the feedback network is called the feedback factor β.

Feedback factor, $$\beta = \frac{X_f}{X_o}.$$

Consider the example of sampling a voltage and feeding it back in series.

The feedback signal can be derived from the output voltage by means of a simple voltage divider network as shown in Fig. 6.10.

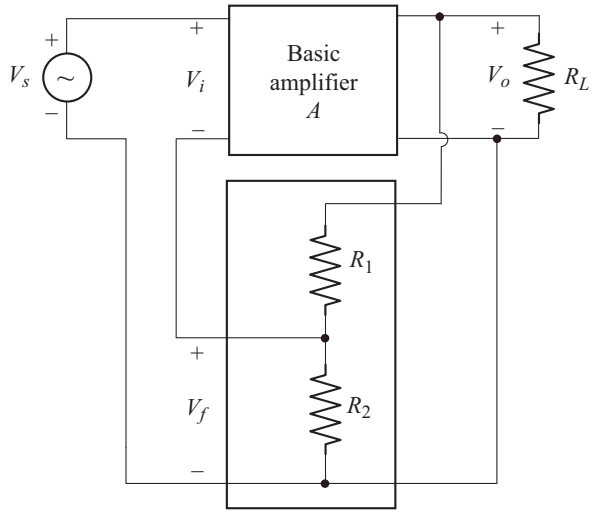


Fig. 6.10 Voltage-sampling and series mixing configuration

The feedback signal or output voltage of the feedback network in Fig. 6.10 is given by

$$V_f = \frac{R_2}{R_1 + R_2} V_o \tag{6.35}$$

$$\therefore \quad \frac{V_f}{V_s} = \frac{R_2}{R_1 + R_2} \tag{6.36}$$

By definition

$$\beta = \frac{V_f}{V_s} = \frac{R_2}{R_1 + R_2} \tag{6.37}$$

Observe that β does not have units in this case. This is not always true, for instance when voltage is sampled and current is derived from the feedback network, the feedback network has the unit of *mhos* or *siemens.*

◆ 6.3 TRANSFER GAIN OF SINGLE LOOP FEEDBACK AMPLIFIER

Let us now, obtain the transfer gain of the feedback amplifier. The block schematic of a single loop feedback amplifier is shown in Fig. 6.11.

In Fig. 6.11 X_S, X_d, X_i, X_o and X_f represent general amplifier signals which may be either voltages or currents depending on the circuit.

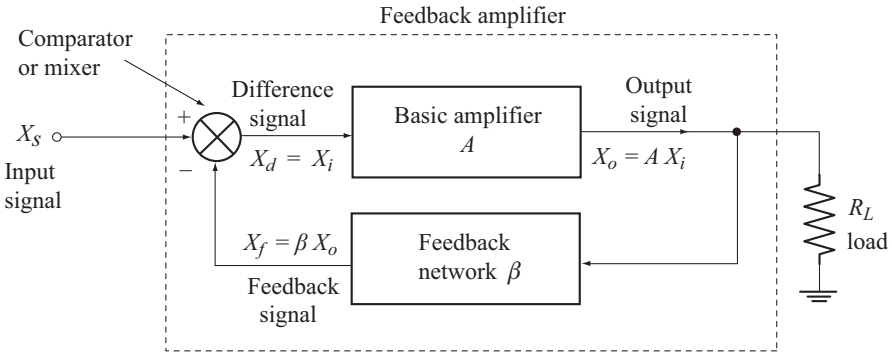


Fig. 6.11 Single-loop feedback amplifier

The transfer gain of the basic amplifier without feedback is given by

$$A = \frac{X_o}{X_i} \tag{6.38}$$

The transfer gain of the feedback amplifier is given by

$$A_f = \frac{X_o}{X_S} \tag{6.39}$$

$$X_o = A X_i \tag{6.40}$$

and $$X_i = X_s - X_f \tag{6.41}$$

where, $$X_f = \beta X_o \tag{6.42}$$

Using these relations in Equation (6.40) we have

$$X_o = A(X_s - X_f) = A(X_s - \beta X_o)$$

$$X_o = A X_s - A \beta X_o$$

$$A X_s = X_o(1 + A\beta)$$

$$\therefore \quad A_f = \frac{X_o}{X_S} = \frac{A}{1 + A\beta} \tag{6.43}$$

Magnitude of the transfer gain is

$$|A_f| = \frac{|A|}{|1 + A\beta|} \tag{6.44}$$

Consider Equation (6.44) :

- If $|1 + A\beta| > 1$, then

  $$|A_f| < |A|$$

  the feedback is termed negative or degenerative.

- If $|1 + A\beta| < 1$, then

$$|A_f| > |A|$$

the feedback is termed positive or regenerative.

6.4 LOOP GAIN

Let us now trace the path of X_i through the feedback loop in Fig. 6.11. The signal X_i gets,

- Multiplied by A in the basic amplifier,
- Multiplied by β in the feedback network,
- Multiplied by –1 in the mixer.

Hence, the loop gain or return ratio is $-A\beta$.

Subtracting the loop gain from unity, we get the return difference defined by

$$D = 1 + A\beta \tag{6.45}$$

Using this relation in Equation 6.44 we get

$$|A_f| = \frac{|A|}{|D|} \tag{6.46}$$

Gain with feedback in decibels is

$$20 \log_{10}|A_f| = 20 \log_{10}|A| - 20 \log_{10}|D| \tag{6.47}$$

$$\text{or} \quad 20 \log_{10}|A| = 20 \log_{10}|A_f| + 20 \log_{10}|D| \tag{6.48}$$

This means that in decibels,

Gain with out feedback = gain with feedback + gain lost due to negative feedback. (6.49)

Thus for instance, a loss of 10 dB gain due to negative feedback is because of the 10 dB feedback negatively in the amplifier.

The amount of feedback in dB = – gain lost due to negative feedback

Let N be the feedback in dB

$$\therefore \quad N = -20 \log_{10}|D|$$

$$= 20 \log_{10} \frac{1}{|D|} \tag{6.50}$$

Substituting for D from Equation 6.46

$$N = -20 \log_{10} \left| \frac{A_f}{A} \right| \tag{6.51}$$

$$\text{or} \quad N = -20 \log_{10} \frac{1}{|1 + A\beta|} \tag{6.52}$$

Example 6.1

A feedback amplifier has a gain of 1000 without feedback. Find the gain with feedback and the amount of feedback in dB for a negative feedback of 10%.

Solution

$$A = 1000$$
$$\%\beta = 10\% \Rightarrow \beta = 0.1$$

From Equation (6.45)

$$D = 1 + A\beta = 1+1000 \times 0.1 = 101$$

From Equation (6.46)

$$|A_f| = \frac{|A|}{|D|} = \frac{1000}{101} = 9.9$$

From Equation (6.52)

$$N = 20 \log_{10}\left[\frac{1}{101}\right]$$
$$N = -40 \text{ dB} \quad \text{(A)}$$

Gain in dB without feedback is

$$20 \log_{10}|A| = 20 \log_{10}[1000] = 60 \text{ dB} \quad \text{(B)}$$

Gain in dB with feedback is

$$20 \log_{10}|A_f| = 20 \log_{10}[9.9] = 20 \text{ dB} \quad \text{(C)}$$

Observe that the negative feedback of 40 *dB [Equation (A)] has caused the gain to drop from* 60 *dB to* 20 *d*B [*Equation (C)].

◆ 6.5 ASSUMPTIONS IN THE ANALYSIS OF FEEDBACK AMPLIFIERS

Three conditions are to be assumed to simplify the analysis of feedback amplifiers.

Condition 1: The input signal is transmitted to the output only through the forward basic amplifier and not through the feedback network. Thus, if the amplifier is deactivated, the output signal should be zero.

Condition 2: The feedback signal is transmitted from the output to the input only through the feedback network and not through the amplifier.

Condition 3: The feedback factor β is independent of load and source resistances. This can be ensured by proper choice of the elements of the feedback network.

◆ 6.6 FEEDBACK AMPLIFIER TOPOLOGIES

We saw in section 6.2 that there could be two types of sampling, either voltage sampling or current sampling independent of the type of mixing. With each type of sampling there could be either series mixing or shunt mixing. This gives rise to four feedback topologies as shown in Table 6.2.

Table 6.2 Feedback amplifier topologies

Sampling	*Mixing*	*Topology*
Voltage	Shunt	Voltage-shunt feedback
Voltage	Series	Voltage-series feedback
Current	Shunt	Current-shunt feedback
Current	Series	Current-series feedback

6.6.1 Voltage-series Feedback Amplifier

Here the output voltage is sampled and the mixing is of series type. For series mixing both source signal and the feedback signal must be voltages. Hence the basic amplifier is a voltage amplifier. Figure 6.12 shows the block diagram of voltage-series feedback amplifier.

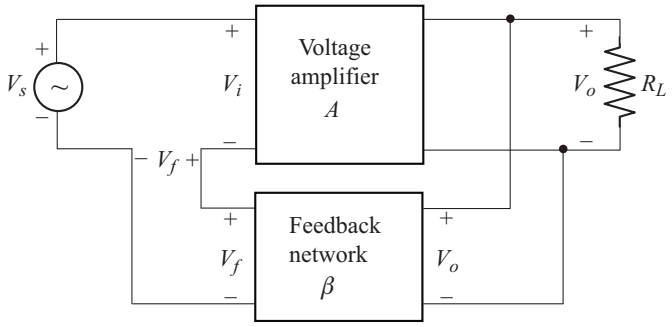


Fig. 6.12 Voltage-series feedback topology

Transfer gain without feedback

$$A = \frac{V_o}{V_i} \tag{6.53}$$

Transfer gain with feedback

$$A_f = \frac{V_o}{V_s} \tag{6.54}$$

It is important to note that

$$A = A_V \tag{6.55}$$

and

$$A_f = A_{Vf} \tag{6.56}$$

A_{Vf} is the closed loop voltage gain or voltage gain with negative feedback.

Feedback network converts output voltage into feedback voltage. Hence feedback factor is given by

$$\beta = \frac{V_f}{V_o} \tag{6.57}$$

$$\Rightarrow \quad V_f = \beta V_o \tag{6.58}$$

6.6.2 Voltage-shunt Feedback Amplifier

Here the output voltage is sampled and the mixing is of shunt type. For shunt mixing both source signal and the feedback signal must be currents. Hence the basic amplifier is a transresistance amplifier. Figure 6.13 shows the block diagram of voltage-shunt feedback amplifier.

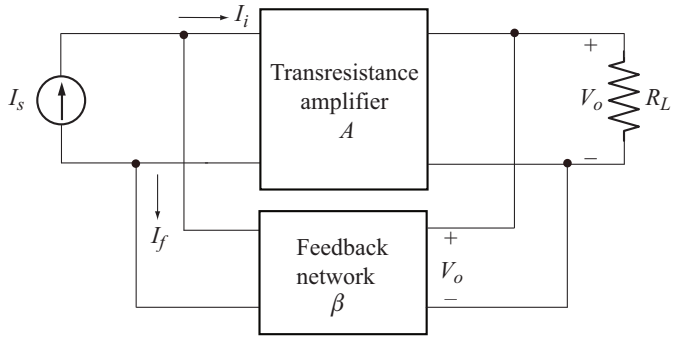


Fig. 6.13 Voltage-shunt feedback topology

Transfer gain without feedback

$$A = \frac{V_o}{I_i} \tag{6.59}$$

Transfer gain with feedback

$$A_f = \frac{V_o}{I_s} \tag{6.60}$$

It is important to note that

$$A = R_M \tag{6.61}$$

and

$$A_f = R_{Mf} \tag{6.62}$$

R_{Mf} is the closed loop transresistance or transresistance with negative feedback.

Feedback network converts output voltage into feedback current. Hence feedback factor is given by

$$\beta = \frac{I_f}{V_o} \tag{6.63}$$

$$\Rightarrow \quad I_f = \beta V_o \tag{6.64}$$

6.6.3 Current-shunt Feedback Amplifier

Here the output current is sampled and the mixing is of shunt type. For shunt mixing both source signal and the feedback signal must be currents. Hence the basic amplifier is a current amplifier. Figure 6.14 shows the block diagram of current-shunt feedback amplifier.

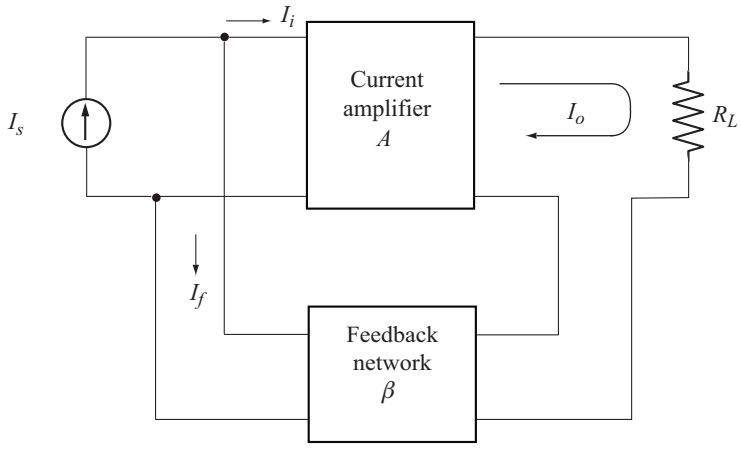


Fig. 6.14 Current-shunt feedback topology

Transfer gain without feedback $$A = \frac{I_o}{I_i} \tag{6.65}$$

Transfer gain with feedback $$A_f = \frac{I_o}{I_s} \tag{6.66}$$

It is important to note that

$$A = A_I \tag{6.67}$$

and $$A_f = A_{If} \tag{6.68}$$

A_{If} is the closed loop current gain or current gain with negative feedback.

Feedback network converts output current into feedback current. Hence the feedback factor is given by

$$\beta = \frac{I_f}{I_o} \tag{6.69}$$

$$\Rightarrow \quad I_f = \beta I_o \tag{6.70}$$

6.6.4 Current-series Feedback Amplifier

Here the output current is sampled and the mixing is of series type. For series mixing both source signal and the feedback signal must be voltages. Hence the basic amplifier is a transconductance amplifier. Figure 6.15 shows the block diagram of current-series feedback amplifier.

Transfer gain without feedback $$A = \frac{I_o}{V_i} \tag{6.71}$$

Transfer gain with feedback $$A_f = \frac{I_o}{V_s} \tag{6.72}$$

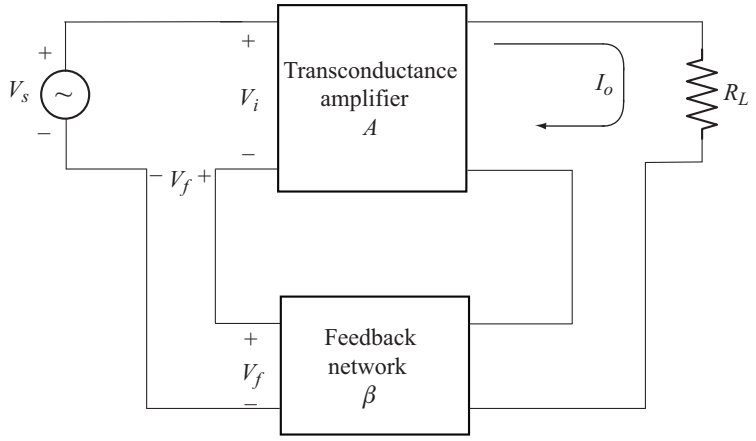


Fig. 6.15 Current-series feedback topology

It is important to note that

$$A = G_M \tag{6.73}$$

and

$$A_f = G_{Mf} \tag{6.74}$$

G_{Mf} is the closed loop transconductance or transconductance with negative feedback.

Feedback network converts output current in to feedback voltage. Hence the feedback factor is given by

$$\beta = \frac{V_f}{I_o} \tag{6.75}$$

$$\Rightarrow \quad V_f = \beta I_o \tag{6.76}$$

Note: While writing the block diagrams of feedback topologies, sources are considered to be ideal. Hence R_s is not shown.

6.6.5 Summary of Feedback Amplifier Topologies

Table 6.3 summarises the feedback amplifier topologies.

Table 6.3 Summary of feedback amplifier topologies

Parameter	*Feedback topologies*			
	Voltage series	*Voltage shunt*	*Current series*	*Current shunt*
Reference	Fig. 6.12	Fig. 6.13	Fig. 6.15	Fig. 6.14
X_o	Voltage	Voltage	Current	Current
X_s, X_f	Voltage	Current	Voltage	Current
A	$A_V = \frac{V_o}{V_i}$	$R_M = \frac{V_o}{I_i}$	$G_M = \frac{I_o}{V_i}$	$A_I = \frac{I_o}{I_i}$

Parameter	Feedback topologies			
	Voltage series	Voltage shunt	Current series	Current shunt
A_f	$A_{Vf} = \frac{V_o}{V_s}$	$R_{Mf} = \frac{V_o}{I_s}$	$G_{Mf} = \frac{I_o}{V_s}$	$A_{If} = \frac{I_o}{I_s}$
β	$\frac{V_f}{V_o}$	$\frac{I_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$

Example 6.2

Using the block diagram of voltage series feedback amplifier, derive the expression for its transfer gain with feedback.

Solution

Refer Fig. 6.12

From Equation (6.53), $V_o = A V_i$ (A)

Applying KVL to the input circuit we have

$$V_s - V_i - V_f = 0$$

or $$V_i = V_s - V_f \quad \text{(B)}$$

Using Equation (B) in Equation (A) we have

$$V_o = A [V_s - V_f]$$

$$= AV_s - AV_f \quad \text{(C)}$$

But $V_f = \beta V_o$ [From Equation 6.58]

Now $V_o = AV_s - A\beta V_o$

$$V_o [1 + A\beta] = A V_s$$

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A} \quad \text{(D)}$$

For voltage series feedback amplifier

$$A = A_V \quad \text{and} \quad A_f = A_{Vf}$$

Now Equation (D) can also be written as

$$A_{Vf} = \frac{A_V}{1 + \beta A_V} \quad \text{(E)}$$

Example 6.3

Using the block diagram of voltage shunt feedback amplifier, derive the expression for its transfer gain with feedback.

Solution

Refer Fig. 6.13

From Equation (6.59), $V_o = A\, I_i$ (A)

Applying KCL at the input circuit we have

$$I_s = I_i + I_f$$

or $$I_i = I_s - I_f \quad \text{(B)}$$

Using Equation (B) in Equation (A) we have

$$V_o = A\,[\,I_s - I_f\,]$$

$$= A\, I_s - A\, I_f \quad \text{(C)}$$

But $I_f = \beta\, V_o$ [From Equation 6.64]

Now $V_o = A\, I_s - A\,\beta\, V_o$

$$V_o\,[\,1 + A\,\beta\,] = A\, I_s$$

$$A_f = \frac{V_o}{I_s} = \frac{A}{1 + A\,\beta} \quad \text{(D)}$$

For voltage shunt feedback amplifier

$$A = R_M \text{ and } A_f = R_{Mf}$$

Now Equation (D) can also be written as

$$R_{Mf} = \frac{R_M}{1 + \beta\, R_M} \quad \text{(E)}$$

Note: Similarly we can derive the expressions for A_f of current series and current shunt feedback amplifiers using the block diagrams given in Fig. 6.15 and Fig. 6.14 respectively.

◆ 6.7 GENERAL CHARACTERISTICS OF NEGATIVE FEEDBACK AMPLIFIER

Though negative feedback reduces the transfer gain it is extensively used in amplifiers. The reason is that with negative feedback, many desirable characteristics are obtained. Now let us examine these desirable characteristics in detail.

6.7.1 Stability of Transfer Gain

Transfer gain with feedback is given by

$$A_f = \frac{A}{1 + \beta\, A} \quad (6.77)$$

Differentiating with respect to A, we have

$$\frac{dA_f}{dA} = \frac{\left[1 + \beta\, A\right] - A\left[\beta\right]}{\left[1 + \beta\, A\right]^2}$$

$$= \frac{1}{\left[1+\beta A\right]^2}$$

$$= \frac{1}{\left[1+\beta A\right]} \cdot \frac{1}{\left[1+\beta A\right]} \tag{6.78}$$

From Equation (6.77) we have

$$\frac{1}{1+\beta A} = \frac{A_f}{A}$$

Using this relation in Equation (6.78) we have

$$\frac{dA_f}{dA} = \frac{A_f}{A} \frac{1}{1+\beta A}$$

$$\frac{dA_f}{dA} = \frac{\left[\frac{dA}{A}\right]}{\left[1+\beta A\right]}$$

$$\left|\frac{dA_f}{A_f}\right| = \frac{\left|\frac{dA}{A}\right|}{|1+\beta A|} \tag{6.79}$$

$\left|\frac{dA_f}{A_f}\right|$ = relative change in gain with feedback

$\left|\frac{dA}{A}\right|$ = relative change in gain without feedback

For negative feedback, $|1 + \beta A| > 1$
Now from Equation (6.79) we get

$$\left|\frac{dA_f}{A_f}\right| < \left|\frac{dA}{A}\right| \tag{6.80}$$

or stated in words:

Relative change in gain with feedback is less than that without feedback. This implies that with negative feedback, the transfer gain changes very little or negative feedback stabilises the transfer gain.

Desensitivity factor

From Equation (6.79) we find that the variation in transfer gain or the sensitivity of transfer gain gets reduced by a factor $D = 1 + \beta A$. For this reason, D is also called the Desensitivity factor.

Example 6.4

An amplifier without feedback has a transfer gain of – 2000. The transfer gain changes by 20% due to temperature. If negative feedback with $\beta = -0.1$ is given, calculate the change in gain of the feedback amplifier.

Solution

$$A = -2000 \quad \beta = -0.1$$

$$\% \left|\frac{dA}{A}\right| = 20\%$$

$$1 + \beta A = 1 + (-0.1)(-2000)$$

$$= 201$$

From Equation (6.79)

$$\% \left|\frac{dA_f}{A_f}\right| = \frac{\% \left|\frac{dA}{A}\right|}{1 + \beta A}$$

$$= \frac{20\%}{201} = 0.099\%$$

Example 6.5

Calculate the gain of a negative-feedback amplifier having $A = -2000$, if the feedback factor is 20 %.

Solution

$$A = -2000$$

$$\% \ \beta = 20\ \%$$

$$\Rightarrow \quad \beta = 0.2$$

For negative feedback, $A\beta$ is positive. Therefore we take

$$\beta = -0.2$$

$$1 + \beta A = 1 + (-0.2)(-2000)$$

$$= 401$$

$$A_f = \frac{A}{1 + \beta A}$$

$$= \frac{-2000}{401} = -4.98$$

6.7.2 Reduction in Non-linear Distortion

The transfer charecterstics of a practical amplifier is non-linear as shown in Fig. 6.16.

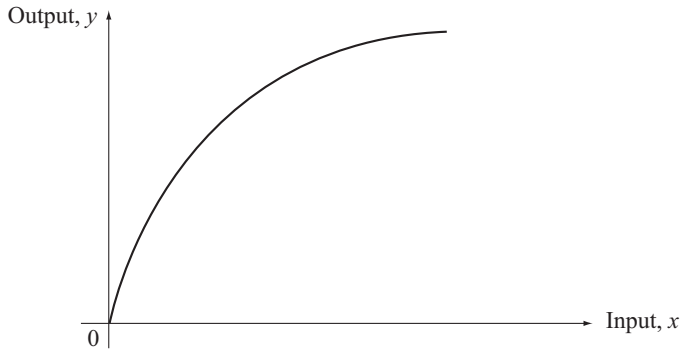


Fig. 6.16 Transfer charecteristics of practical amplifier

Since, the transfer charecteristics is non-linear, the input-output relationship can be expressed as

$$y = k_1 x + k_2 x^2 + k_3 x^3 + \cdots \tag{6.81}$$

where the first term represents the linear term followed by the non-linear terms. For instance, if the input is sinusoidal of large amplitude, say

$$x = A_o \sin \omega t \tag{6.82}$$

Then, Equation (6.81) becomes

$$y = k_1 A_o \sin \omega t + k_2 A_o^2 \sin^2 \omega t + k_3 A_o^3 \sin^3 \omega t + \cdots$$

which can be expressed in the general form as

$$y = B_o + B_1 \sin \omega t + B_2 \sin 2\omega t + B_3 \sin 3\omega t + \cdots \tag{6.83}$$

where B_o is the dc term, B_1 is the amplitude of the fundamental, B_2 is the amplitude of the second harmonic and so on.

Equation 6.83 indicates that y is not an exact replace of x, but is distorted, referred to as harmonic distortion or non-linear distortion. It can be shown from Fourier analysis that as the order of the harmonic increases, its amplitude decreases.

$$\text{i.e.,} \qquad |B_1| > |B_2| > |B_3| > \cdots \tag{6.84}$$

To study the effect of negative feedback on harmonic distortion, let us assume that only second harmonic distortion is present. Let B_{2f} be the second harmonic distortion at the output in the presence of negative feedback.

When B_{2f} is sampled it gets

- Multiplied by β in the feedback network
- Multiplied by -1 in the mixer
- Multiplied by A in the basic amplifier

Finally it becomes $-A\beta B_{2f}$

Hence, the second harmonic component at the output in the presence of negative feedback is

$$B_{2f} = B_2 - A\beta B_{2f}$$

$$B_{2f}(1 + A\beta) = B_2$$

$$\therefore \quad B_{2f} = \frac{B_2}{1 + A\beta} = \frac{B_2}{D} \tag{6.85}$$

$$\text{or} \quad \left| B_{2f} \right| = \frac{|B_2|}{|1 + A\beta|} = \frac{|B_2|}{|D|} \tag{6.86}$$

We know that for negative feedback

$$|1 + A\beta| > 1 \quad \text{and hence} \quad |B_{2f}| < |B_2|$$

Observe that the second-harmonic distortion gets reduced by a factor $|1 + A\beta|$.

6.7.3 Reduction of Noise

Let N represents the output noise without feedback and let N_f represents the output noise with feedback. When N_f is sampled, it gets multiplied by $-A\beta$ around the feedback loop and becomes $-A\beta N_f$.

Thus, the noise at the output in the presence of negative feedback is

$$N_f = N - A\beta N_f$$

$$\text{or} \quad N_f = \frac{N}{1 + A\beta} = \frac{N}{D} \tag{6.87}$$

$$\text{or} \quad |N_f| = \frac{|\mathrm{N}|}{|1 + A\beta|} = \frac{|N|}{|D|} \tag{6.88}$$

Equation (6.88) shows that the output noise reduces by a factor of $|1 + A\beta|$ in the presence of negative feedback since $|1 + A\beta| > 1$.

6.7.4 Reduction in Frequency Distortion

The gain of an amplifier becomes a function of frequency due to internal device capacitances, associated coupling and bypass elements such as capacitors and transformers. As a result, different frequency components are amplified to different extents.

We have seen that the gain of an amplifier with negative feedback is given by

$$A_f = \frac{A}{1 + A\beta}$$

If $|A\beta| >> 1$, then

$$A_f \approx \frac{A}{A\beta}$$

$$\therefore \quad A_f = \frac{1}{\beta} \tag{6.89}$$

Under this condition, A_f depends only on β. In most of the circuits, β network contains only resistors and therefore the feedback factor β is independent of frequency. As a result, A_f becomes independent of frequency. Thus negative feedback reduces frequency distortion.

6.8 EFFECT OF NEGATIVE FEEDBACK ON INPUT RESISTANCE

The effect of negative feedback on input resistance depends on the nature of mixing.

In case of series mixing the input resistance increases while in the case of shunt mixing the input resistance decreases.

Let us now see how series mixing increases the input resistance. The input stage of a feedback amplifier with series mixing is shown in Fig. 6.17.

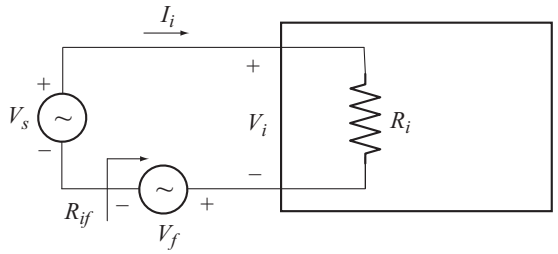


Fig. 6.17 Input stage of feedback amplifier with series mixing

From Fig. 6.17 the input resistance without feedback is given by

$$R_i = \frac{V_i}{I_i} \tag{6.90}$$

While the input resistance with feedback R_{if} is given by

$$R_{if} = \frac{V_s}{I_i} \tag{6.91}$$

In the presence of negative feedback V_f is in opposite polarity with respect to V_s and hence I_i with negative feedback is less than that without feedback. As a result R_{if} is greater than R_i.

Now, let us look at the situation in case of shunt mixing. The input stage of a feedback amplifier with shunt mixing is shown in Fig. 6.18.

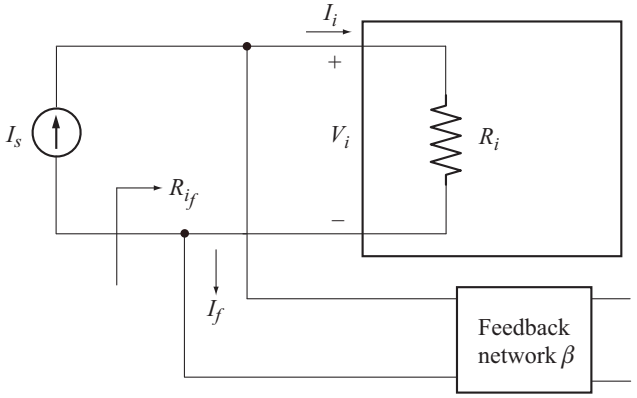


Fig. 6.18 Input stage of feedback amplifier with shunt mixing

Observe that the feedback network appears in parallel with the input terminals of the amplifier. From Fig. 6.18 input resistance without feedback is

$$R_i = \frac{V_i}{I_i} \tag{6.92}$$

and in the presence of negative feedback, the input resistance is

$$R_{if} = \frac{V_i}{I_s} \tag{6.93}$$

But $$I_s = I_i + I_f$$

$$R_{if} = \frac{V_i}{I_i + I_f} \tag{6.94}$$

From Equations (6.92) and (6.94) it is clear that $R_{if} < R_i$.

6.8.1 Input Resistance of Voltage-series Feedback Amplifier

We now obtain an expression for R_{if} for the voltage-series feedback amplifier. Figure 6.19 shows a typical voltage-series feedback circuit.

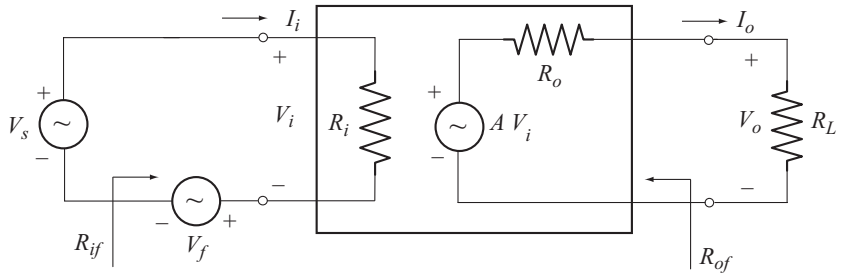


Fig. 6.19 Voltage series feedback amplifier

$R_i = \dfrac{V_i}{I_i}$ = Input resistance without feedback

$R_{if} = \dfrac{V_s}{I_i}$ = Input resistance with feedback.

Applying KVL to the input circuit of Fig. 6.19, we have

$$V_s - V_i - V_f = 0 \tag{6.95}$$

But $$V_i = I_i R_i \text{ and } V_f = \beta V_o$$

Substituting these relations in Equation 6.95 we have

$$V_s - I_i R_i - \beta V_o = 0 \tag{6.96}$$

But $$V_o = A V_i = A I_i R_i$$

Using this relation in Equation (6.96) we have

$$V_s - I_i R_i - \beta A\ I_i R_i = 0$$

$$V_s = I_i R_i [1 + \beta A]$$

$$\text{Now} \qquad R_{if} = \frac{V_s}{I_i} = R_i [1 + \beta A] \tag{6.97}$$

$$\text{Since} \quad [1 + \beta A] > 1$$

$$R_{if} > R_i$$

Note that the input resistance increases by a factor $1 + \beta A$ as expected for series mixing.

6.8.2 Input Resistance of Voltage-shunt Feedback Amplifier

The input resistance can be computed from the voltage-series feedback circuit shown in Fig. 6.20.

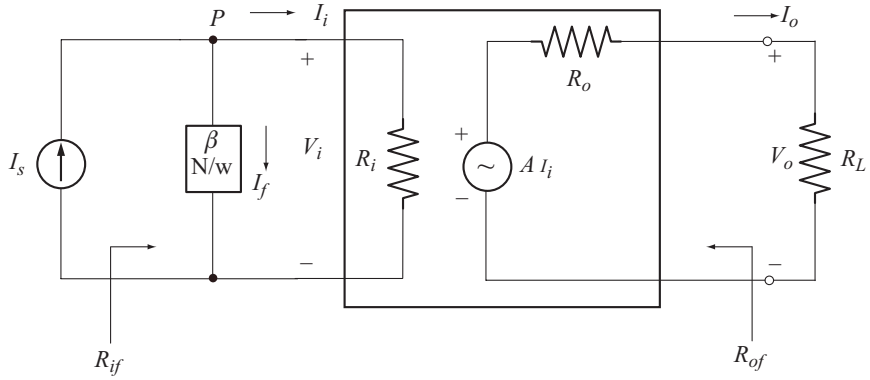


Fig. 6.20 Voltage – shunt feedback amplifier

$$R_i = \frac{V_i}{I_i} = \text{Input resistance without feedback}$$

$$R_{if} = \frac{V_i}{I_s} = \text{Input resistance with feedback}$$

Applying KCL at the node P of Fig. 6.20

$$I_s = I_i + I_f \tag{6.98}$$

$$\text{But} \qquad I_i = \frac{V_i}{R_i} \quad \text{and} \quad I_f = \beta V_o$$

Substituting these relations in Equation (6.98) we have

$$I_s = \frac{V_i}{R_i} + \beta V_o$$

Also $$V_o = A I_i$$

$$= A \frac{V_i}{R_i}$$

Using this relation in the above Equation we get

$$I_s = \frac{V_i}{R_i} + \beta A \frac{V_i}{R_i}$$

$$= \frac{V_i}{R_i}[\,1 + \beta A\,]$$

Now $$R_{if} = \frac{V_i}{I_s} = \frac{R_i}{1+\beta A} \tag{6.99}$$

Since $[\,1+\beta A\,] > 1$

$$R_{if} < R_i$$

Note that the input resistance decreases by a factor $1+\beta A$ as expected for shunt mixing.

6.8.3 Input Resistance of Current-series Feedback Amplifier

The circuit for computation of the input resistance of a current-series feedback amplifier is shown in Fig. 6.21.

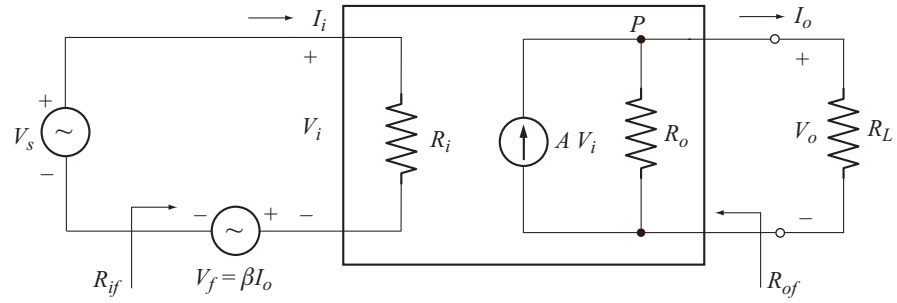


Fig. 6.21 Current-series feedback amplifier

$R_i = \dfrac{V_i}{I_i}$ = Input resistance without feedback

$R_{if} = \dfrac{V_s}{I_i}$ = Input resistance with feedback

Applying KVL to the input circuit of Fig. 6.21, we have

$$V_s - V_i - V_f = 0 \tag{6.100}$$

But $$V_i = I_i R_i \text{ and } V_f = \beta I_o$$

Using these relations in Equation (6.100) we have

$$V_s - I_i R_i - \beta I_o = 0 \tag{6.101}$$

But $$I_o = A V_i$$

$$= A I_i R_i$$

Using this relation in Equation (6.101) we get

$$V_s - I_i R_i - \beta A I_i R_i = 0$$

$$V_s = I_i R_i [1 + \beta A]$$

Now $$R_{i_f} = \frac{V_s}{I_i} = R_i [1 + \beta A] \tag{6.102}$$

Since $[1 + \beta A] > 1$

$$R_{i_f} > R_i$$

Note that the input resistance increases by a factor $1 + \beta A$ as expected for series mixing.

6.8.4 Input Resistance of Current-shunt Feedback Amplifier

Figure 6.22 shows the circuit of a current-shunt feedback amplifier for the computation of input resistance.

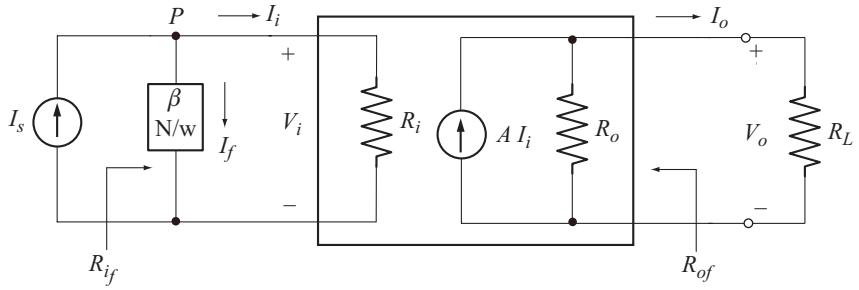


Fig. 6.22 Current-shunt feedback amplifier

$R_i = \frac{V_i}{I_i}$ = Input resistance without feedback,

$R_{i_f} = \frac{V_i}{I_s}$ = Input resistance with feedback.

Applying KCL to the input node *P* we have

$$I_s = I_i + I_f \tag{6.103}$$

But $$I_i = \frac{V_i}{R_i} \text{ and } I_f = \beta I_o$$

Substituting these relations in Equation (6.103) we have

$$I_s = \frac{V_i}{R_i} + \beta I_o \tag{6.104}$$

But $$I_o = A I_i$$

$$= A \frac{V_i}{R_i}$$

Using this relations in Equation (6.104) we have

$$I_s = \frac{V_i}{R_i} + \beta A \frac{V_i}{R_i}$$

$$= \frac{V_i}{R_i} [\, 1 + \beta A \,]$$

Now $$R_{if} = \frac{V_i}{I_s} = \frac{R_i}{1 + \beta A} \tag{6.105}$$

Since $[\, 1 + \beta A \,] > 1$

$$R_{if} < R_i$$

Note that input resistance decreases by a factor $1 + \beta A$ for shunt mixing.

◆ 6.9 EFFECT OF NEGATIVE FEEDBACK ON OUTPUT RESISTANCE

The effect of negative feedback on output resistance depends on the nature of sampling.

The output resistance decreases in the case of voltage sampling while it increases in the case of the current sampling.

Let us first see how voltage sampling reduces the output resistance. Consider the output circuit of a typical voltage amplifier shown in Fig. 6.23.

We know that, $$A_f = \frac{A}{1 + \beta A}$$

If $\beta A \gg 1$

Then $$A_f \approx \frac{A}{\beta A} = \frac{1}{\beta}$$

Note that A_f is independent of both source and load resistances. Thus, ideally the output voltage V_o would remain the same irrespective of changes in load resistance R_L in the presence of negative feedback. This is possible in the circuit of Fig. 6.23, only if

$$R_{of} \approx 0 \quad \text{or} \quad R_{of} \ll R_L$$

Under this condition, $$V_o = A_f V_s$$

The circuit to analyse the effect of negative feedback on a current sampling circuit is shown in Fig. 6.24.

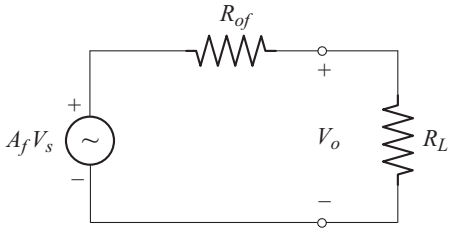


Fig. 6.23 Output stage of a feedback amplifier with voltage sampling

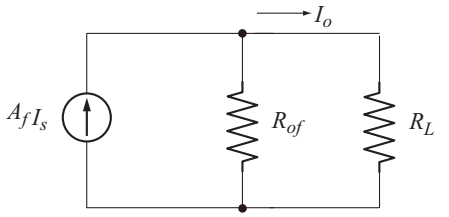


Fig. 6.24 Output stage of a feedback amplifier with current sampling

In this case, under stabilization through negative feedback the current I_o through R_L remain unchanged with changes in R_L, since A_f is independent of source and load resistances under negative feedback. This is obviously possible only if $R_{of} = \infty$ or $R_{of} \gg R_L$ in the circuit of Fig. 6.24, in which case

$$I_o = A_f I_s$$

6.9.1 Output Resistance of Voltage-Series Feedback Amplifier

We apply the following procedure to find the output resistance of feedback amplifier

1. Reduce V_s (I_s) to zero
2. Remove R_L and connect a voltage source V between the output terminals.

Let I be the current driven by the voltage source V into the amplifier output terminals. The output resistance with feedback is given by

$$R_{of} = \frac{V}{I} \tag{6.106}$$

Let us apply these steps to the voltage series feedback amplifier of Fig. 6.19. The resulting circuit is shown in Fig. 6.25.

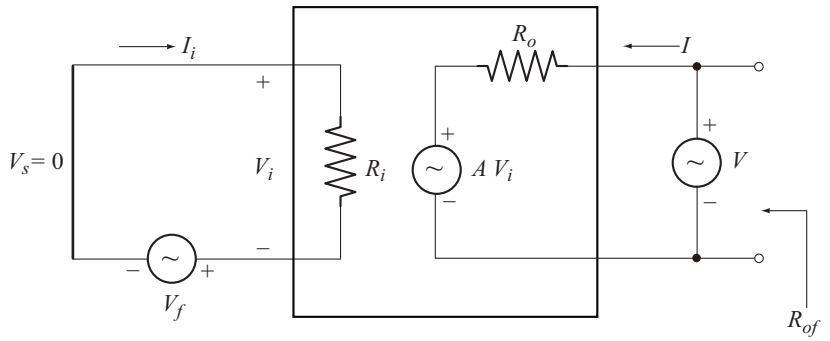


Fig. 6.25 Output resistance of voltage series feedback amplifier

Applying KVL to the input circuit we have

$$V_s - V_i - V_f = 0 \tag{6.107}$$

Since $V_s = 0$, we get

$$V_i = -V_f \tag{6.108}$$

$$V_f = \beta V_o$$

But $V_o = V$

$\therefore$ $V_f = \beta V$

Using this relation in Equation (6.108) we get

$$V_i = -\beta V \tag{6.109}$$

Applying KVL to the output circuit, we have

$$V - I R_o - A V_i = 0 \tag{6.110}$$

Substituting Equation (6.109) in Equation (6.110) we have

$$V - I R_o - A[-\beta V] = 0$$

$$V[1 + \beta A] = I R_o$$

Now $$R_{of} = \frac{V}{I} = \frac{R_o}{1 + \beta A} \tag{6.111}$$

Since, $(1 + \beta A) > 1$

$$R_{of} < R_o$$

Note that the output resistance decreases by a factor $1+\beta A$ as expected for voltage sampling.

6.9.2 Output Resistance of Voltage Shunt Feedback Amplifier

Let us obtain the equivalent circuit shown in Fig. 6.26 from the circuit of Fig. 6.20 by

1. Reducing I_s to zero,
2. Replacing R_L by a voltage source V.

Applying KCL at the node P of the circuit of Fig. 6.26

$$I_i + I_f = 0$$

$\therefore$ $I_i = -I_f$ (6.112)

But $I_f = \beta V_o = \beta V$

$\therefore$ $I_i = -\beta V$ (6.113)

Applying KVL to the output circuit of Fig. 6.26

$$A\,I_i + I\,R_o - V = 0 \tag{6.114}$$

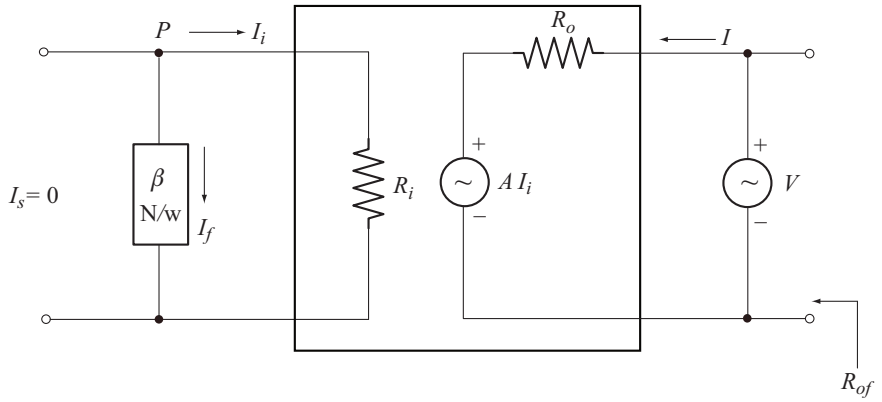


Fig. 6.26 Output resistance of voltage shunt feedback amplifier

Substituting for I_i from Equation (6.113)

$$A\,(-\beta\,V) + I\,R_o - V = 0$$

$$I\,R_o = V\,(1 + A\,\beta) \tag{6.115}$$

By definition

$$R_{of} = \frac{V}{I}$$

∴ From Equation (6.115)

$$R_{of} = \frac{R_o}{1 + \beta\,A} \tag{6.116}$$

Since $[1 + \beta\,A] > 1$

$$R_{of} < R_o$$

Note that the output resistance decreases by a factor $1 + \beta\,A$ as expected for voltage sampling.

6.9.3 Output Resistance of Current Series Feedback Amplifier

Let us obtain the equivalent circuit of the current series feedback amplifier shown in Fig. 6.21 to calculate the output resistance. The equivalent circuit is shown in Fig. 6.27.

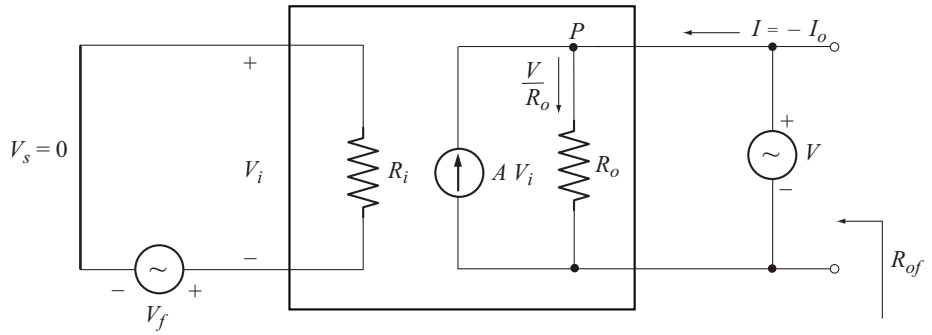


Fig. 6.27 Output resistance of current series feedback amplifier

Applying KVL to the input circuit of Fig. 6.27, we have

$$-V_i - V_f = 0 \tag{6.117}$$

or $$V_i = -V_f$$

By definition

$$V_f = \beta I_o$$

But $$I_o = -I \tag{6.118}$$

$$\therefore \quad V_f = -\beta I$$

Substituting this relation in Equation 6.117, we have

$$V_i = \beta I \tag{6.119}$$

Applying KCL at node P of the circuit in Fig. 6.27

$$A V_i + I - \frac{V}{R_o} = 0 \tag{6.120}$$

Substituting for V_i from Equation (6.119)

$$A\beta I + I = \frac{V}{R_o}$$

$$\frac{V}{R_o} = I(1 + A\beta) \tag{6.121}$$

By definition,

$$R_{of} = \frac{V}{I}$$

$$\therefore \quad R_{of} = R_o(1 + \beta A) \tag{6.122}$$

Since $[1 + \beta A] > 1$

$$R_{of} > R_o$$

Note that output resistance increases by a factor $1 + \beta A$ as expected for current sampling.

6.9.4 Output Resistance of Current-shunt Feedback Amplifier

Let us obtain the equivalent circuit of the current-shunt feedback amplifier shown in Fig. 6.22 to calculate the output resistance. The equivalent circuit is shown in Fig. 6.28.

Applying KCL at node *P* of the input circuit shown in Fig. 6.28, we have

$$I_i + I_f = 0 \tag{6.123}$$

or $I_i = -I_f$

By definition $I_f = \beta I_o$

But $I_o = -I$

$\therefore$ $I_f = -\beta I$ (6.124)

Substituting this relation in Equation (6.123), we have

$$I_i = \beta I \tag{6.125}$$

Applying KCL at node *Q* of the output circuit in Fig. 6.28, we have.

$$A I_i + I - \frac{V}{R_o} = 0$$

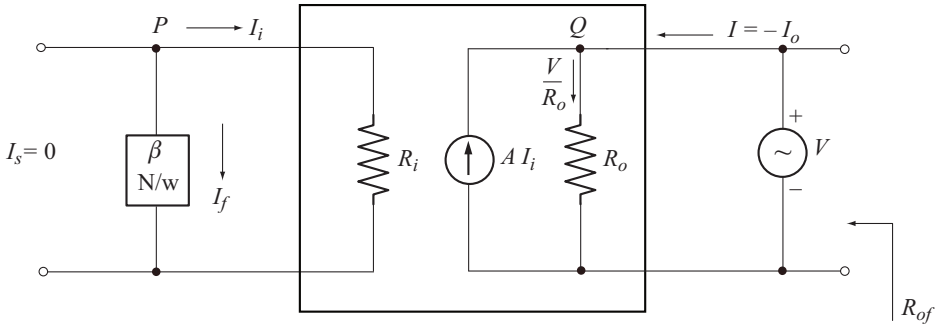


Fig. 6.28 Output resistance of current shunt feedback amplifier

Substituting for I_i from Equation (6.125)

$$A\beta I + I = \frac{V}{R_o} \tag{6.126}$$

$$I(1+\beta A) = \frac{V}{R_o}$$

By definition, $R_{of} = \frac{V}{I}$

$\therefore$ From Equation (6.126)

$$R_{of} = R_o(1 + \beta A) \tag{6.127}$$

Since $[1 + \beta A] > 1$

$$R_{of} > R_o$$

Note that the output resistance increases by a factor $1+\beta A$ as expected for current sampling.

Table 6.4 Summarizes the effect of negative feedback on input and output resistances on all the feedback topologies.

Table 6.4 Summary of effect of negative feedback on input and output resistance

Parameter	*Feedback topologies*			
	Voltage series	*Voltage shunt*	*Current series*	*Current shunt*
R_{if}	$R_i\ (1 + \beta A)$	$\frac{R_i}{1+\beta A}$	$R_i(\ 1 + \beta A)$	$\frac{R_i}{1+\beta A}$
R_{of}	$\frac{R_o}{1+\beta A}$	$\frac{R_o}{1+\beta A}$	$R_o(1 + \beta A)$	$R_o\ (1 + \beta A)$

◆ 6.10 EFFECT OF NEGATIVE FEEDBACK ON BANDWIDTH

For any amplifier the product of gain and bandwidth called the gain-bandwidth product is a constant whether the feedback is present or not.

∴ Gain-bandwidth product with feedback = Gain-bandwidth product without feedback

$$[A_f]\,[B\,W_f] = [A][B\,W]$$

or
$$B\,W_f = \frac{A}{A_f}\,B\,W \tag{6.128}$$

where $B\,W$ = Bandwidth without feedback
$B\,W_f$ = Band width with feedback

Since
$$A_f = \frac{A}{1+\beta A}$$

We have
$$\frac{A}{A_f} = 1 + \beta A$$

Using this relation in Equation (6.128) we have

$$B\,W_f = B\,W\,[\,1+\beta A\,] \tag{6.129}$$

Since $[\,1+\beta A\,] > 1$

$$B\,W_f > B\,W$$

Note that bandwidth increases by a factor $[1+\beta A]$ since the gain reduces by the same factor, in order to keep the gain bandwidth product constant.

Figure 6.29 shows the effect of negative feedback on bandwidth and gain.

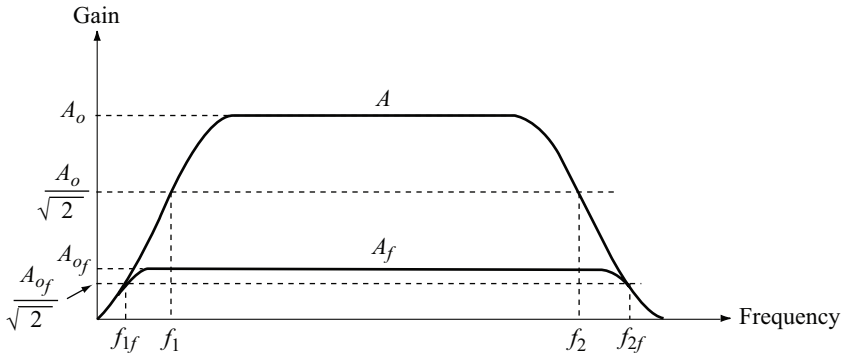


Fig. 6.29 Effect of negative feedback on gain and band width

A_o = Midband gain without feedback

A_{of} = Midband gain with feedback

$$A_{of} = \frac{A_o}{1+\beta A_o} \tag{6.130}$$

$$BW_f = f_{2f} - f_{1f} \tag{6.131}$$

$$BW = f_2 - f_1 \tag{6.132}$$

f_{2f} and f_{1f} are the upper and lower 3 dB frequencies with feedback. f_2 and f_1 are the corresponding frequencies without feedback.

Observe that

$$f_{1f} < f_1$$

and $$f_{2f} > f_2$$

6.11 ADVANTAGES OF NEGATIVE FEEDBACK

The advantages of negative feedback can now be listed based on the discussions in the preceding sections.

- Negative feedback stabilizes transfer gain.
- Negative feedback reduces non-linear distortion by a factor, $1 + \beta A$. This means that the operation of the amplifier becomes more linear than without feedback.
- Noise output is reduced by a factor, $1 + \beta A$.
- Negative feedback reduces frequency distortion.
- Voltage amplifiers generally have a high input resistance and a low output resistance. Negative feedback further increases the input resistance and further decreases the output resistance for a voltage amplifier.

Similarly, for other topologies, the input and output resistances improve towards their ideal values.

- Negative feedback improves the frequency response of an amplifier.

It is to be noted that all these advantages are derived at the cost of transfer gain as we have seen that the transfer gain with feedback is less than the transfer gain with out feedback.

Example 6.6

An amplifier has a bandwidth of 200 kHz and a voltage gain of 1000.

(a) What will be the new bandwidth and gain if 5% negative feedback is introduced.
(b) What is the gain-bandwidth product with and without feedback.
(c) What should be the amount of feedback if the bandwidth required is 1 MHz.

Solution

Bandwidth without feedback $BW = 200$ kHz.

Voltage gain without feedback $A = 1000$

(a) $$\% \beta = 5\% \Rightarrow \beta = 0.05$$
$$1 + \beta A = 1 + (1000)(0.05) = 51$$

$\therefore$ Bandwidth with feedback

$$BW_f = BW \times (1 + \beta A)$$
$$= (200 \text{ kHz})(51) = 10200 \text{ kHz}.$$
$$BW_f = 10.2 \text{ MHz}$$

(b) Gain bandwidth product without feedback is

$$(A)(BW) = (1000)(200 \text{ kHz}) = 2 \times 10^8$$

$$A_f = \frac{A}{1 + \beta A} = \frac{1000}{51} = 19.6$$

Gain bandwidth product with feedback is

$$(A_f)(BW_f) = (19.6)(10.2 \times 10^6) = 2 \times 10^8$$

The gain bandwidth product is the same with and without feedback as expected

(c) Given $BW_f = 1$ MHz

$$BW_f = BW[1 + \beta A]$$

$$\therefore \quad 1 + \beta A = \frac{BW_f}{BW} = \frac{1 \text{ MHz}}{200 \text{ kHz}} = 5$$

Now $$\beta = \frac{5 - 1}{A} = \frac{4}{1000} = 0.004 \text{ or } 0.4\%$$

Example 6.7

An amplifier has a open-loop voltage gain $A = 1000 \pm 100$. It is required to have an amplifier whose voltage gain varies by no more than $\pm$ 0.1 %.

(a) Find the reverse transmission factor β of the feedback network used.
(b) Find gain with feedback.

Solution

Given $A = 1000 \pm 100$

Gain varies between 900 and 1100

Nominal value of gain $A = 1000$

and $\pm \Delta A = \pm 100$

$$\frac{\Delta A}{A} = \frac{100}{1000} = 0.1$$

or $$\% \frac{\Delta A}{A} = 0.1 \times 100 = 10\ \%$$

(a) It is required to have a gain variation of 0.1 %

i.e., $$\% \frac{\Delta A_f}{A_f} = 0.1\ \%$$

or $$\frac{\Delta A_f}{A_f} = \frac{0.1}{100} = 0.001$$

From Equation (6.79)

$$|1+\beta A| = \frac{\left|\frac{\Delta A}{A}\right|}{\left|\frac{\Delta A_f}{A_f}\right|}$$

$$= \frac{0.1}{0.001} = 100$$

$$\beta = \frac{100-1}{A} = \frac{99}{1000} = 0.099$$

or $$\% \beta = 9.9\ \%$$

(b) $$A_f = \frac{A}{1+\beta A} = \frac{1000}{100} = 10$$

Now $$A_f = 10 \pm 0.1\% = 10 \pm 0.01$$

Note that A_f varies between 9.99 and 10.01.

Example 6.8

An amplifier consists of three identical stages connected in cascade. The output voltage is sampled and returned to the input in series opposing. It is desired that the relative change $\frac{dA_f}{A_f}$ in the closed-loop voltage gain A_f must not exceed ϕ_f. Show that the minimum value of the open-loop gain A of the amplifier is given by

$$A = [\,3A_f\,]\,\frac{|\phi_1|}{|\phi_f|}$$

where ϕ_1 is defined as $\frac{dA_1}{A_1}$ is the relative change in the voltage gain of each stage of the amplifier.

Solution

$$\left|\frac{d\,A_f}{A_f}\right| = \frac{\left|\frac{dA}{A}\right|}{|1 + A\beta|} \tag{A}$$

Let A_1 = gain of the each stage without feedback.
∴ Overall gain without feedback is

$$A = A_1 \times A_1 \times A_1 = A_1^{\,3} \tag{B}$$

Differentiating Equation (B) with respect to A_1

$$\frac{d\,A}{d\,A_1} = 3\,A_1^{\,2}$$

or
$$d\,A = 3\,A_1^{\,2}\,.\,d\,A_1 \tag{C}$$

From Equation (B)
$$A = A_1^{\,2}\,.\,A_1$$

∴
$$A_1^{\,2} = \frac{A}{A_1}$$

Substituting in Equation (C)

$$d\,A = \frac{3A}{A_1}\,.\,d\,A_1 \tag{D}$$

or
$$\frac{d\,A}{A} = 3\,\frac{d\,A_1}{A_1}$$

Given
$$\phi_1 = \frac{d\,A_1}{A_1}$$

Therefore, Equation (D) becomes

$$\left.\begin{aligned} \frac{d A}{A} &= 3\,\phi_1 \\ \text{Also given} \quad \frac{d A_f}{A_f} &= \phi_f \end{aligned}\right\} \tag{E}$$

Substituting Equation (E) in Equation (A)

$$|\phi_f| = \frac{|3\phi_1|}{|1 + A\beta|} \tag{F}$$

But $$A_f = \frac{A}{1 + A\beta}$$

$$\therefore \quad 1 + A\beta = \frac{A}{A_f}$$

Substituting this relation in Equation (F)

$$\left|\phi_f\right| = 3\,\frac{\left|\phi_1\right|}{\left|\frac{A}{A_f}\right|} = 3\,A_f\,\frac{\left|\phi_1\right|}{|A|}$$

$$\therefore \quad A = 3\,A_f\,\frac{\left|\phi_1\right|}{\left|\phi_f\right|}$$

Example 6.9

An amplifier without feedback gives a fundamental output of 36 V with 7% second-harmonic distortion when the input is 0.028 V.

(a) What is the output voltage if 1.2 % of the output is fed back into the input in a negative voltage - series feedback circuit?

(b) What is the input voltage if the fundamental output is maintained at 36 V but the second harmonic distortion is reduced to 1 %.

Solution

Fundamental output voltage without feedback $V_o = 36$ V

% second-harmonic distortion without feedback $\%\,B_2 = 7\,\%$

Input voltage without feedback $V_i = 0.028$ V

Voltage gain without feedback

$$A_V = \frac{V_o}{V_i} = \frac{36}{0.028} = 1285.7$$

(a) $$\% \ \beta = 1.2\%$$

$$\therefore \quad \beta = \frac{1.2}{100} = 0.012$$

Now $$1 + A_V \beta = 1 + (1285.7)\ (0.012)$$

$$= 16.4284$$

$$A_{Vf} = \frac{A_V}{1+\beta A_V} = \frac{1285.7}{16.4284}$$

$$= 78.26$$

$$A_{Vf} = \frac{V_{of}}{V_{if}}$$

V_{if} is the input voltage with feedback. Since input voltage has not changed,

$$V_{if} = V_i = 0.028 \text{ V}$$

Now $$V_{of} = A_{Vf}\ V_{if} = (78.26)\ (0.028 \text{ V}) = 2.19 \text{ V}$$

(b) % second-harmonic distortion with feedback is given as

$$\% \ B_{2f} = 1\ \%$$

and $$V_{of} = 36 \text{ V}$$

$$\% \ B_{2f} = \frac{\%B_2}{1+\beta A_V}$$

$$\therefore \quad 1 + \beta A_V = \frac{\%B_2}{\%B_{2f}} = \frac{7}{1} = 7$$

Voltage gain with feedback

$$A_{Vf} = \frac{A_V}{1+\beta A_V} = \frac{1285.7}{7} = 183.67$$

$$A_{Vf} = \frac{V_{of}}{V_i}$$

or $$V_i = \frac{V_{of}}{A_{Vf}} = \frac{36\text{V}}{183.67} = 0.196 \text{ V}$$

Example 6.10

An amplifier with an open-loop gain of 1000 delivers 10 W of output power at 10% second-harmonic distortion when the input signal is 10 mV. If 40 dB negative voltage-series feedback is applied and the output power is to remain at 10 W, determine.

(a) the required input signal,
(b) % harmonic distortion

Solution

Open-loop voltage gain means gain without feedback

$$\therefore \qquad A_V = 1000$$

Output power without feedback

$$P_o = 10 \text{ W}$$

$$P_o = \frac{V_o^2}{R_L} \qquad \text{(A)}$$

where R_L is the load resistance.

% second harmonic-distortion without feedback, % B_2 = 10 %

Input voltage, $V_i = 10 \text{ mV}$

$$A_V = \frac{V_o}{V_i}$$

$$\therefore \qquad V_o = A_V \cdot V_i = 1000 \times 10 \text{ mV} = 10 \text{ V}$$

Negative feedback in dB,

$$N = -40 \text{ dB}$$

$$N = 20 \log_{10} \left[\frac{1}{1 + \beta A_V} \right]$$

$$= -20 \log_{10} [1 + \beta A_V]$$

$$-40 = -20 \log_{10} [1 + \beta A_V]$$

$$\log_{10} [1 + \beta A_V] = 2$$

$$1 + \beta A_V = \log_{10}^{-1} [2] = 100$$

Now $$A_{Vf} = \frac{A_V}{1 + \beta A_V} = \frac{1000}{100} = 10$$

(a) Output power with feedback is $P_{of} = 10 \text{ W} = P_o$

$$P_{of} = \frac{V_{of}^2}{R_L} \qquad \text{(B)}$$

Since R_L is fixed, from Equations (A) and (B) we find that

$$V_{of} = V_o = 10 \text{ V}$$

$$A_{Vf} = \frac{V_{of}}{V_{if}}$$

$\therefore$ The required input voltage is, $V_{if} = \frac{V_{of}}{A_{Vf}} = \frac{10}{10} = 1 \text{ V}$

(b) % second harmonic distortion with feedback is

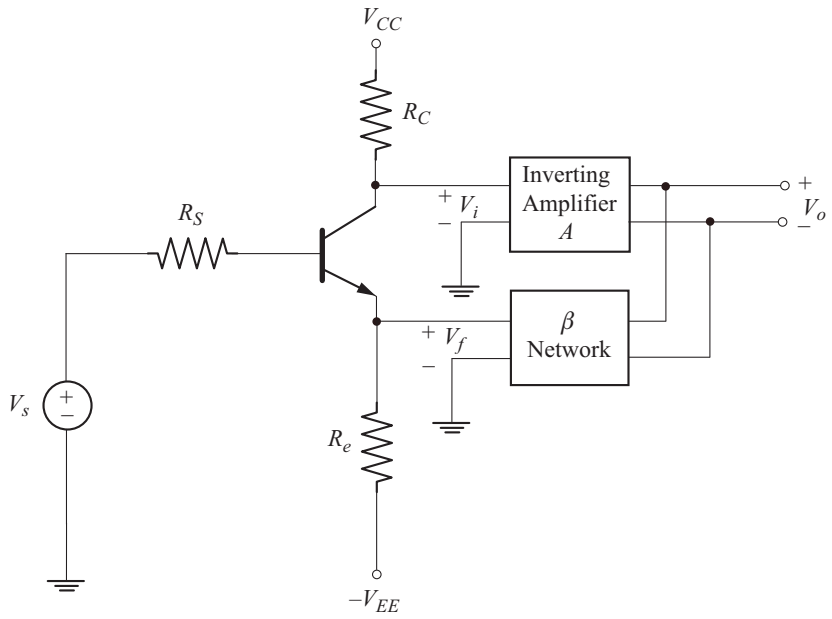
$$\% B_{2f} = \frac{\% B_2}{D} = \frac{10\%}{100}$$

or $$\% B_{2f} = 0.1\%$$

Example 6.11

(a) For the circuit shown, find the ac voltage V_i as a function of V_s and V_f. Assume that the input resistance of inverting amplifier is infinite. $A = A_V = -1000$, $\beta = \frac{V_f}{V_o} = \frac{1}{100}$, $R_s = R_C = R_e = 1\,\text{k}\Omega$, $h_{ie} = 1\,\text{k}\Omega$, $h_{re} = h_{oe} = 0$ and $h_{fe} = 100$.

(b) Find $A_{Vf} = \frac{V_o}{V_s} = \left(A \frac{V_i}{V_s} \right)$



Solution

$$A = A_V = -1000$$

$$\beta = \frac{1}{100} = \frac{V_f}{V_o}$$

$$R_s = R_C = R_e = 1\,\text{k}\Omega$$

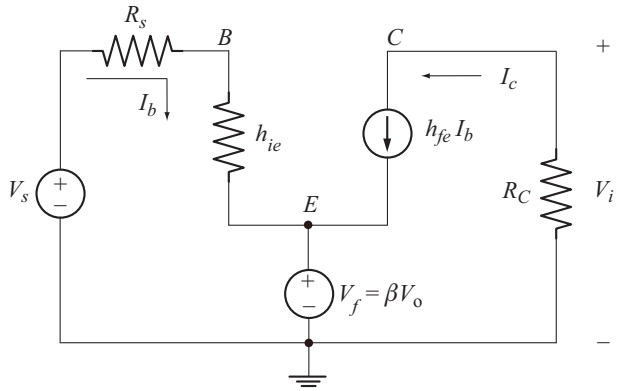
$$h_{ie} = 1\,\text{k}\Omega$$

$$h_{re} = h_{oe} = 0$$
$$h_{fe} = 100$$

(a) β network provides an output voltage V_f proportional to its input voltage V_o, which is nothing but the inverting amplifier output voltage.

$$V_f = \beta V_o \tag{A}$$

Let us write the ac equivalent circuit of transistor amplifier. Since $h_{re} = 0$, $h_{re} V_{ce}$ can be treated as short-circuit and $1/h_{oe}$ can be treated as open circuit since $h_{oe} = 0$.



$$V_i = -I_c R_C$$

But $$I_c = h_{fe} I_b$$

$\therefore$ $$V_i = -h_{fe} I_b R_C \tag{B}$$

Applying KVL to the input circuit

$$V_s - I_b R_s - I_b h_{ie} - V_f = 0$$

$\therefore$ $$I_b = \frac{V_s - V_f}{R_s + h_{ie}} \tag{C}$$

Combining Equations (B) and (C), we get

$$V_i = -h_{fe} R_C \frac{V_s - V_f}{R_s + h_{ie}}$$

$$= -(100)\ (1\ \text{k}\Omega)\ \frac{(V_s - V_f)}{(1\ \text{k}\Omega + 1\ \text{k}\Omega)}$$

$\therefore$ $$V_i = -50\ (V_S - V_f) \tag{D}$$

(b) For the inverting amplifier

$$V_o = A\, V_i = A_V\, V_i$$

Substituting for V_i from Equation (D), we have

$$V_o = A_V\,[-50\,(V_s - V_f)\,]$$
$$V_o = -50\;A_V V_s + 50\;A_V V_f$$

Substituting for V_f from Equation (A) we have

$$V_o = -50\,A_V V_s + 50\,A_V\,(\beta\, V_o)$$
$$V_o\,[1 - 50\,\beta\,A_V] = -50\;A_V\,V_S$$
$$\therefore \quad A_{Vf} = \frac{V_o}{V_s} = \frac{-50\,A_V}{1 - 50\,\beta\,A_V}$$
$$= \frac{-(50)(-1000)}{1 - 50\left(\frac{1}{100}\right)(-1000)}$$
$$A_{Vf} = 99.8$$

Example 6.12

A voltage amplifier has the following parameter values without feedback.

$$A_V = -1000, \quad R_i = 20\ \text{k}\Omega, \quad R_o = 15\ \text{k}\Omega, \quad \text{Bandwidth} = 200\ \text{kHz}$$

Compute these parameter values if negative-series feedback with $\beta = -0.1$ is given.

Solution

$$1 + \beta\,A_V = 1 + (-0.1)\,(-1000) = 101$$
$$A_{Vf} = \frac{A_V}{1 + \beta\,A_V} = \frac{-1000}{101} = -9.9$$

Series mixing input resistance

$$\therefore \quad R_{if} = R_i\,[\,1 + \beta\,A_V\,] = (20\ \text{k}\Omega)\,(101) = 2.02\ \text{M}\Omega$$

Voltage sampling reduces output resistance

$$\therefore \quad R_{of} = \frac{R_o}{1 + \beta\,A_V} = \frac{15\,\text{k}\Omega}{101} = 148.51\ \Omega$$
$$BW_f = BW\;[1 + \beta\,A_V] = (200\ \text{kHz})\,(101) = 20.2\ \text{MHz}$$

◆ 6.12 PRACTICAL FEEDBACK CIRCUITS

So for we have studied the effect of negative feedback in various topologies using the block diagram approach. Now let us study the practical feedback circuits.

6.12.1 FET Amplifier with Voltage-series Feedback

Figure 6.30 shows common source FET amplifier with voltage-series feedback.

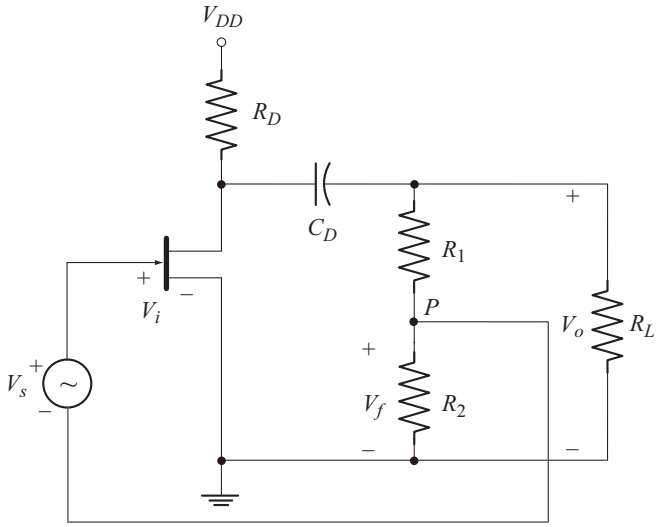


Fig. 6.30 FET amplifier with voltage-series feedback

The output voltage V_o is divided in the voltage divider consisting of R_1 and R_2. The feedback voltage is the voltage across R_2. Using voltage division rule,

$$V_f = \frac{R_2}{R_1 + R_2} V_o \tag{6.133}$$

Equation (6.133) is of the form

$$V_f = \beta V_o \tag{6.134}$$

We find that

$$\beta = \frac{V_f}{V_o} = \frac{R_2}{R_1 + R_2} \tag{6.135}$$

Note that the feedback voltage is proportional to output voltage. Hence the sampled signal is the output voltage.

Applying KVL to the input circuit we have

$$V_s - V_i - V_f = 0$$

or

$$V_i = V_s - V_f \tag{6.136}$$

Note that V_f is mixed in series with V_s. Also V_f subtracts from V_s which implies that feedback is negative.

The sampled signal is the output voltage and the feedback voltage derived from the output voltage is mixed in series with the source voltage. Hence the topology is voltage voltage series feedback. Also the basic amplifier is a voltage amplifier.

Basic Amplifier without Feedback

Let us obtain the ac equivalent circuit of the basic amplifier without feedback from the feedback amplifier of Fig. 6.30.

- To obtain ac equivalent circuit let us short the coupling capacitor C_D and reduce V_{DD} to zero.
- To reduce feedback to zero, we have to open the connection at *P* and connect it to ground. The ac equivalent circuit of basic amplifier without feedback is shown in Fig. 6.31.

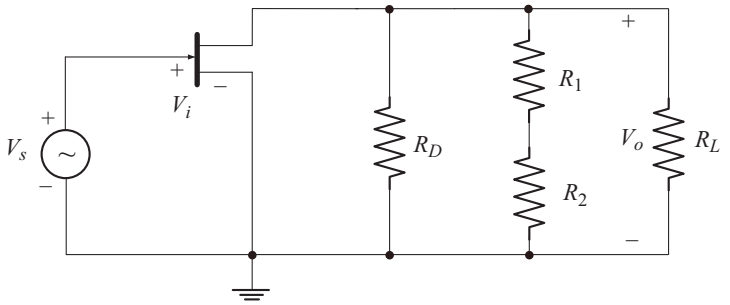


Fig. 6.31 Basic amplifier without feedback

From Fig. 6.31, we find that

$$V_i = V_s \tag{6.137}$$

The effective load on the FET amplifier is

$$R'_L = R_D \,||\, [R_1 + R_2] \,||\, R_L \tag{6.138}$$

Analysis of FET amplifier is discussed in Chapter 9. The voltage gain of the common-source FET amplifier of Fig. 6.31 is given by

$$A_V = -g_m R'_L \tag{6.139}$$

Voltage gain with feedback is given by

$$A_{Vf} = \frac{A_V}{1+\beta A_V} \tag{6.140}$$

It is important to note that the product $\beta\, A_V$ should be positive. Since A_V is negative, it is appropriate to write

$$\beta = \frac{-R_2}{R_1 + R_2} \tag{6.141}$$

Now

$$1 + \beta\, A_V = 1 + \left[\frac{-R_2}{R_1 + R_2}\right]\left[-g_m R'_L\right]$$

$$= 1 + g_m \frac{R_2 R'_L}{R_1 + R_2} \tag{6.142}$$

Using Equations (6.139) and (6.142) in Equation (6.140) we have

$$A_{Vf} = \frac{-g_m R'_L}{1 + g_m \dfrac{R_2 R'_L}{R_1 + R_2}} \tag{6.143}$$

If $\beta A_V \gg 1$, from Equation (6.140) we get

$$A_{Vf} \approx \frac{1}{\beta}$$

or
$$A_{Vf} = -\frac{R_1 + R_2}{R_2} \tag{6.144}$$

Note that A_{Vf} depends only on the external resistors R_1 and R_2 and independent of the FET parameter g_m. If R_1 and R_2 are stable resistors, then A_{Vf} is also stabilized.

Example 6.13

The FET amplifier of Fig. 6.30 has the following parameter values.

$$R_1 = 100\ \text{k}\Omega \quad R_2 = 10\ \text{k}\Omega \quad R_L = 15\ \text{k}\Omega$$
$$R_D = 10\ \text{k}\Omega \quad g_m = 5000\ \mu\text{S}$$

Calculate the voltage gains A_V and A_{Vf}.

Solution

$$R_L' = R_D \,||\, [\, R_1 + R_2 \,] \,||\, R_L$$
$$= 10\ \text{k}\Omega \,||\, [\, 100\ \text{k}\Omega + 10\ \text{k}\Omega \,] \,||\, 15\ \text{k}\Omega$$
$$= 5.68\ \text{k}\Omega$$
$$A_V = -g_m R'_L$$
$$= -(5000\ \mu\text{S})\,(5.68\ \text{k}\Omega) = -28.4$$
$$\beta = \frac{-R_2}{R_1 + R_2} = -\frac{10\ \text{k}\Omega}{100\ \text{k}\Omega + 10\ \text{k}\Omega} = -0.09$$
$$1 + \beta A_V = 1 + (-0.09)(-28.4) = 3.556$$
$$A_{Vf} = \frac{A_V}{1 + \beta A_V} = -\frac{28.4}{3.556} = -7.9865$$

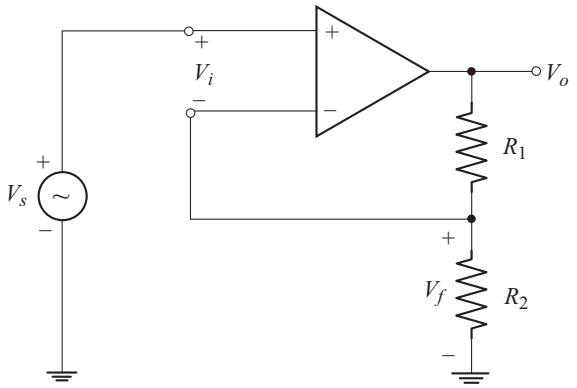
Example 6.14

For the op-amp non inverting amplifier shown below, the following data are available:

$$A_V = 2 \times 10^5 \quad R_1 = 10\ \text{k}\Omega$$

$$R_i = 2\ \text{M}\Omega \quad R_2 = 1\ \text{k}\Omega$$
$$R_o = 75\ \Omega$$

Calculate A_{Vf}, R_{if} and R_{of}.



Solution

Using voltage division rule at the output we have

$$V_f = \frac{R_2}{R_1 + R_2} V_o = \beta V_o$$

Note that feedback voltage is derived from output voltage.

$$\therefore \quad \beta = \frac{R_2}{R_1 + R_2}$$
$$= \frac{1\ \text{k}\Omega}{10\ \text{k}\Omega + 1\ \text{k}\Omega} = 0.09$$

Applying KVL to the input circuit we have

$$V_s - V_i - V_f = 0$$
$$\Rightarrow \quad V_i = V_s - V_f$$

Note that mixing is series.
Hence the topolgy is voltage series feedback.

$$1 + \beta A_V = 1 + (0.09)(2 \times 10^5) = 18{,}001$$
$$A_{Vf} = \frac{A_V}{1 + \beta A_V} = \frac{2 \times 10^5}{18{,}001} = 11.11$$

Voltage sampling reduces the output resistance.

$$\therefore \quad R_{of} = \frac{R_o}{1 + \beta A_V} = \frac{75\ \Omega}{18{,}001} = 4.16\ \text{m}\Omega$$

Series mixing increases the input resistance.

$$\therefore \qquad R_{if} = R_i [\, 1 + \beta A_V] = (2\ \text{M}\Omega\ )\,(18{,}001) = 36{,}002\ \text{M}\Omega$$

Note: For op-amp non-inverting amplifier

$$A_{Vf} \approx 1 + \frac{R_1}{R_2} = 1 + \frac{10\,\text{k}\Omega}{1\,\text{k}\Omega} = 11$$

This result is consistent with the one which is calculated earlier since $\beta A_V \gg 1$.

6.12.2 Voltage Series Feedback in Emitter-follower

Figure 6.32 shows the circuit of emitter-follower which employs voltage series feedback.

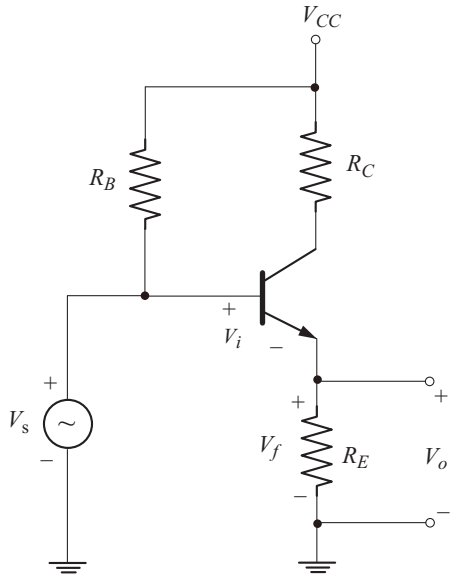


Fig. 6.32 Emitter-follower

From the circuit of Fig. 6.32 we find that

$$V_f = V_o \tag{6.145}$$

But
$$V_f = \beta V_o \tag{6.146}$$

Comparing Equations (6.145) and (6.146) we find that

$$\beta = \frac{V_f}{V_o} = 1 \tag{6.147}$$

Note that the entire output voltage is fedback at the input or the feedback is 100 %.
Applying KVL to the input circuit we have

$$V_s - V_i - V_f = 0$$

or $$V_i = V_s - V_f \quad (6.148)$$

Note that V_f is mixed in series with V_s. Also, V_f subtracts from V_s which implies that feedback is negative.

The sampled signal is the output voltage and the feedback voltage derived from the output voltage is mixed in series with the source voltage. Hence the topology is voltage series feedback. Also the basic amplifier is a voltage amplifier.

The ac equivalent circuit of emitter-follower is obtained by reducing V_{CC} to zero in the circuit of Fig. 6.32. This is shown in Fig. 6.33.

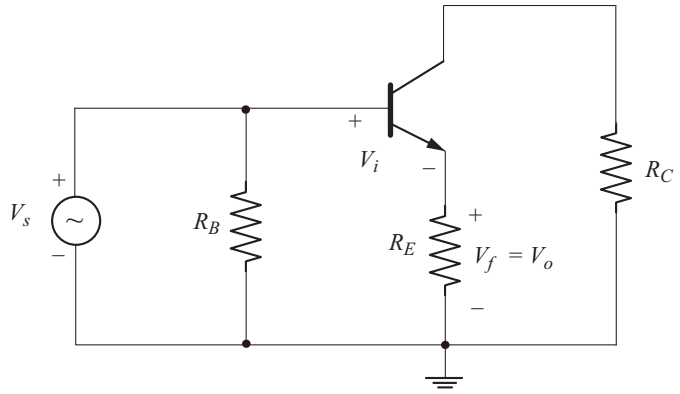


Fig. 6.33 AC equivalent circuit of emitter-follower

Basic Amplifier Circuit without Feedback

Now let us obtain the basic amplifier without feedback. This can be obtained by combining the features of input and output circuits. The procedures for drawing the input and output circuits are given below.

To draw the input circuit, we have to reduce the sampling to zero. Since the output voltage is sampled, it can be reduced to zero by short circuiting R_E in the circuit of Fig. 6.33. The input circuit is shown in Fig. 6.34.

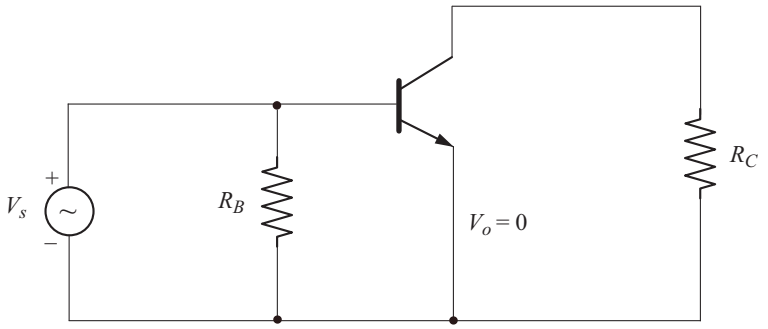


Fig. 6.34 Input circuit obtained by short circuiting R_E

To draw the output circuit, we have to avoid the mixing of V_f and V_s. This can be done by opening the input loop in the circuit of Fig. 6.33. The output circuit is shown in Fig. 6.35.

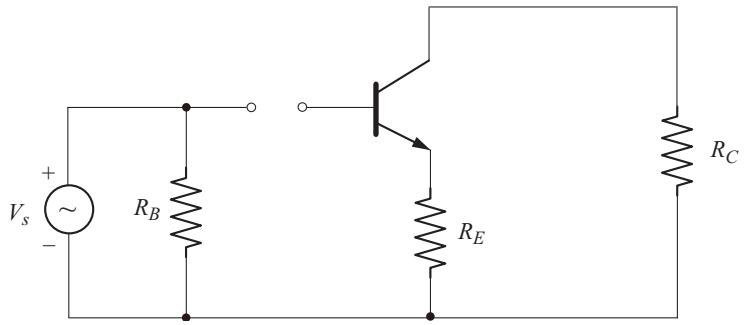


Fig. 6.35 Output circuit obtained by opening the input loop

The basic amplifier circuit without feedback is obtained by combing the features of input and output circuits as shown in Fig. 6.36.

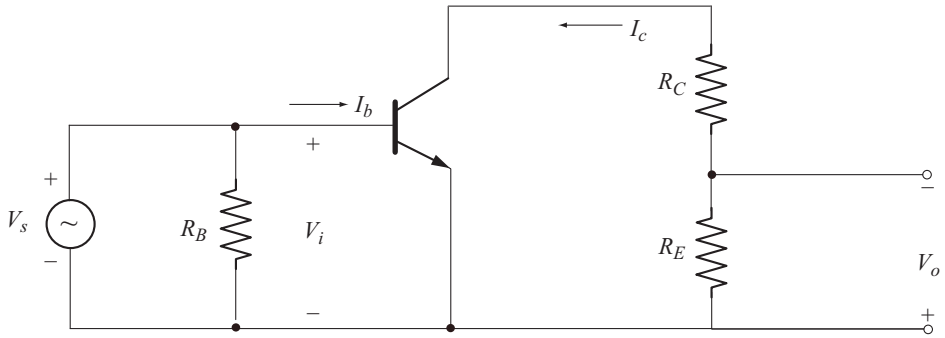


Fig. 6.36 Basic amplifier without feedback

Let us replace the transistor by its low frequency small signal approximate hybrid model as shown in Fig. 6.37.

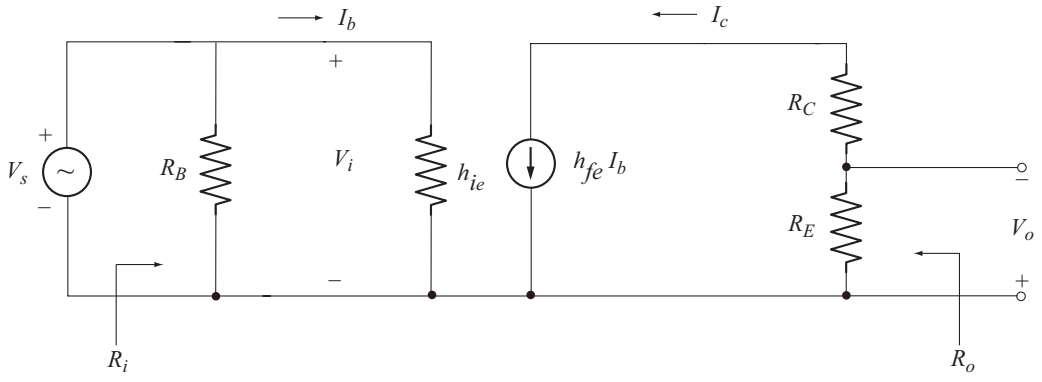


Fig. 6.37 Basic amplifier without feedback using hybrid model

Voltage Gain with Feedback

From the equivalent circuit of Fig. 6.37

$$V_i = h_{ie}\, I_b \tag{6.149}$$

$$V_o = I_c\, R_E$$

But $$I_c = h_{fe}\, I_b$$

$$\therefore \quad V_o = h_{fe}\; I_b\; R_E \tag{6.150}$$

Voltage gain without feedback is

$$A_V = \frac{V_o}{V_i}$$

$$= \frac{h_{fe} I_b\, R_E}{h_{ie}\, I_b}$$

$$A_V = \frac{h_{fe}\, R_E}{h_{ie}} \tag{6.151}$$

$$1 + \beta\, A_V = 1 + (1)\left[\frac{h_{fe} R_E}{h_{ie}}\right]$$

$$= \frac{h_{ie} + h_{fe} R_E}{h_{ie}} \tag{6.152}$$

Voltage gain with feedback is

$$A_{Vf} = \frac{A_V}{1+\beta A_V} = \frac{\left[\dfrac{h_{fe} R_E}{h_{ie}}\right]}{\left[\dfrac{h_{ie} + h_{fe} R_E}{h_{ie}}\right]}$$

$$A_{Vf} = \frac{h_{fe} R_E}{h_{ie} + h_{fe} R_E} \tag{6.153}$$

Usually $$h_{fe}\, R_E \gg h_{ie}$$

$$\therefore \quad A_{Vf} \approx \frac{h_{fe}\, R_E}{h_{fe}\, R_E} = 1$$

which is true for emitter follower.

Input Resistance with Feedback

From the circuit of Fig. 6.37, the input resistance without feedback is

$$R_i = R_B \parallel h_{ie} \tag{6.154}$$

Usually $$R_B \gg h_{ie}$$

$$\therefore \quad R_i \approx h_{ie} \tag{6.155}$$

Series mixing increases input resistance. Therefore input resistance with feedback is

$$R_{if} = R_i[1 + \beta A_V]$$

$$= [h_{ie}]\left[\frac{h_{ie} + h_{fe}R_E}{h_{ie}}\right]$$

$$R_{if} = h_{ie} + h_{fe} R_E \tag{6.156}$$

Output Resistance with Feedback

To find the output resistance without feedback, let us reduce the current source to zero in the output circuit of Fig. 6.37. The resulting circuit is shown in Fig. 6.38.

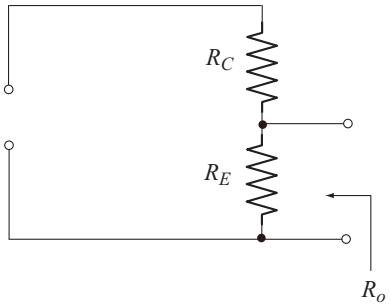


Fig. 6.38 Circuit to find output resistance

From the circuit of Fig. 6.38, output resistance without feedback is

$$R_o = R_E \tag{6.157}$$

Voltage sampling reduces output resistance. Therefore output resistance with feedback is

$$R_{of} = \frac{R_o}{1 + \beta A_V}$$

$$= \frac{R_E}{\left[\frac{h_{ie} + h_{fe}R_E}{h_{ie}}\right]}$$

$$= \frac{R_E h_{ie}}{h_{ie} + h_{fe}R_E} \tag{6.158}$$

If $h_{fe}R_E \gg h_{ie}$

then $R_{of} \approx \frac{R_E h_{ie}}{h_{fe} R_E}$

or $R_{of} = \frac{h_{ie}}{h_{fe}}$ (6.159)

Example 6.15

The following data is available for the voltage series feedback amplifier of Fig. 6.32.

$$R_B = 50\ \text{k}\Omega \quad R_E = 1\ \text{k}\Omega \quad R_C = 1\ \text{k}\Omega$$
$$h_{ie} = 2\ \text{k}\Omega \quad h_{fe} = 150$$

Calculate

(a) A_V and A_{Vf}
(b) R_i and R_{if}
(c) R_o and R_{of}

Solution

(a)
$$A_V = \frac{h_{fe} R_E}{h_{ie}} = \frac{(150)\ (1\text{k}\Omega)}{2\text{k}\Omega} = 75$$
$$1 + \beta A_V = 1 + 75 = 76 \ [\text{since } \beta = 1]$$
$$A_{Vf} = \frac{A_V}{1 + \beta A_V} = \frac{75}{76} = 0.986$$

(b)
$$R_i = R_B \| h_{ie}$$
$$= 50\ \text{k}\Omega \ \| \ 2\ \text{k}\Omega = 1.923\ \text{k}\Omega$$
$$R_{if} = R_i [1 + \beta A_V]$$
$$= (1.923\ \text{k}\Omega\ )\ (76) = 146.148\ \text{k}\Omega$$

Alternatively
$$R_{if} \approx h_{ie} + h_{fe}\ R_E$$
$$= 2\ \text{k}\Omega + (150)\ \ (1\ \text{k}\Omega\ )$$
$$= 152\ \text{k}\Omega$$

(c)
$$R_o = R_E = 1\ \text{k}\Omega$$
$$R_{of} = \frac{R_o}{1 + \beta A_V}$$
$$= \frac{1\text{k}\Omega}{76} = 13.15\ \Omega$$

Alternatively
$$R_{of} = \frac{h_{ie}}{h_{fe}} = \frac{2\ \text{k}\Omega}{150} = 13.33\ \Omega$$

16.12.3 Current Series Feedback Amplifier

Figure 6.39 shows the circuit of current series feedback amplifier. Note that the circuit is a CE amplifier with unbypassed R_E.

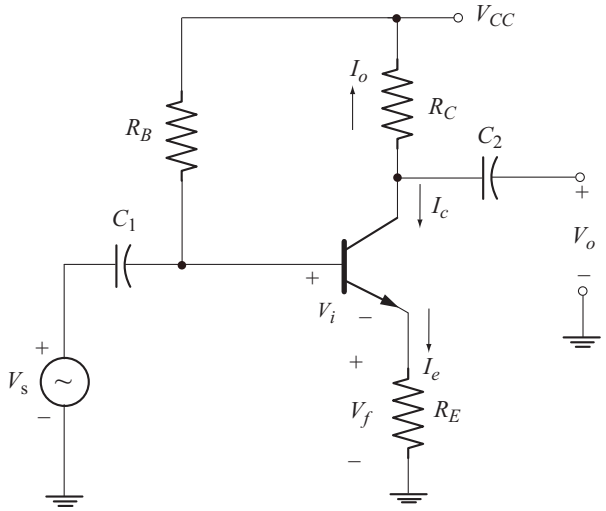


Fig. 6.39 Current series feedback amplifier

The feedback voltage is the voltage across R_E

$$V_f = I_e R_E \tag{6.160}$$

$$I_e \approx I_c$$

But $$I_c = -I_o$$

$\therefore$ $$I_e = -I_o \tag{6.161}$$

Using this relation in Equation (6.160) we have

$$V_f = -R_E I_o \tag{6.162}$$

Equation (6.162) is of the form

$$V_f = \beta I_o \tag{6.163}$$

We find that $$\beta = \frac{V_f}{I_o} = -R_E \tag{6.164}$$

Note that the feedback voltage is proportional to the output current. Hence the sampled signal is the output current.

Applying KVL to the input circuit we have

$$V_s - V_i - V_f = 0$$

or $$V_i = V_s - V_f \tag{6.165}$$

Note that V_f is mixed in series with V_S, also V_f subtracts from V_S which implies that feedback is negative.

The sampled signal is the output current and the feedback voltage derived from the output current is mixed in series with the source voltage. Hence the topology is current series feedback. Also the basic amplifier is a transconductance amplifier.

The ac equivalent circuit is obtained by reducing V_{CC} to zero and short circuiting the capacitors C_1 and C_2 as shown in Fig. 6.40.

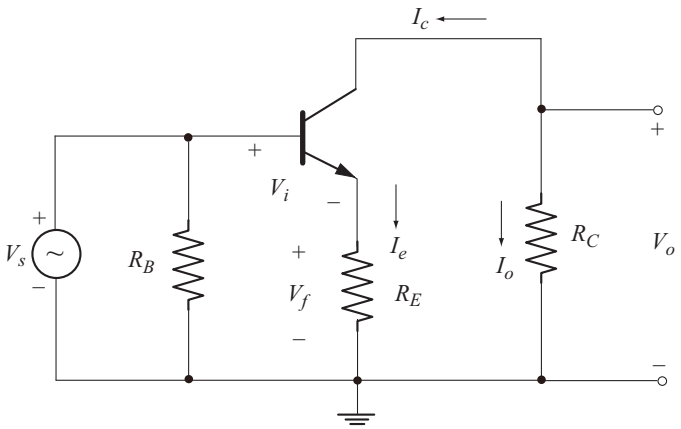


Fig. 6.40 AC equivalent circuit of current series feedback amplifier

Basic Amplifier Circuit without Feedback

The input circuit is obtained by reducing the sampling to zero. Since the output current is sampled, it can be reduced to zero by open circuiting the collector in the circuit of Fig. 6.40. This is shown in Fig. 6.41.

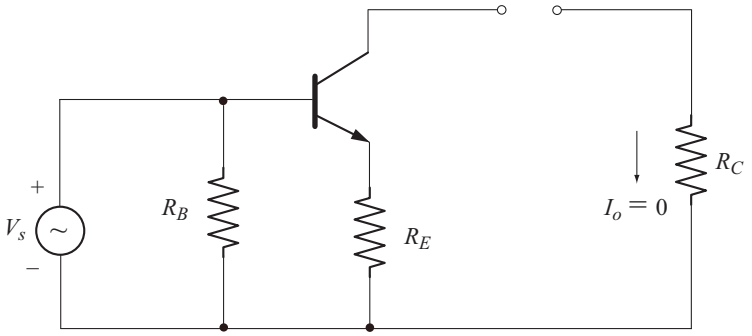


Fig. 6.41 Input circuit obtained by open circuiting the collector

The output circuit is obtained by reducing the mixing to zero. Since the mixing is series, the input loop has to be opened in the circuit of Fig. 6.40. This is shown in Fig. 6.42.

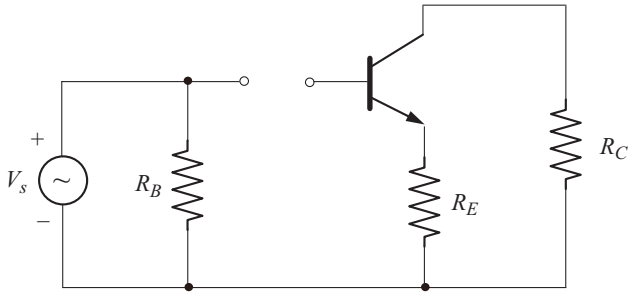


Fig. 6.42 Output circuit obtained by opening the input loop

The basic amplifier circuit without feedback is obtained by combining the features of input and output circuits as shown in Fig. 6.43.

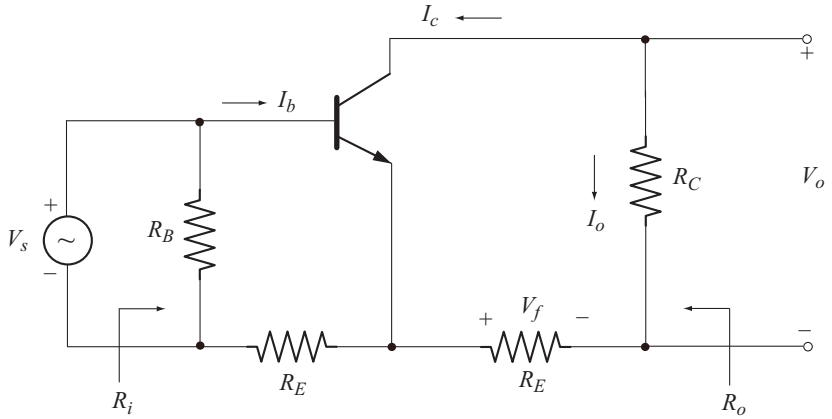


Fig. 6.43 Basic amplifier circuit without feedback

Let us replace the transistor by its small signal approximate hybrid equivalent circuit as shown in Fig. 6.44.

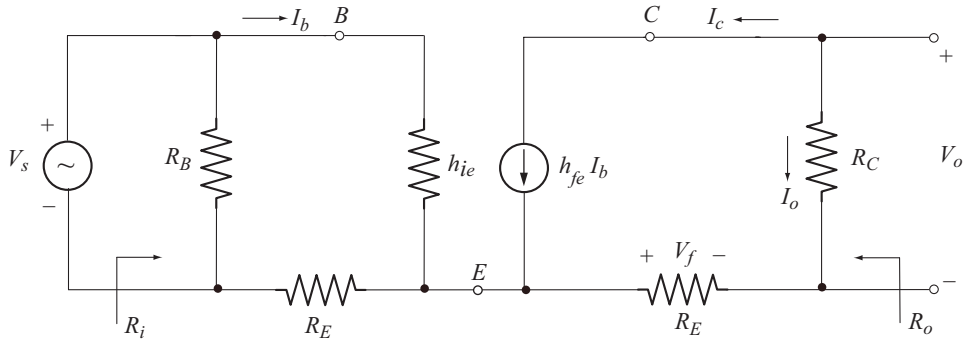


Fig. 6.44 AC equivalent circuit using hybrid model

Transfer Gain with Feedback

Since the basic amplifier is transconductance amplifier the transfer gain is the transcondcutance Transfer gain without feedback is given by

$$A = G_M = \frac{I_o}{V_i} \tag{6.166}$$

From Equation (6.165)

$$V_i = V_s - V_f$$

In the absence of feedback, $V_f = 0$

$$\therefore \quad V_i = V_s$$

Now from Equation 6.166 we have

$$A = \frac{I_o}{V_s} \tag{6.167}$$

But $I_o = -I_c$

and $I_c = h_{fe} I_b$

$$\therefore \quad I_o = -h_{fe} I_b \tag{6.168}$$

Applying KVL to the input circuit of Fig. 6.44 we have

$$V_s = I_b [h_{ie} + R_E] \tag{6.169}$$

Using Equations (6.168) and (6.169) in Equation (6.167) we have

$$A = \frac{-h_{fe} I_b}{I_b \left[h_{ie} + R_E\right]}$$

Now

$$A = G_M = \frac{-h_{fe}}{h_{ie} + R_E} \tag{6.170}$$

Transfer gain with feedback is

$$A_f = G_{Mf} = \frac{I_o}{V_s} = \frac{A}{1 + \beta A} \tag{6.171}$$

$$1 + \beta A = 1 + [-R_E] \left[\frac{-h_{fe}}{h_{ie} + R_E}\right]$$

$$= \frac{h_{ie} + \left(1 + h_{fe}\right) R_E}{h_{ie} + R_E} \tag{6.172}$$

Now

$$A_f = \frac{\left[\dfrac{-h_{fe}}{h_{ie} + R_E}\right]}{\left[\dfrac{h_{ie} + \left(1 + h_{fe}\right) R_E}{h_{ie} + R_E}\right]}$$

$$A_f = G_{Mf} = \frac{-h_{fe}}{h_{ie} + (1 + h_{fe}) R_E} \tag{6.173}$$

Since $h_{fe} \gg 1,\ (1 + h_{fe}) \approx h_{fe}$

Now
$$A_f = G_{Mf} \approx \frac{-h_{fe}}{h_{ie} + h_{fe} R_E} \tag{6.174}$$

Input Resistance with Feedback

From the circuit of Fig. 6.44, the input resistance without feedback is

$$R_i = R_B \,||\, [h_{ie} + R_E]$$

Usually $R_B \gg h_{ie} + R_E$

$$\therefore \quad R_i \approx h_{ie} + R_E \tag{6.175}$$

Series mixing increases input resistance. Therefore input resistance with feedback is

$$R_{if} = R_i [1 + \beta A]$$

$$= [h_{ie} + R_E] \left[\frac{h_{ie} + (1 + h_{fe}) R_E}{h_{ie} + R_E} \right]$$

$$R_{if} = h_{ie} + (1 + h_{fe}) R_E \tag{6.176}$$

Since $1 + h_{fe} \approx h_{fe}$

$$R_{if} \approx h_{ie} + h_{fe} R_E \tag{6.177}$$

Output Resistance with Feedback

To find the output resistance without feedback, let us reduce the current source to zero in the output circuit of Fig. 6.44. The resulting circuit is shown in Fig. 6.45.

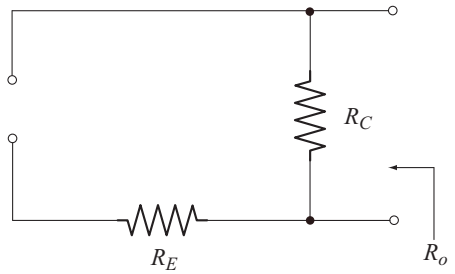


Fig. 6.45 Circuit to find output resistance

From the circuit of Fig. 6.45, the output resistance without feedback is

$$R_o = R_C \tag{6.178}$$

Current sampling increases output resistance. Therefore output resistance with feedback is

$$R_{of} = R_o[1+\beta A]$$

$$R_{of} = R_C\left[\frac{h_{ie}+(1+h_{fe})R_E}{h_{ie}+R_E}\right]$$

$$= R_C\left[\frac{(h_{ie}+R_E)+h_{fe}R_E}{h_{ie}+R_E}\right]$$

or
$$R_{of} = R_C\left[1+\frac{h_{fe}R_E}{h_{ie}+R_E}\right] \quad (6.179)$$

Voltage Gain with Feedback

Voltage gain without feedback is

$$A_V = \frac{V_o}{V_i} = \frac{V_o}{V_s}$$

But
$$V_o = I_o R_C$$

$$\therefore \quad A_V = \left[\frac{I_o}{V_s}\right] R_C \quad (6.180)$$

But
$$A = \frac{I_o}{V_s}$$

$$\therefore \quad A_V = A\,R_C = G_M\,R_C \quad (6.181)$$

Substituting for A from Equation (6.170) we have

$$A_V = \frac{-h_{fe}R_C}{h_{ie}+R_E} \quad (6.182)$$

Using Equation (6.181), the voltage gain with feedback can be written as

$$A_{Vf} = A_f\,R_C = G_{Mf}\,R_C \quad (6.183)$$

Substituting for A_f from Equation (6.174) we have

$$A_{Vf} = \frac{-h_{fe}R_C}{h_{ie}+h_{fe}R_E} \quad (6.184)$$

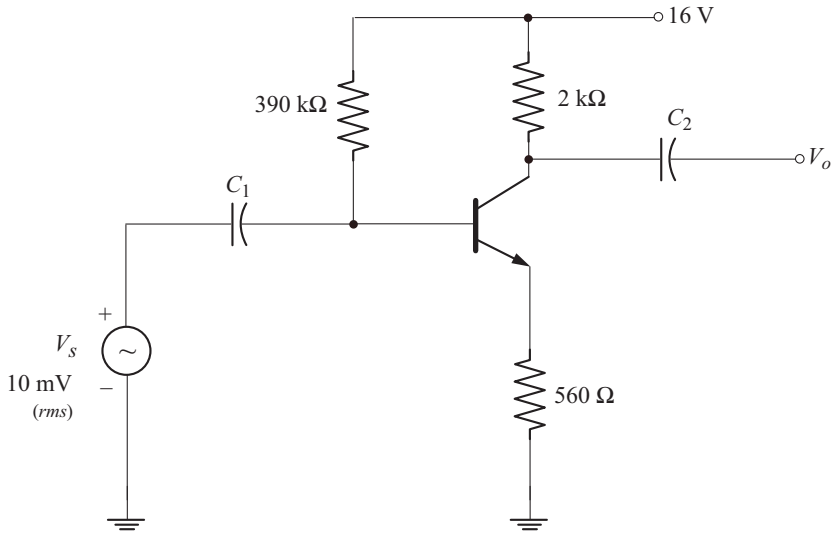
Example 6.16

For the current series feedback amplifier shown below, calculate the following:

(a) Desentisivity factor
(b) Transfer gain with feedback
(c) Voltage gain with and without feedback

(d) Input resistance with and without feedback
(e) Output resistance with and without feedback
(f) Output current with and without feedback
(g) Output voltage with and without feedback

For the transistor used, $h_{fe} = 200$ and $h_{ie} = 2$ kΩ.



(a) Desentisivity factor is

$$D = 1 + \beta A$$

$$\beta = -R_E = -560\ \Omega$$

$$A = G_M = \frac{-h_{fe}}{h_{ie} + R_E}$$

$$= \frac{-200}{2000\ \Omega + 560\ \Omega} = -0.078125\ \text{℧}$$

$$D = 1 + [-560\ \Omega]\ [-0.078125\ \text{℧}] = 44.75$$

(b) Transfer gain with feedback is

$$A_f = G_{Mf} = \frac{A}{D} = \frac{-0.078125\ \text{℧}}{44.75} = -1.745\ \text{m℧}$$

(c) Voltage gain without feedback is

$$A_V = A\,R_C = [-0.078125\ \text{℧}]\ [2\ \text{k}\Omega] = -156.25$$

Voltage gain with feedback is

$$A_{Vf} = A_f\,R_C = (-1.745\ \text{m℧})\ (2\ \text{k}\Omega) = -3.49$$

(d) Input resistance without feedback is

$$R_i = h_{ie} + R_E = 2\ \text{k}\Omega + 560\ \Omega = 2.56\ \text{k}\Omega$$

Input resistance with feedback is

$$R_{if} = h_{ie} + h_{fe} R_E = 2\ \text{k}\Omega + (200)(560\ \Omega) = 114\ \text{k}\Omega$$

Alternatively

$$R_{if} = R_i\ [1 + \beta A\ ] = (2.56\ \text{k}\Omega)\ (44.75) = 114.56\ \text{k}\Omega$$

(e) Output resistance with out feedback is

$$R_o = R_C = 2\ \text{k}\Omega$$

Output resistance with feedback is

$$R_{of} = R_C \left[1 + \frac{h_{fe} R_E}{h_{ie} + R_E}\right]$$

$$= (2\ \text{k}\Omega)\ \left[1 + \frac{(200)\ (560\Omega)}{2\text{k}\Omega + 560\Omega}\right] = 89.5\ \text{k}\Omega$$

Alternatively

$$R_{of} = R_o\ [1 + \beta A] = (2\ \text{k}\Omega)\ (44.75) = 89.5\ \text{k}\Omega$$

(f) Output current without feedback is

$$I_o = A \cdot V_S$$
$$= (-0.078125\ \Omega)\ (10\ \text{mV})$$
$$= -0.78125\ \text{mA (rms)}$$

Output current with feedback is

$$I_o = A_f V_s$$
$$= (-1.745\ \text{m}\mho)\ (10\ \text{mV}) = -17.45\ \mu\text{A (rms)}$$

(g) Output voltage with out feedback is

$$V_o = A_V V_s$$
$$= (-156.25)\ (10\ \text{mV}) = -1.5625\ \text{V}$$

Output voltage with feedback is

$$V_o = A_{Vf} V_s$$
$$= (-3.49)\ (10\ \text{mV})$$
$$= -34.9\ \text{mV (rms).}$$

Note: If h_{ie} is not given, we can find the same using the relation, $h_{ie} = \beta\ r_e = h_{fe} r_e$

where $$r_e = \frac{26\ \text{mV}}{I_E}$$

6.12.4 Voltage-shunt Feedback Amplifier

Figure 6.46 shows the voltage shunt feedback amplifier using an FET. Feed back is given from drain to gate through the feedback resister R_F.

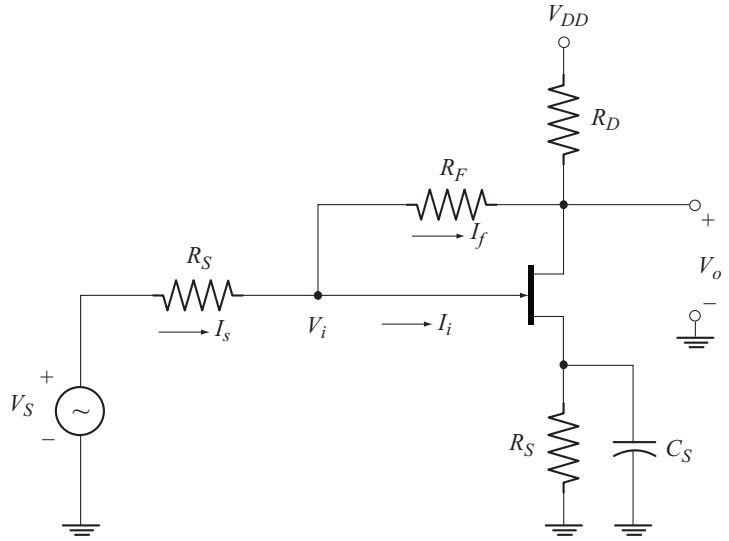


Fig. 6.46 Voltage-shunt feedback amplifier

The feedback current is given by

$$I_f = \frac{V_i - V_o}{R_F} \tag{6.185}$$

Due to voltage amplification,

$$|V_o| \gg |V_i|$$

$$\therefore \quad I_f \approx \frac{-V_o}{R_F} \tag{6.186}$$

The above equation is of the form

$$I_f = \beta V_o \tag{6.187}$$

Comparing the two equations we find that

$$\beta = -\frac{1}{R_F} \tag{6.188}$$

Note that the feedback current is derived from the output voltage. Hence the sampled signal is the output voltage. Also feedback network converts output voltage into feedback current.

Applying KCL at the input node we have

$$I_S = I_i + I_f$$

or

$$I_i = I_S - I_f \tag{6.189}$$

Note that the source current is mixed in shunt with the feedback current. Also the feedback current subtracts from the source current. Hence the feedback is negative.

Since the output voltage is sampled and the feedback current derived from the output voltage is mixed in shunt with source current, the topology is voltage-shunt feedback.

AC Equivalent Circuit of Feedback Amplifier

The ac equivalent circuit of feedback amplifier is obtained by reducing V_{DD} to zero and treating the capacitor C_S as short circuit. The resulting circuit is shown in Fig. 6.47. The voltage source at the input is converted into its equivalent current source.

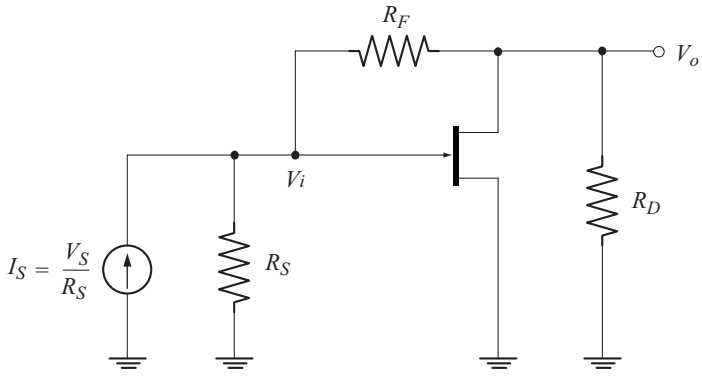


Fig. 6.47 Ac equivalent circuit of voltage-shunt feedback amplifier

Basic Amplifier Circuit without Feedback

The input circuit is obtained by reducing sampling to zero. Since output voltage is sampled, the sampling can be reduced to zero by reducing V_o to zero. This is done by connecting drain terminal to ground. Now as seen from the input side, R_F appears between gate and ground.

The output circuit is obtained by reducing mixing to zero. Since the mixing is shunt, it can be reduced to zero by reducing V_i to zero or connecting gate terminal to ground. Now as seen from the output side R_F appears between drain and ground.

These features are combined to write the basic amplifier circuit with out *feedback* as shown in Fig. 6.48

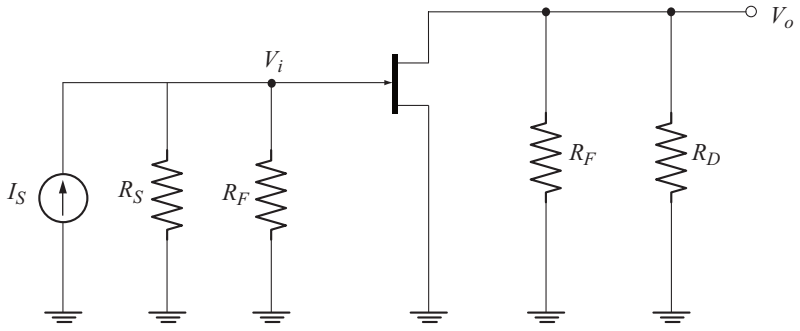


Fig. 6.48 Basic amplifier circuit with out feedback

Let us replace the FET by its small signal model. The resulting circuit is shown in Fig. 6.49.

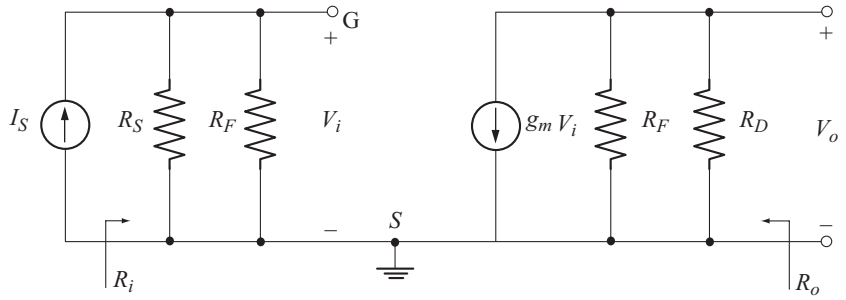


Fig. 6.49 Basic amplifier circuit using small signal model of FET

Transfer Gain with Feedback

Transfer gain with out feedback is given by

$$A = R_M = \frac{V_o}{I_s} \tag{6.190}$$

From the output circuit of Fig. 6.49, we have

$$V_o = -g_m V_i [R_F \| R_D] \tag{6.191}$$

usually $R_F \gg R_D$. As a result

$$R_F \| R_D \approx R_D$$

$$\therefore \quad V_o \approx -g_m V_i R_D \tag{6.192}$$

$$\text{Also} \quad V_i = I_S [R_S \| R_F]$$

Taking $R_S \| R_F \approx R_S$, we have

$$V_i \approx I_S R_S = V_S \tag{6.193}$$

using Equation (6.193) in Equation (6.192) we have

$$V_o = -g_m [I_S R_S] R_D$$

$$\text{Now} \quad A = \frac{V_o}{I_s} = -g_m R_S R_D \tag{6.194}$$

Transfer gain with feedback is given by

$$A_f = R_{Mf}$$

$$= \frac{V_o}{I_s} = \frac{A}{1+\beta A}$$

$$A_f = \frac{-g_m R_D R_S}{1+\left[\frac{-1}{R_F}\right]\left[-g_m R_D R_S\right]}$$

$$A_f = \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S} \tag{6.195}$$

Voltage Gain with Feedback

From Equation (6.192)

$$V_o = -g_m V_i R_D \tag{6.196}$$

Using Equation (6.193) in Equation (6.196) we have

$$V_o = -g_m V_s R_D$$

Now voltage gain without feedback is

$$A_V = \frac{V_o}{V_s} = -g_m R_D \tag{6.197}$$

Voltage gain with feedback is

$$A_{Vf} = \frac{V_o}{V_s}$$

$$= \left[\frac{V_o}{I_s}\right]\left[\frac{I_s}{V_s}\right]$$

$$= [A_f]\left[\frac{1}{R_s}\right] \qquad [\because V_S = I_S R_S]$$

Substituting for A_f from Equation (6.195) we have

$$A_{Vf} = \left[\frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S}\right]\left[\frac{1}{R_S}\right]$$

$$A_{Vf} = \frac{-g_m R_D R_F}{R_F + g_m R_D R_S} \tag{6.198}$$

Input Impedance with Feedback

From the circuit of Fig. 6.49, input impedance without feedback is

$$R_i = R_S \,||\, R_F \tag{6.199}$$

Shunt mixing reduces input impedance. Hence input impedance with feedback is

$$R_{if} = \frac{R_i}{1+\beta A} \tag{6.200}$$

Output Impedance with Feedback

From the circuit of Fig. 6.49, output impedance without feedback is

$$R_o = R_F \| R_D \tag{6.201}$$

Voltage sampling reduces output impedance. Hence output impedance with feedback is

$$R_{of} = \frac{R_o}{1+\beta A} \tag{6.202}$$

Example 6.17

The following data are available for the voltage shunt feedback amplifier of Fig. 6.46.

$g_m = 5$ m℧ $R_D = 5.1$ kΩ $R_S = 1$ kΩ $R_F = 10$ kΩ

Calculate the following:

(a) Transfer gain with and without feedback
(b) Voltage gain with and without feedback
(c) Input impedance with and without feedback
(d) Output impedance with and without feedback

Solution

(a) Transfer gain without feedback is

$$A = -g_m R_D R_S$$
$$= -[5\text{ m℧}][5.1\text{ k}\Omega][1\text{ k}\Omega] = -25.5\text{ k}\Omega$$

Transfer gain with feedback is

$$A_f = \frac{A}{1+\beta A}$$
$$1+\beta A = 1 + \left[\frac{-1}{10\text{k}\Omega}\right][-25.5\text{ k}\Omega] = 3.55$$
$$A_f = \frac{-25.5\text{k}\Omega}{3.55} = -7.18\text{ k}\Omega$$

(b) Voltage gain with out feedback is

$$A_V = -g_m R_D = -[5\text{ m℧}][5.1\text{ k}\Omega] = -25.5$$

Voltage gain with feedback is

$$A_{Vf} = \frac{A_f}{R_S} = \frac{-7.18\text{k}\Omega}{1\text{k}\Omega} = -7.18$$

(c) Input impedance with out feedback is

$$R_i = R_S \| R_F = 1\text{ k}\Omega \| 10\text{ k}\Omega = 0.909\text{ k}\Omega$$

Input impedance with feedback is

$$R_{if} = \frac{R_i}{1+\beta A} = \frac{0.909\,\text{k}\Omega}{3.55} = 256\ \Omega$$

(d) output impedance with out feedback is

$$R_o = R_D \| R_F = 5.1\ \text{k}\Omega \| 10\ \text{k}\Omega = 3.37\ \text{k}\Omega$$

output impedance with feedback is

$$R_{of} = \frac{R_o}{1+\beta A} = \frac{3.37\text{k}\Omega}{3.55} = 0.949\ \text{k}\Omega$$

Exercise Problems

6.1 A feedback amplifier has a gain $A = -1000$. Calculate the gain with feedback if 10% negative feedback is given.

6.2 An amplifier has a gain of – 200 and gain variation of 15%. Calculate the gain variation if 20% negative feedback is given.

6.3 A voltage series negative feedback amplifier has the following data.
$A = -1000$ $R_i = 2\ \text{k}\Omega$ $R_o = 25\ \text{k}\Omega$.
If 20% negative feedback is given, calculate the values of A_f, R_{if} and R_{of}.

6.4 An FET voltage series feedback amplifier has the following data.
$R_1 = 500\ \text{k}\Omega$ $R_2 = 1\ \text{k}\Omega$ $R_o = 30\ \text{k}\Omega$ $R_D = 10\ \text{k}\Omega$ and $g_m = 4000\ \mu\text{S}$.
Calculate A_V and A_{Vf}.

6.5 A transistor current series feedback amplifier has the following data.
$R_B = 50\ \text{k}\Omega$ $R_C = 2.7\ \text{k}\Omega$ $R_E = 600\ \Omega$ $V_{CC} = 15\ \text{V}$ $h_{fe} = 200$ $h_{ie} = 1000\ \Omega$.
Calculate A_V and A_{Vf}.

6.6 An FET Voltage shunt feedback amplifier has the following data.
$R_S = 1.2\ \text{k}\Omega$ $R_F = 15\ \text{k}\Omega$ $R_D = 10\ \text{k}\Omega$ $g_m = 10\ \text{mS}$.
Calculate A_V and A_{Vf}.

Chapter 7

Power Amplifiers

A power amplifier in a stereo, radio or television system is intended to deliver a large voltage and current in to a low impedance load such as a loud speaker. In a stereo system the voltage level of a small signal from a radio tuner, tape player or compact disc is first amplified by the input stage of power amplifier which is called the driver. The output voltage of the driver then drives the output stage which is a current amplifier. Due to large voltage and current swings in a power amplifier, the non-linearity of the amplifying device is an importnat consideration. Besides this, conversion efficiency is also of prime concern since the power amplifier converts the dc power of the supply voltage to the ac power delivered to the load. This chapter discusses the various classes of operation, power dissipation and non linear distortion resulting from large signal operation.

◆ 7.1 CLASSIFICATION OF POWER AMPLIFIERS

Power amplifiers are classified based on the location of the quiescent operating point or *Q*-point on the dc load line as follows:

1. Class A power amplifiers.
2. Class B power amplifiers.
3. Class AB power amplifiers.
4. Class C power amplifiers.

A class D amplifier is another class of power amplifier, which is designed to operate with digital or pulse type signals.

7.1.1 Class A Power Amplifier

In class A power amplifier, the *Q*-point is located at the centre of the load line as shown in Fig. 7.1, so that the output signal varies over the full cycle of the input signal.

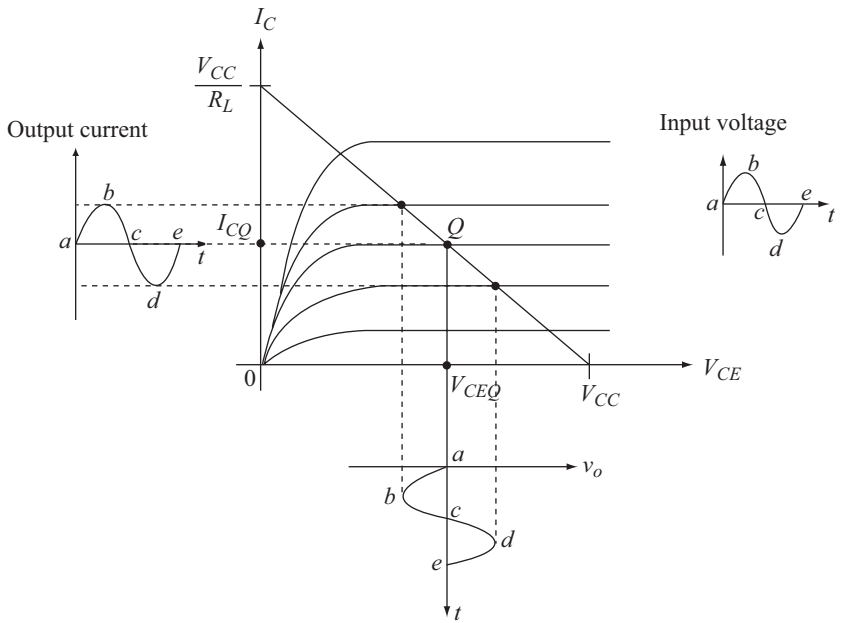


Fig. 7.1 Input-output waveforms for a class A power amplifier

7.1.2 Class B Power Amplifier

In class B power amplifier, the *Q*-point is located at cut-off as shown in Fig. 7.2, so that the output signal varies over one half cycle of the input signal.

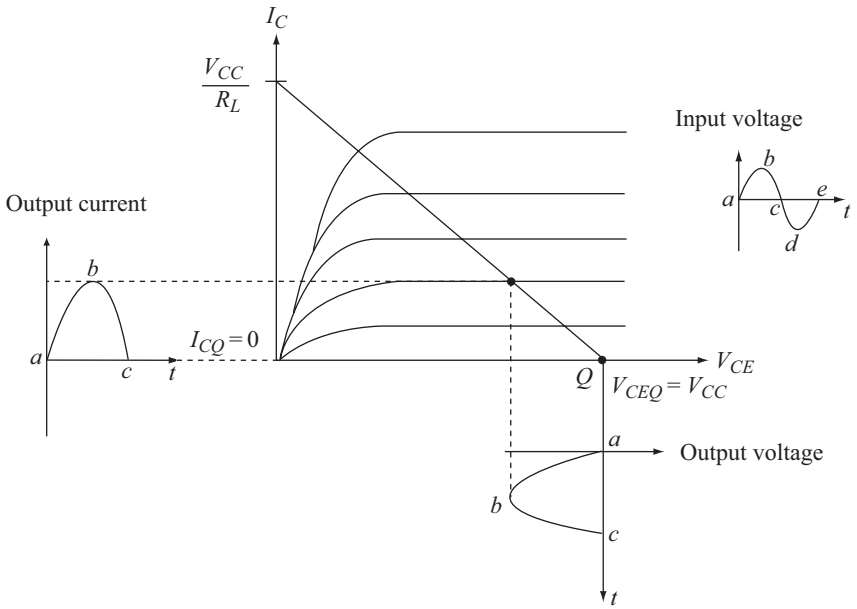


Fig. 7.2 Input-output waveforms for a class B power amplifier

Observe that a single class B amplifier provides only one half-cycle at the output. Thus, a second class B amplifier is used to obtain the amplified output of the other half-cycle. These two amplifiers would then be combined to obtain an amplified output of the full-cycle of the input signal. Such a combination is called a *push-pull configuration*.

7.1.3 Class AB Power Amplifier

We saw in Section 7.1.2 that the *Q*-point of a class B amplifier is at $V_{CE} = V_{CC}$ and $I_C = 0$ mA. This implies that the transistor is at zero bias. The base-emitter junction of the transistor will be forward-biased and the transistor brought into the active region only when the input voltage exceeds the cut-in voltage, V_γ of the base-emitter junction. During the periods when $v_i < V_\gamma$ the output current will be zero as shown in Fig. 7.3.

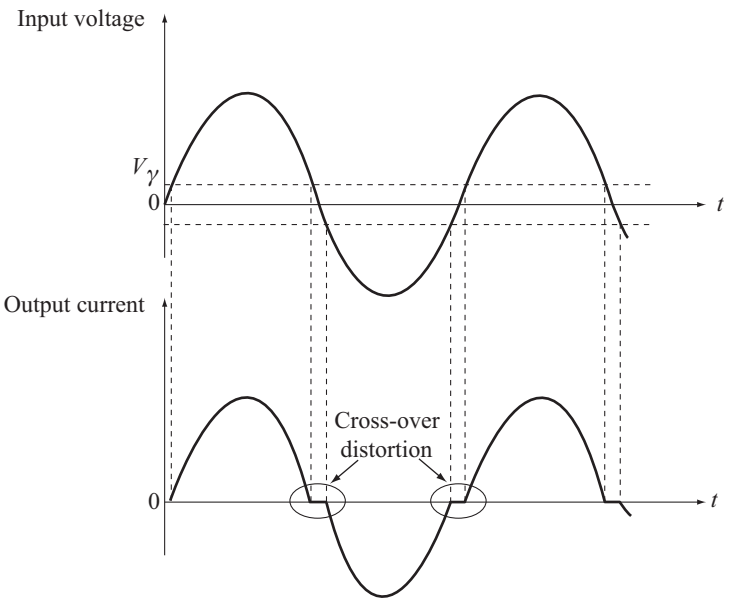


Fig. 7.3 Cross-over distortion in class B push-pull amplifier

The output waveform is not an exact replica of the input waveform. i.e., the output signal is distorted. Observe that the distortion occurs at every zero-crossing of the input signal. Hence, the distortion is called cross-over distortion.

This can be overcome by locating the operating point slightly above cut-off. Since, the *Q*-point is located slightly above cut-off as in class B amplifier but much below the centre of the dc load line as in class A amplifier, these amplifiers are referred to as class AB Power Amplifiers.

7.1.4 Class C Power Amplifier

In class C power amplifier, the transistor is biased below cut-off. Let the extent of reverse-bias be V_{BB}. The transistor operates in the active region and a current flows only for $v_i > V_{BB} + V_\gamma$, where V_γ is the cut-in voltage of the base-emitter junction. The current would then be pulses of short duration as shown in Fig. 7.4.

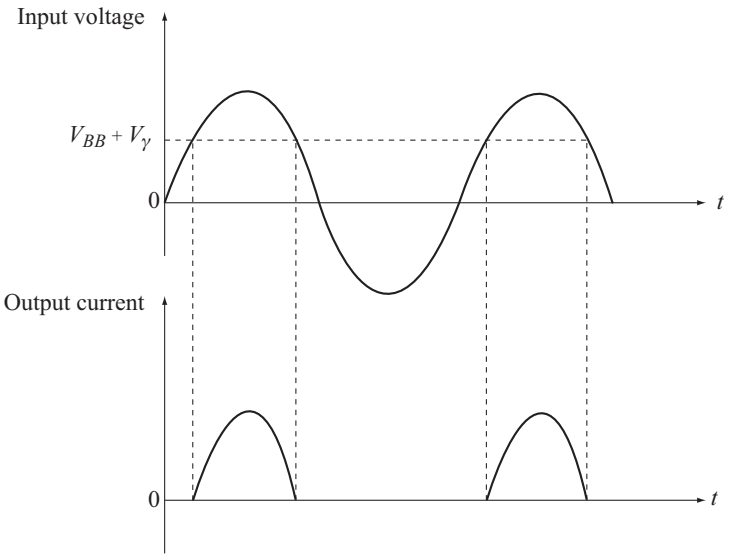


Fig. 7.4 Current pulses in class C power amplifier

Observe that the output current flows for less than one half-cycle of the input signal. The full-cycle of the input signal is obtained at the output by the use of a tuned circuit at the collector as shown in Fig. 7.5.

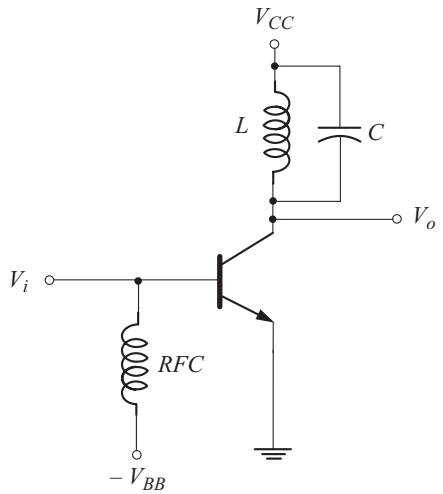


Fig. 7.5 Tuned class C power amplifier

A periodic sinusoidal input signal will produce a periodic non-sinusoidal output current. By Fourier analysis, we know that a non-sinusoidal periodic waveform consists of the fundamental sinusoidal component (whose frequency is same as the frequency of non-sinusoidal periodic waveform) and its harmonics. When this current is passed through the *LC* circuit, which is tuned

to the fundamental frequency, it produces the full amplified fundamental signal at the output. Observe that this is a single frequency amplifier depending on the values of L and C. The resonant frequency is given by

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{7.1}$$

The values of L and C are selected such that the resonant frequency is equal to the fundamental frequency.

Class C amplifiers are thus used only in communication circuits, where frequency selection is important. The negative bias is applied through a radio frequency coil to isolate the high-frequency input signal and the dc bias source.These discussions are summarized in Table 7.1.

Table 7.1 Operating cycle of various power-amplifiers

Class / *Parameter*	*A*	*B*	*AB*	*C*
Operating cycle	360°	180°	180°	< 180°

◆ 7.2 CLASS A POWER AMPLIFIER

Depending on how the load is connected at the amplifier output, we have two types of class A power amplifiers as given below.

1. Series-fed Class A power amplifier.
2. Transformer-coupled Class A power amplifier.

7.2.1 Series-fed Class A Power Amplifier

A fixed-bias series-fed class A power amplifier is shown in Fig. 7.6.

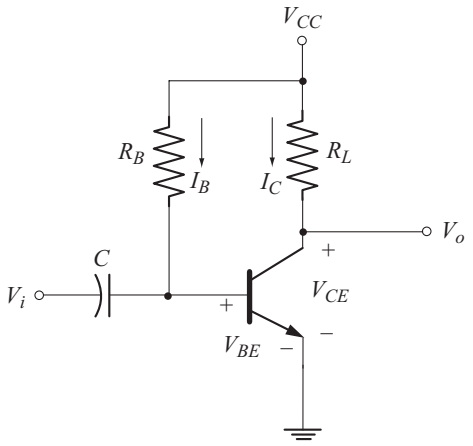


Fig. 7.6 Series-fed class A power amplifier

This circuit is called a series-fed amplifier because the load R_L is connected in series with the collector.

Since R_L is in the collector circuit, it can as well be denoted by R_C.

DC Analysis

From Fig. 7.6, the base current

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{7.2}$$

and the collector current

$$I_C = \beta I_B \tag{7.3}$$

where β is the dc current gain of the transistor in the CE configuration.

Applying KVL to the collector-emitter circuit, we have

$$V_{CC} = I_C R_L + V_{CE} \tag{7.4}$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{CE}}{R_L} \tag{7.5}$$

Equation (7.5) can be written as

$$I_C = \left(-\frac{1}{R_L}\right) V_{CE} + \frac{V_{CC}}{R_L} \tag{7.6}$$

where the equation of the dc load is in the slope-intercept form.

Thus, the slope of the dc loadline is $\left(-\frac{1}{R_L}\right)$ and the intercept on the current axis is $\frac{V_{CC}}{R_L}$ as shown in Fig. 7.7.

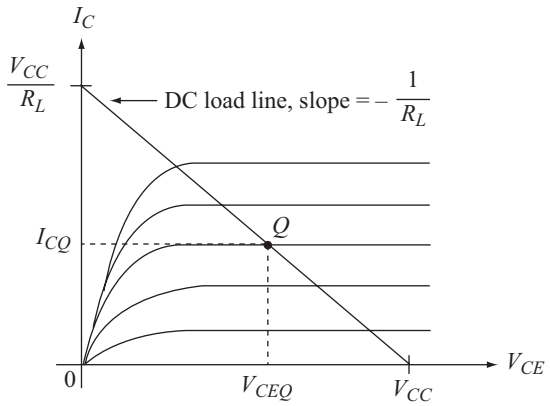


Fig. 7.7 DC load line of class A series-fed power amplifier

AC Analysis

In the circuit of Fig. 7.6, both the dc current and the ac current flows through the same load R_L connected in series with the collector. Hence, the ac load line is the same as the dc load line. The output voltage and current excursions of the series-fed Class A power amplifier is shown in Fig. 7.8.

Observe in Fig. 7.8 that as the amplitude of the input signal increases, the amplitude of the output current as well as the output voltage increases to a maximum extent bounded by

$$0 \text{ and } \frac{V_{CC}}{R_L} \text{ for output current}$$

and

$$0 \text{ and } V_{CC} \text{ for output voltage.}$$

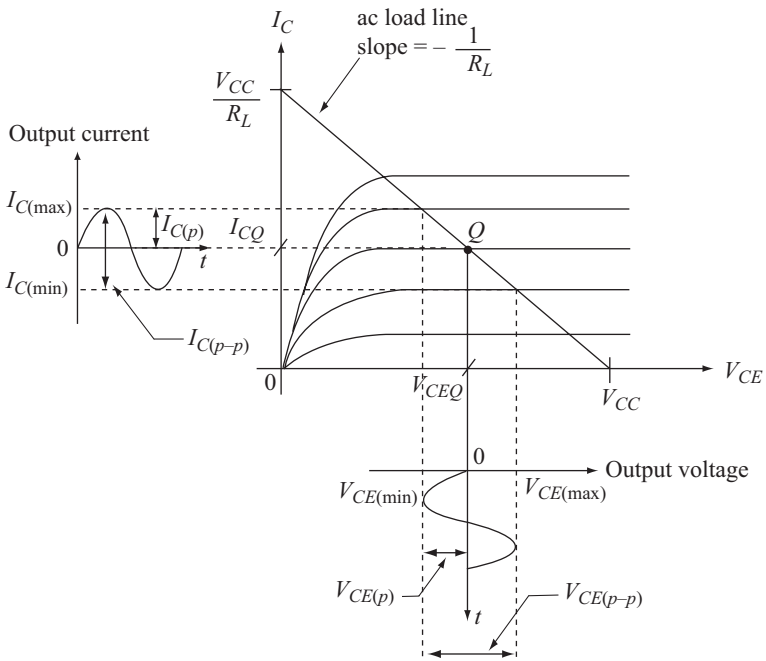


Fig. 7.8 Output voltage and current excursions of the series-fed class A power amplifier

Power Considerations

For the power amplifier, the input power is supplied from the dc source V_{CC}.

$\therefore$ The dc power input is given by

$$P_{i(dc)} = V_{CC} I_{CQ}$$

The dc power $P_{i(dc)}$, will be continuously drawn from the supply V_{CC} regardless of whether the ac input signal is present or not. The circuit operates with low efficiency due to continuous power dissipation in the collector circuit.

The ac output power delivered to the load can be expressed in the following ways:

Using RMS Values

The ac power delivered to the load is given by

$$P_{o(\text{ac})} = V_{CE(\text{rms})} I_{C(\text{rms})} \tag{7.7}$$

But $$I_{C(\text{rms})} = \frac{V_{CE(\text{rms})}}{R_L} \text{ or } V_{CE(\text{rms})} = I_{C\,(\text{rms})} R_L$$

Using these relations in Equation (7.7), the ac output power can be expressed as

$$P_{o(\text{ac})} = \frac{V^2_{CE(\text{rms})}}{R_L} \tag{7.8}$$

or $$P_{o(\text{ac})} = I^2_{C(\text{rms})} R_L \tag{7.9}$$

Using Peak Values

We know that, $$V_{CE(\text{rms})} = \frac{V_{CE(p)}}{\sqrt{2}} \text{ and } I_{C\,(\text{rms})} = \frac{I_{C(p)}}{\sqrt{2}}$$

where $V_{CE(p)}$ = peak load voltage
and $I_{C(p)}$ = peak load current

Using these relations in Equation (7.7) we have

$$P_{o(\text{ac})} = \frac{V_{CE(p)}}{\sqrt{2}} \cdot \frac{I_{C(p)}}{\sqrt{2}}$$

$$= \frac{V_{CE(p)} I_{C(p)}}{2} \tag{7.10}$$

But $$V_{CE\,(p)} = I_{C\,(p)} R_L \quad \Rightarrow \quad I_{C\,(p)} = \frac{V_{CE(p)}}{R_L}$$

Using these relations in Equation (7.10) we have

$$P_{o(\text{ac})} = \frac{V^2_{CE(p)}}{2 R_L} \tag{7.11}$$

or $$P_{o(\text{ac})} = \frac{I^2_{C(p)}}{2} R_L \tag{7.12}$$

Using Peak-to-peak Values

The peak-to-peak load voltage is

$$V_{CE(p-p)} = 2\, V_{CE(p)} \quad \Rightarrow \quad V_{CE(p)} = \frac{V_{CE(p-p)}}{2}$$

and the peak-to-peak load current is

$$I_{C\,(p-p)} = 2\,I_{C(p)} \quad \Rightarrow \quad I_{C(p)} = \frac{I_{C(p-p)}}{2}$$

Using these relations in Equation (7.10) we have

$$P_{o(\text{ac})} = \frac{V_{CE(p-p)}\,I_{C(p-p)}}{8} \tag{7.13}$$

Equation (7.11) can be rewritten as

$$P_{o(\text{ac})} = \frac{V^2_{CE(p-p)}}{8\,R_L} \tag{7.14}$$

and from Equation (7.12) we have

$$P_{o(\text{ac})} = \frac{I^2_{C(p-p)}}{8}\,R_L \tag{7.15}$$

Using Maximum and Minimum Values

From Fig. 7.8

$$V_{CE(p-p)} = V_{CE(\max)} - V_{CE(\min)} \tag{7.16}$$

$$I_{C(p-p)} = I_{C(\max)} - I_{C(\min)} \tag{7.17}$$

Using these relations in Equation (7.13) we have

$$P_{o(\text{ac})} = \frac{[V_{CE(\max)} - V_{CE(\min)}][I_{C(\max)} - I_{C(\min)}]}{8} \tag{7.18}$$

Maximum ac Output Power

From Equation (7.18)

$P_{o(\text{ac})}$ is maximum, when

$$\left.\begin{aligned} V_{CE(\min)} &= 0 \qquad I_{C(\min)} = 0 \\ V_{CE(\max)} &= V_{CC} \qquad I_{C(\max)} = \frac{V_{CC}}{R_L} \end{aligned}\right\} \tag{7.19}$$

Substituting in Equation (7.18)

$$P_{o(\text{ac})\max} = \frac{V_{CC}}{8} \cdot \frac{V_{CC}}{R_L}$$

or

$$P_{o(\text{ac})\max} = \frac{V^2{}_{CC}}{8R_L} \tag{7.20}$$

This equation can be used to select the value of V_{CC} for a desired power output and a given load.

Note that in the analysis, we have assumed that the transistor is linear and thus both the input and output signals are purely sinusoidal.

The merits of the amplifier are that it is simple and no coupling element is required. The serious **drawbacks** however are

- There is an impedance mismatch between the power amplifier and the load.
- It has very poor conversion efficiency (see section 7.5.1)
- Most often, the load for power amplifier is the loud speaker which is basically a magnetic circuit. In the series-fed amplifier, both ac and dc current would flow through this magnetic load resulting in core saturation.

Example 7.1

A class A series-fed power amplifier is required to deliver a maximum power of 20 W to a load of 4 Ω. Calculate the required supply voltage.

Solution

Given,

$$P_{o(\text{ac})\max} = 20 \text{ W} \quad R_L = 4\ \Omega$$

From Equation (7.20)

$$P_{o(\text{ac})\max} = \frac{V^2_{CC}}{8R_L}$$

$$\therefore \quad V_{CC} = \sqrt{8 P_{o(\text{ac})\max} R_L}$$

$$= \sqrt{8 \times 20 \times 4} = \sqrt{640} = 25.29 \text{ V}$$

$$V_{CC} = 25.29 \text{ V}$$

7.2.2 Transformer-Coupled Class A Power Amplifier

This is also referred to often as the transformer-coupled audio power amplifier. We saw that one of the serious drawbacks of the series-fed power amplifier was impedance mismatch.

Impedance Matching using Transformer

Consider the output equivalent circuit of the series fed class A power amplifier shown in Fig. 7.9.

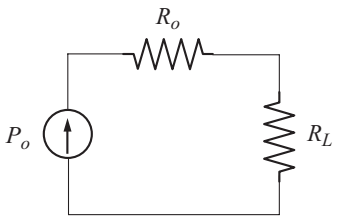


Fig. 7.9 Output equivalent circuit of series-fed class A power amplifier

P_o represents the ac power developed at the output of power amplifier and R_o is its output resistance.

For transistor amplifier, $R_o \approx \dfrac{1}{h_{oe}}$ which is of the order of kilo ohms. But the typical load for an audio power amplifier is loud speaker whose impedance is of the order of 5 to 50 Ω.

We know from the maximum power transfer theorem that maximum power is transferred to the load when $R_L = R_o$. This is not the case in audio amplifiers, resulting in a reduced power being delivered to the load because of impedance mismatch. For maximum power transfer, the value of R_L needs to be boosted to the value of R_o. This is called impedance transformation which can be done using a transformer. Impedance transformation can be explained with Fig. 7.10 .

In Fig. 7.10,

V_1 = primary voltage
V_2 = secondary voltage
I_1 = primary current
I_2 = secondary current

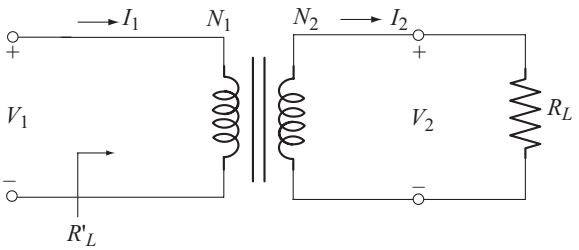


Fig. 7.10 Impedance transformation using transformer

Load on the secondary,

$$R_L = \frac{V_2}{I_2} \tag{7.21}$$

$$R_L' = \frac{V_1}{I_1} \tag{7.22}$$

where R_L' is the load reflected at the primary.

For the transformer

$$\frac{V_1}{V_2} = \frac{N_1}{N_2} \tag{7.23}$$

and

$$\frac{I_2}{I_1} = \frac{N_1}{N_2} \tag{7.24}$$

Multiplying Equations (7.23) and (7.24)

$$\frac{V_1 I_2}{V_2 I_1} = \frac{N_1^2}{N_2^2} \tag{7.25}$$

$$\frac{V_1 / I_1}{V_2 / I_2} = \left(\frac{N_1}{N_2}\right)^2 \tag{7.26}$$

Substituting Equations (7.21) and (7.22) in Equation (7.26), we have

$$\frac{R_L'}{R_L} = \left(\frac{N_1}{N_2}\right)^2$$

or
$$R_L' = R_L \left(\frac{N_1}{N_2}\right)^2 \tag{7.27}$$

$R_L' > R_L$ can be achieved by choosing $N_1 > N_2$. i.e., we have to use a step down transformer of appropriate turns ratio.

Analysis of Amplifier Stage

A transformer-coupled class A power amplifier is shown in Fig. 7.11(a).

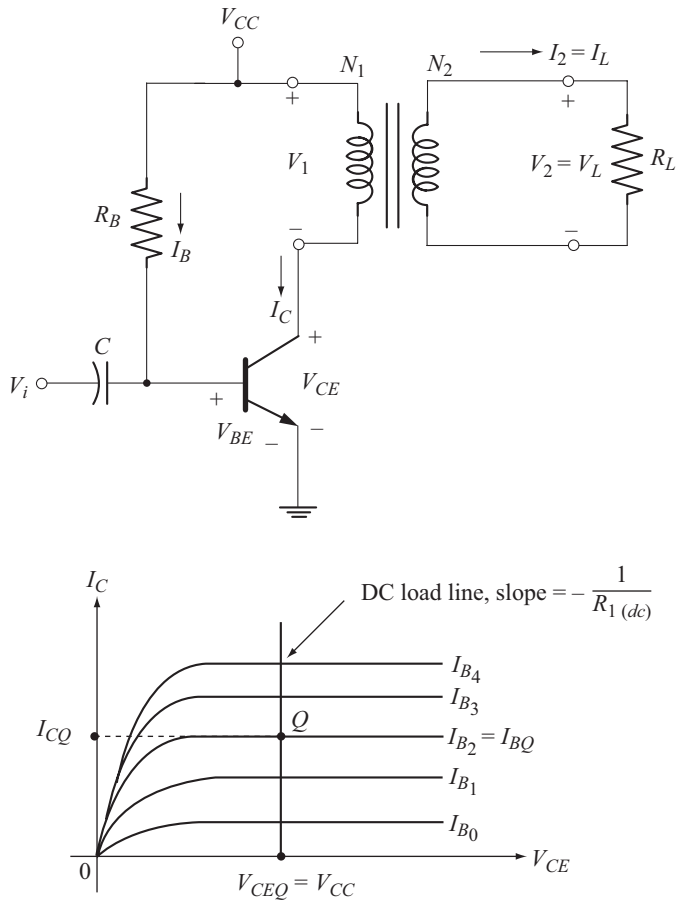


Fig. 7.11 Transformer-coupled power amplifier
(a) Circuit (b) DC load line

DC Analysis

Applying KVL to the collector- emitter circuit of Fig. 7.11 (a), we have,

$$V_{CC} = I_C R_{1\,(dc)} + V_{CE} \tag{7.28}$$

where $R_{1\,(dc)}$ is the dc resistance of the primary winding of the transformer.

Equation (7.28) can be re-written as

$$I_C R_{1\,(dc)} = V_{CC} - V_{CE} \tag{7.29}$$

$$\therefore \quad I_C = \left(-\frac{1}{R_{1\,(dc)}}\right) V_{CE} + \frac{V_{CC}}{R_{1\,(dc)}} \tag{7.30}$$

which is the equation of the dc load line in the slope-intercept form, with slope = $-\frac{1}{R_{1\,(dc)}}$ and current-axis intercept $\frac{V_{CC}}{R_{1\,(dc)}}$. Since, the dc resistance of the transformer will be very low of the order of a few ohms, the slope is close to ∞ and the dc load line will be almost vertical as shown in Fig. 7.11(b).

Observe in Equation (7.28) that $I_C R_{1\,(dc)}$ will be close to zero and therefore $V_{CE} = V_{CC}$.

The intersection of the dc load line and the base current set by the biasing circuit defines the operating point as illustrated in Fig. 7.11(b) for $I_{B_2} = I_{BQ}$.

AC Analysis

The ac load line has a slope of $-\frac{1}{R'_L}$, passing through the *Q*-point as shown in Fig. 7.12.

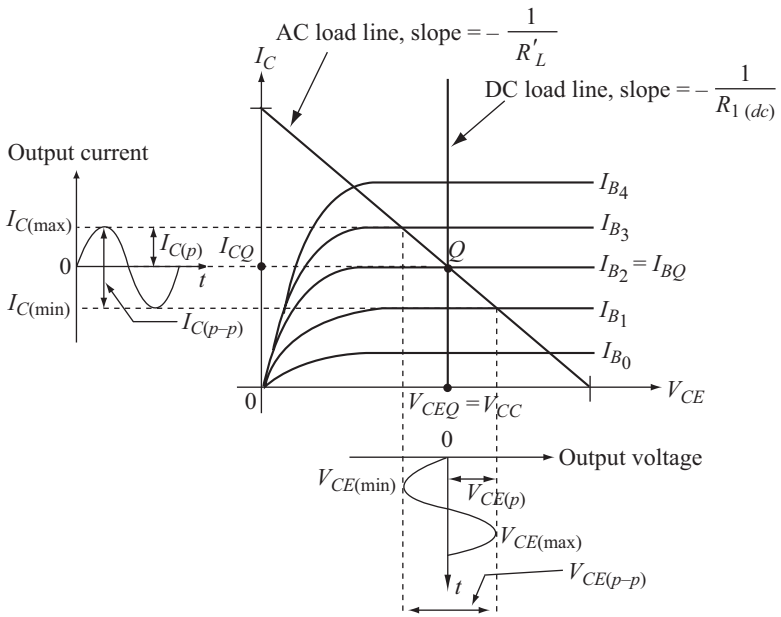


Fig. 7.12 The ac load line with output voltage and current variations in a transformer-coupled class A power amplifier

From Fig. 7.12, it is clear that the maximum output voltage at the primary will exceed V_{CC}. Thus, it is necessary to ensure that the possible voltage swings do not exceed the transistor voltage ratings.

The dc power drawn by the circuit is given by

$$P_{i(dc)} = V_{CC} I_{CQ} \tag{7.31}$$

Let us assume that the efficiency of the transformer is 100 percent so that the ac power developed in the collector circuit or the primary of the transformer equals the ac power delivered to the load on the secondary side.

From Equation (7.10), the ac power developed across the primary is given by

$$P_{o(\text{ac})} = \frac{V_{CE(p)} I_{C(p)}}{2} \tag{7.32}$$

From Fig. 7.12,

$$V_{CE(\max)} = V_{CC} + V_{CE(p)} \tag{7.33}$$

and $$V_{CE(\min)} = V_{CC} - V_{CE(p)} \tag{7.34}$$

Adding Equations (7.33) and (7.34) we get

$$V_{CE(\max)} + V_{CE(\min)} = 2\, V_{CC}$$

or $$V_{CC} = \frac{V_{CE(\max)} + V_{CE(\min)}}{2} \tag{7.35}$$

Subtracting Equations (7.33) and (7.34), we get

$$V_{CE(\max)} - V_{CE(\min)} = 2\, V_{CE(p)} = V_{CE(p\text{-}p)}$$

or $$V_{CE(p)} = \frac{V_{CE(\max)} - V_{CE(\min)}}{2} = \frac{V_{CE(p-p)}}{2} \tag{7.36}$$

similarly $$I_{C(p)} = \frac{I_{C(\max)} - I_{C(\min)}}{2} = \frac{I_{C(p-p)}}{2} \tag{7.37}$$

Using these relations in Equation (7.32) we get

$$P_{o(\text{ac})} = \frac{[V_{CE(\max)} - V_{CE(\min)}][I_{C(\max)} - I_{C(\min)}]}{8} \tag{7.38}$$

or $$P_{o(\text{ac})} = \frac{V_{CE(p-p)} I_{C(p-p)}}{8} \tag{7.39}$$

But $$I_{C(p\text{-}p)} = \frac{V_{CE(p-p)}}{R_L'} \quad \Rightarrow \quad V_{CE(p\text{-}p)} = I_{C(p\text{-}p)} R_L'$$

Using these relations in Equation (7.39) we have

$$P_{o(\text{ac})} = \frac{V^2_{CE(p-p)}}{8R_L'} = \frac{V^2_{CE(p)}}{2R_L'} \tag{7.40}$$

$$\text{or} \qquad P_{o(\text{ac})} = \frac{I^2_{C(p-p)}}{8} R'_L = \frac{I^2_{C(p)}}{2} R'_L \tag{7.41}$$

AC Power Delivered to the Load

The ac power delivered to the load on the secondary side is

$$P_L = V_{L(\text{rms})} I_{L(\text{rms})} \tag{7.42}$$

$$\text{Using} \qquad I_{L(\text{rms})} = \frac{V_{L(\text{rms})}}{R_L}$$

$$P_L = \frac{V^2_{L(\text{rms})}}{R_L} \tag{7.43}$$

$$\text{or} \qquad P_L = I^2_{L\,(\text{rms})} R_L \tag{7.44}$$

The load current $I_{L(\text{rms})}$ can be obtained from

$$\frac{I_{L(\text{rms})}}{I_{C(\text{rms})}} = \frac{N_1}{N_2} \qquad [\because I_{L(\text{rms})} = I_{2(\text{rms})}]$$

$$\text{or} \qquad I_{L(\text{rms})} = \frac{N_1}{N_2} I_{C\,(\text{rms})} \tag{7.45}$$

Since we have assumed ideal transformer for which the efficiency is 100 percent,

$$P_L = P_{o(\text{ac})} \tag{7.46}$$

If the transformer is not ideal, P_L and $P_{o(\text{ac})}$ are related by

$$P_L = \eta_{\text{TFR}} P_{o(\text{ac})} \tag{7.47}$$

where η_{TFR} is the efficiency of the transformer.

Maximum ac Output Power

From Equation (7.38), we find that the ac output power $P_{o(\text{ac})}$ is maximum when $V_{CE(\text{min})} = 0$ and $I_{C(\text{min})} = 0$

$$\text{Thus,} \qquad P_{o(\text{ac})\,\max} = \frac{V_{CE(\text{max})} I_{C(\text{max})}}{8}$$

$$\text{Using} \qquad I_{C\,(\text{max})} = \frac{V_{CE(\text{max})}}{R'_L}, \quad \text{we have}$$

$$P_{o(\text{ac})\,\max} = \frac{V^2_{CE(\text{max})}}{8R'_L} \tag{7.48}$$

From Equation (7.35),

$$\text{with} \qquad V_{CE\,(\text{min})} = 0, \quad \text{we get}$$

$$V_{CE(\text{max})} = 2\,V_{CC}$$

Using this relation in Equation (7.48) we have

$$P_{o(\text{ac})\max} = \frac{V_{CC}^2}{2R'_L} \tag{7.49}$$

Example 7.2

A class A transformer coupled audio power amplifier is requird to deliver a maximum of 1 W into a loud speaker of 10 Ω resistance. If the output resistance of the amplifier is 1000 Ω, calculate

(a) Turns ration of the transformer required
(b) Power supply voltage
Assume an ideal transformer (100 % efficiency)

Solution

Given

$$P_{o(\text{ac})\ \max} = 1\ \text{W} \quad R_L = 10\ \Omega \quad R_o = 1000\ \Omega$$

(a) From Equation (7.27)

$$R'_L = R_L \left(\frac{N_1}{N_2}\right)^2$$

$$\therefore \quad \left(\frac{N_1}{N_2}\right)^2 = \frac{R'_L}{R_L}$$

For maximum power transfer,

$$R'_L = R_o$$

$$\therefore \quad \frac{N_1}{N_2} = \sqrt{\frac{R_o}{R_L}} = \sqrt{\frac{1000}{10}} = 10$$

or $\quad N_1 : N_2$ is 10:1

A 10:1 step down transformer is to be used.

(b) From Equation (7.49)

$$P_{o\ (\text{ac})\ \max} = \frac{V_{CC}^2}{2R'_L} = \frac{V_{CC}^2}{2R_o}$$

$$\therefore \quad V_{CC} = \sqrt{2R_o\, P_{o(\text{ac})\max}}$$

$$= \sqrt{2 \times 1000 \times 1}$$

$$V_{CC} = 44.7\ \text{V}$$

Let $\quad V_{CC} = 45\ \text{V}$

Example 7.3

Repeat Example 7.2, if the transformer efficiency is 75%.

Solution

Given,

$$P_{o(\text{ac})\,\max} = 1\text{W} \quad R_L = 10\ \Omega \quad R_o = 1000\ \Omega \quad \text{Transformer efficiency} = 75\ \%$$

(a) Transformer turns ratio is 10 as before.

(b) $P_{o(\text{ac})\max}$ represents the maximum ac power developed in the primary of the transformer.

It is required to deliver 1 W of power in the load connected to the secondary.

$$\text{Therefore,}\quad P_{o(\text{ac})\max} = \frac{\text{Power delivered to } R_L}{\text{Transformer efficiency}} = \frac{1\text{W}}{0.75} = \frac{4}{3}\ \text{W}$$

$$\therefore \qquad V_{CC} = \sqrt{2R_o\, P_{o(\text{ac})\max}} = \sqrt{2\times 1000\times\frac{4}{3}} = 51.64\ \text{V}$$

$$\text{Let} \qquad V_{CC} = 52\ \text{V}.$$

Observe that a higher supply voltage is required if the transformer is not ideal.

Example 7.4

A load of 10 Ω is connected between the secondary terminals of a 20:1 transformer. Calculate the effective resistance seen looking into the primary terminals.

Solution

$$R_L' = \left(\frac{N_1}{N_2}\right)^2 R_L$$

$$= (20)^2\ (10\ \Omega)$$

$$= 4\ \text{k}\Omega$$

Example 7.5

Find the turns ratio of the transformer required to match a 6 Ω speaker load so that the effective load resistance seen at the primary is 8 kΩ?

Solution

$$R_L' = \left(\frac{N_1}{N_2}\right)^2 R_L$$

$$\frac{N_1}{N_2} = \sqrt{\frac{R_L'}{R_L}} = \sqrt{\frac{8\,\text{k}\Omega}{6\,\Omega}} = 36.51$$

7.3 HARMONIC DISTORTION OR NON LINEAR DISTORTION

So far we have assumed that the transistor is linear. However, the dynamic transfer characteristic is non linear as shown in Fig (a). The non-linearity arises because the static output characteristics are not equidistant straight lines for constant increments in the input excitation. If the dynamic transfer curve is nonlinear over the signal excursion range, the output will not be sinusoidal when the input is sinusoidal. This type of distortion is called non-linear distortion or harmonic distortion.

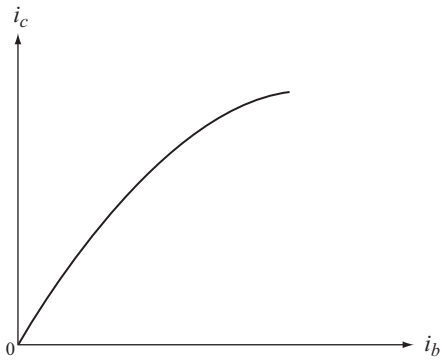


Fig. (a) Dynamic transfer characteristics of a transistor

In the presence of non linearity, the input-output relation can be expressed as

$$i_c = G_1 i_b + G_2 i_b^2 + G_3 i_b^3 + \cdots \quad \text{(A)}$$

where the first term represents the linear term followed by the non-linear terms. For instance if the input is sinusoidal of large amplitude, say

$$i_b = I_{bm} \sin \omega t \quad \text{(B)}$$

Then Equation (A) becomes

$$i_c = G_1 I_{bm} \sin\omega t + G_2 I_{bm}^2 \sin^2 \omega t + G_3 I_{bm}^3 \sin^3 \omega t + \cdots$$

which can be expressed in the general form as

$$i_c = B_0 + B_1 \sin\omega t + B_2 \sin 2\omega t + B_3 \sin 3\omega t + \cdots \quad \text{(C)}$$

In Equation (C)

- B_0 is the dc term
- $B_1 \sin \omega t$ is the fundamental component whose frequency is same as the input frequency (i.e ω)
- $B_2 \sin 2\omega t$ is the second harmonic component whose frequency is twice the input frequency (i.e. 2ω)
- $B_3 \sin 3\omega t$ is the third harmonic component whose frequency is thrice the input frequency (i.e. 3ω) and so on.

ω is called the fundamental frequency, 2 ω the second harmonic frequency, 3 ω the third harmonic frequency and so on.

Since the non-linearity of the dynamic transfer characteristics of the transistor results in the generation of harmonics of the input frequency, the distortion is termed non-linear distortion or harmonic distortion.

The Fourier analysis of the output signal reveals that as the order of the harmonic increases, its amplitude decreases

i.e., $$| B_1 | > | B_2 | > | B_3 | > \cdots \quad \text{(D)}$$

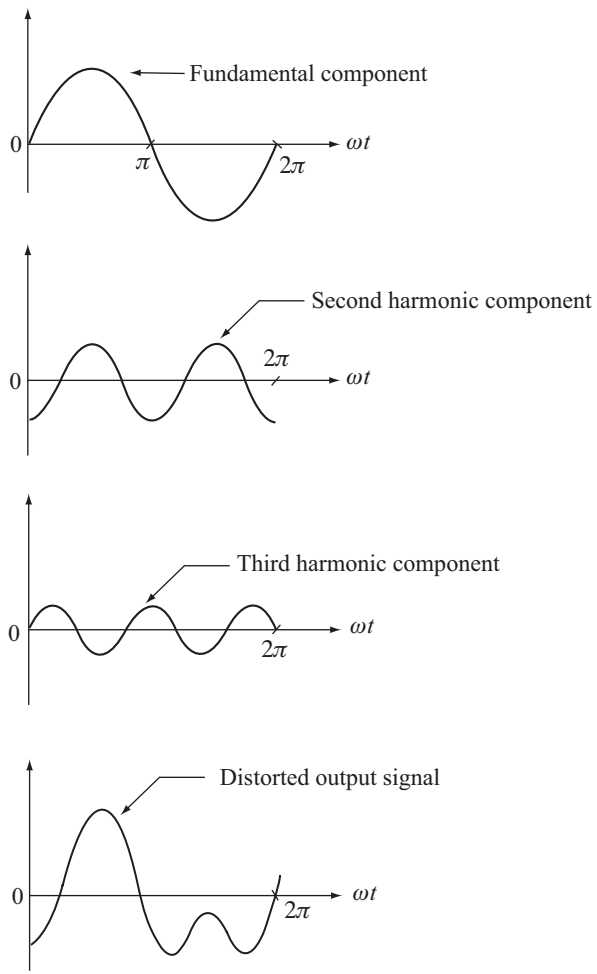


Fig. (b) Graphical representation of harmonic components and the distorted output signal

From the above equation we find that the second harmonic component has the largest amplitude of all other harmonic components and it is the principal source of harmonic distortion.

Fig. (b) shows the graphical description of Harmonic components of a distorted signal.

7.3.1 Second Harmonic Distortion

In the previous section we found that the second harmonic component has the largest amplitude of all other harmonic components which is the principal source of harmonic distortion. Now Let us proceed to estimate the magnitude of second harmonic distortion by considering the second order non linearity.

The relationship between the collector current and base current is given by

$$i_c = G_1 i_b + G_2 i_b^2 \tag{7.50}$$

where, i_c and i_b represent the instantaneous collector and base current respectively and G_1 and G_2 are constants.

Let the input base current be of the form

$$i_b = I_{bm} \cos \omega t \tag{7.51}$$

i_b is represented by I_{bm} cos ωt for sake of computational simplicity; it could as well be I_{bm} sin ωt where, I_{bm} is peak value of base current. Substituting Equation (7.51) in Equation (7.50)

$$i_c = G_1 (I_{bm} \cos \omega t) + G_2 (I_{bm} \cos \omega t)^2 \tag{7.52}$$

But
$$\cos^2 \omega t = \frac{1 + \cos 2\omega t}{2} \tag{7.53}$$

$\therefore$
$$i_c = G_1 (I_{bm} \cos \omega t) + G_2 I_{bm}^2 \frac{(1 + \cos 2\omega t)}{2}$$

$$= G_1 (I_{bm} \cos \omega t) + \frac{G_2 I_{bm}^2}{2} + \frac{G_2 I_{bm}^2}{2} \cos 2\omega t$$

$$i_c = \frac{G_2 I_{bm}^2}{2} + G_1 I_{bm} \cos \omega t + \frac{G_2 I_{bm}^2}{2} \cos 2\omega t \tag{7.54}$$

Let
$$B_0 = \frac{G_2 I_{bm}^2}{2} = B_2$$

and
$$B_1 = G_1 I_{bm}$$

where B_0 represents the dc term while B_1 represents the peak value of the fundamental output current and B_2 the peak value of the second harmonic component of the output current.

Now Equation (7.54) becomes

$$i_c = B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t \tag{7.55}$$

From Equation (7.55) observe that under second order non-linearity, we get

- B_0, a dc term indicating that a part of the input signal is being rectified.
- B_1cos ωt, an ac term which represents the amplified input signal and
- B_2 cos 2 ωt, another ac term which represents the second harmonic component.

Thus, because of the dc term and the second harmonic component, the output signal will not be an exact replica of the input signal.

Now, the total instantaneous collector current

i_C = Quiescent collector current + instantaneous collector current

$$i_C = I_{CQ} + i_c \tag{7.56}$$

Substituting for i_c from Equation (7.55), we have

$$i_C = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\,\omega t \tag{7.57}$$

We can estimate the amplitudes of B_0, B_1 and B_2 from the dynamic transfer characteristics shown in Fig. 7.13.

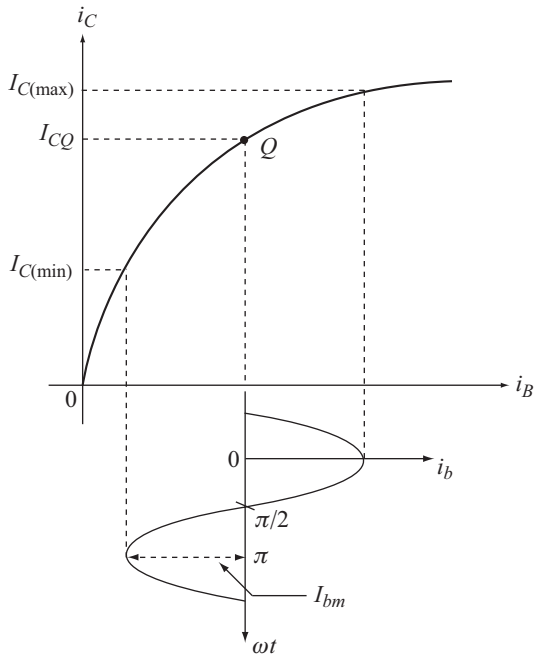


Fig. 7.13 Computation of harmonic components

There are 3 unknowns in Equation (7.57), i.e., B_0, B_1 and B_2 and hence we consider three points, i.e, $I_{C(max)}$, I_{CQ} and $I_{C(min)}$ on the dynamic transfer characteristics. This procedure is known as the **3-point method** of calculating harmonic distortion.

From Fig. 7.13, we have,

$$\left.\begin{aligned} &\text{at } \omega t = 0, && i_C = I_{C\,(max)} \\ \text{and} \quad &\text{at } \omega t = \frac{\pi}{2}, && i_C = I_{CQ} \\ &\text{at } \omega t = \pi, && i_C = I_{C\,(min)} \end{aligned}\right\} \tag{7.58}$$

Applying this condition to Equation (7.57), we get

$$I_{C(\max)} = I_{CQ} + B_0 + B_1 + B_2 \tag{7.59}$$

$$I_{CQ} = I_{CQ} + B_0 - B_2$$

$$\Rightarrow \quad B_0 = B_2 \tag{7.60}$$

as expected, and

$$I_{C(\min)} = I_{CQ} + B_0 - B_1 + B_2 \tag{7.61}$$

Applying Equation (7.60) to Equations (7.59) and (7.61),

$$I_{C(\max)} = I_{CQ} + 2\,B_0 + B_1 \tag{7.62}$$

and

$$I_{C(\min)} = I_{CQ} + 2\,B_0 - B_1 \tag{7.63}$$

Subtracting Equation (7.63) from Equation (7.62)

$$I_{C(\max)} - I_{C(\min)} = 2\,B_1$$

or

$$B_1 = \frac{I_{C(\max)} - I_{C(\min)}}{2} \tag{7.64}$$

Adding equations (7.62) and (7.63)

$$I_{C(\max)} + I_{C(\min)} = 2\,I_{CQ} + 4\,B_0$$

$$\therefore \quad B_0 = B_2 = \frac{I_{C(\max)} + I_{C(\min)} - 2\,I_{CQ}}{4} \tag{7.65}$$

% second harmonic distortion is given by

$$D_2 = \frac{\text{Magnitude of second harmonic component}}{\text{Magnitude of fundamental}} \times 100\,\%$$

$$D_2 = \frac{|B_2|}{|B_1|} \times 100\,\% \tag{7.66}$$

Substituting for B_1 and B_2 we get

$$D_2 = \left| \frac{\frac{1}{2}[I_{C(\max)} + I_{C(\min)}] - I_{CQ}}{I_{C\max} - I_{C\min}} \right| \times 100\,\% \tag{7.67}$$

In a similar manner, the second harmonic distortion can expressed interms of collector-emitter voltages as

$$D_2 = \left| \frac{\frac{1}{2}[V_{CE(\max)} + V_{CE(\min)}] - V_{CEQ}}{V_{CE(\max)} - V_{CE(\min)}} \right| \times 100\,\% \tag{7.68}$$

Example 7.6

The following readings are available for a power amplifier. Calculate the second harmonic distortion in each case.

(a) $V_{CEQ} = 10\text{ V}$ $V_{CE(\max)} = 18\text{ V}$ $V_{CE(\min)} = 1\text{ V}$

(b) $V_{CEQ} = 10\text{ V}$ $V_{CE(\max)} = 19\text{ V}$ $V_{CE(\min)} = 1\text{ V}$

Solution

(a)
$$D_2 = \left| \frac{\frac{1}{2}[V_{CE(\max)} + V_{CE(\min)}] - V_{CEQ}}{V_{CE(\max)} - V_{CE(\min)}} \right| \times 100\%$$

$$= \left| \frac{\frac{1}{2}[18\text{V} + 1\text{V}] - 10\text{V}}{18\text{V} - 1\text{V}} \right| \times 100\% = 2.94\%$$

(b)
$$D_2 = \left| \frac{\frac{1}{2}[19\text{V} + 1\text{V}] - 10\text{V}}{19\text{V} - 1\text{V}} \right| \times 100\% = 0\%$$

Example 7.7

A transistor supplies 0.85 W to a 4 kΩ load. The zero signal DC collector current is 31 mA and the dc collector current with signal is 34 mA. Determine the second harmonic distortion.

Solution

Given,

$$P_{o(\text{ac})} = 0.85\text{ W} \qquad R_L = 4\text{ k}\Omega$$

Under zero signal, the collector current is the quiscent collector current.

$$\therefore \quad I_{CQ} = 31\text{ mA}$$

When the signal is present, the dc collector current is $I_{CQ} + B_0$

$$\therefore \quad I_{CQ} + B_0 = 34\text{ mA}$$

$$\therefore \quad B_0 = 34\text{ mA} - 31\text{ mA} = 3\text{ mA}$$

$$\therefore \quad B_0 = B_2 = 3\text{ mA}$$

The given $P_{o(\text{ac})}$ is the power delivered by the fundamental component.

$$P_{o(\text{ac})} = \left(\frac{I_{L(\text{p})}}{\sqrt{2}} \right)^2 \times R_L$$

Since B_1 is the peak value of the fundamental, $I_{L(\text{p})} = B_1$

$$\therefore \quad P_{o(\text{ac})} = \left(\frac{B_1}{\sqrt{2}}\right)^2 \times R_L$$

$$\frac{B_1^2}{2} = \frac{P_{o(\text{ac})}}{R_L}$$

$$B_1 = \sqrt{\frac{2\,P_{o(\text{ac})}}{R_L}} = \sqrt{\frac{2 \times 0.8\ \text{W}}{4\,\text{k}\Omega}} = 20\ \text{mA}$$

$$\therefore \quad \%\ D_2 = \frac{|B_2|}{|B_1|} \times 100\%$$

$$= \frac{3\ \text{mA}}{20\ \text{mA}} \times 100\% = 15\%$$

Example 7.8

Non-linear distortion results in the generation of frequencies in the output that are not present in the input. If the dynamic curve can be represented by the equation $i_c = G_1\, i_b + G_2\, i_b^2$ and if the input signal is given by $i_b = (I_1 \cos \omega_1 t + I_2 \cos \omega_2 t)$, show that the output will contain a DC term and sinusoidal terms of frequencies ω_1, ω_2, $2\,\omega_1$, $2\,\omega_2$, $(\omega_1 + \omega_2)$ and $(\omega_1 - \omega_2)$.

Solution

Given

$$i_c = G_1\, i_b + G_2\, i_b^2 \qquad \text{(A)}$$

and

$$i_b = I_1 \cos \omega_1 t + I_2 \cos \omega_2 t \qquad \text{(B)}$$

Substituting Equation (B) into (A)

$$i_c = G_1\,(I_1 \cos \omega_1 t + I_2 \cos \omega_2 t) + G_2\,(I_1 \cos \omega_1 t + I_2 \cos \omega_2 t)^2$$

$$i_c = G_1 I_1 \cos \omega_1 t + G_1 I_2 \cos \omega_2 t + G_2\,(I_1^2 \cos^2 \omega_1 t + I_2^2 \cos^2 \omega_2 t + 2\, I_1 I_2 \cos \omega_1 t \cos \omega_2 t) \qquad \text{(C)}$$

$$\cos^2 \omega_1 t = \frac{1 + \cos 2\,\omega_1 t}{2}$$

$$\cos^2 \omega_2 t = \frac{1 + \cos 2\,\omega_2 t}{2}$$

$$\cos \omega_1 t\ \cos \omega_2 t = \frac{\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t}{2}$$

Using these relations in Equation (C)

$$i_c = G_1 I_1 \cos \omega_1 t + G_1 I_2 \cos \omega_2 t + G_2 I_1^2 \frac{(1 + \cos 2\omega_1 t)}{2} + G_2 I_2^2 \frac{(1 + \cos 2\omega_2 t)}{2} +$$

$$2\, G_2 I_1 I_2 \left(\frac{\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t}{2}\right)$$

$$= G_1 I_1 \cos \omega_1 t + G_1 I_2 \cos \omega_2 t + \frac{G_2 I_1^2}{2} + \frac{G_2 I_1^2}{2} \cos 2\omega_1 t + \frac{G_2 I_2^2}{2}$$

$$+ \frac{G_2 I_2^2}{2} \cos 2\omega_2 t + G_2 I_1 I_2 \cos(\omega_1 + \omega_2)\, t + G_2 I_1 I_2 \cos(\omega_1 - \omega_2)\, t$$

$$= \frac{G_2}{2}(I_1^2 + I_2^2) + G_1 I_1 \cos \omega_1 t + G_1 I_2 \cos \omega_2 t + \frac{G_2 I_1^2}{2} \cos 2\omega_1 t$$

$$+ \frac{G_2 I_2^2}{2} \cos 2\omega_2 t + G_2 I_1 I_2 \cos(\omega_1 + \omega_2)\, t + G_2 I_1 I_2 \cos(\omega_1 - \omega_2)\, t \quad \text{(D)}$$

Observe that Equation (D) has a dc component besides the cosine terms with frequencies ω_1, ω_2, $2\omega_1$, $2\omega_2$, $(\omega_1 + \omega_2)$ and $(\omega_1 - \omega_2)$

7.4 HIGHER-ORDER HARMONIC DISTORTION

In section 7.3.1, we have considered only second-order non-linearity. In a power amplifier since the magnitudes of voltages and currents will be large, it is necessary to consider higher-order non-linearities also.

We can express the output current by a power series of the form

$$i_c = G_1 i_b + G_2 i_b^2 + G_3 i_b^3 + G_4 i_b^4 + \cdots + \cdots \quad (7.69)$$

$$i_b = I_{bm} \cos \omega t$$

Now Equation (7.69) can be written as

$$I_c = G_1(I_{bm} \cos \omega t) + G_2(I_{bm} \cos \omega t)^2 + G_3 (I_{bm} \cos \omega t)^3 + G_4 (I_{bm} \cos \omega t)^4 + \cdots + \cdots \quad (7.70)$$

Using proper trigonometric identities, Equation (7.70) can be compactly represented as

$$i_c = B_0 + B_1 \cos \omega t + B_2 \cos 2\,\omega t + B_3 \cos 3\,\omega t + B_4 \cos 4\,\omega t + \cdots \quad (7.71)$$

Observe the presence of higher-order harmonic terms corresponding to 2ω, 3ω, 4ω etc., in Equation (7.71).

The total instantaneous collector current

$$i_C = I_{CQ} + i_c$$

$$\therefore \quad i_C = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\,\omega t + B_3 \cos 3\,\omega t + B_4 \cos 4\,\omega t \quad (7.72)$$

Truncating after the 4th harmonic term.

There are 5 unknowns B_0 to B_4 which can be computed graphically using the ***5-point procedure***.

Calculation of Total Harmonic Distortion

% second harmonic distortion,

$$D_2 = \frac{|B_2|}{|B_1|} \times 100\% \quad (7.73)$$

% third harmonic distortion

$$D_3 = \frac{|B_3|}{|B_1|} \times 100\% \tag{7.74}$$

and % fourth harmonic distortion is

$$D_4 = \frac{|B_4|}{|B_1|} \times 100\% \tag{7.75}$$

Total harmonic distortion (THD) or distortion factor is

$$\text{THD} = D = \sqrt{D_2^2 + D_3^2 + D_4^2} \tag{7.76}$$

In general

$$D = \sqrt{D_2^2 + D_3^2 + D_4^2 + D_5^2 + \cdots} \tag{7.77}$$

when all the harmonic components are considered.

Now, let us calculate the total power output.

$$P = P_1 + P_2 + P_3 + P_4 + \cdots \tag{7.78}$$

where, P_1 is the power delivered to the load by the fundamental component and

P_i is the power delivered to the load by the i^{th} harmonic component (for $i = 2, 3, \ldots$)

P_1 = (Fundamental rms current)^2 × load resistance

$$\therefore \quad P_1 = \left(\frac{B_1}{\sqrt{2}}\right)^2 R_L$$

$$P_1 = \left(\frac{B_1^2}{2}\right) R_L \tag{7.79}$$

Similarly for $i = 2, 3, 4 \ldots$

$$P_i = \left(\frac{B_i^2}{2}\right) R_L \tag{7.80}$$

Substituting Equations (7.79) and (7.80) in Equation (7.78), the total power output is given by

$$P = \frac{B_1^2 R_L}{2} + \frac{B_2^2 R_L}{2} + \frac{B_3^2 R_L}{2} + \cdots + \cdots$$

$$P = \frac{B_1^2 R_L}{2}\left[1 + \left(\frac{B_2}{B_1}\right)^2 + \left(\frac{B_3}{B_1}\right)^2 + \cdots\right] \tag{7.81}$$

$$P = P_1 (1 + D_2^2 + D_3^2 + \cdots) \tag{7.82}$$

From Equation (7.77)

$$D^2 = D_2^2 + D_3^2 + D_4^2 + \cdots$$

$\therefore$ Substituting in Equation (7.82)

$$P = P_1 (1 + D^2) \tag{7.83}$$

or $$P = P_1 (1 + \text{THD}^2) \tag{7.84}$$

Note:

- The analysis given above can also be performed in terms of the components of output voltage. For distinction, we can use the symbols $A_0, A_1, A_2, A_3, \cdots$ to represent the dc, fundamental, second harmonic, third harmonic etc components respectively of the output voltage.
- The symbols $I_0, I_1, I_2, I_3, I_4, \cdots$ can be equivalently used instead of $B_0, B_1, B_2, B_3, B_4, \cdots$ respectively to represent the components of output current.
- Similarly the symbols $V_0, V_1, V_2, V_3, V_4, \cdots$ can be used instead of $A_0, A_1, A_2, A_3, A_4, \cdots$ respectively to represent the components of output voltage.

Example 7.9

The input excitation of an amplifier is $i_b = I_{bm} \sin \omega t$. Prove that the output current can be represented by a Fourier series which contains only odd sine components and even cosine components.

Solution

From Equation (7.69) the output current is given by

$$i_c = G_1 i_b + G_2 i_b^2 + G_3 i_b^3 + \cdots \tag{A}$$

Given, $$i_b = I_{bm} \sin \omega t \tag{B}$$

Substituting Equation (B) in Equation (A)

$$\begin{aligned} i_c &= G_1 I_{bm} \sin \omega t + G_2 (I_{bm} \sin \omega t)^2 + G_3 (I_{bm} \sin \omega t)^3 + \cdots \\ &= G_1 I_{bm} \sin \omega t + G_2 I_{bm}^2 \sin^2 \omega t + G_3 I_{bm}^3 \sin^3 \omega t + \cdots \end{aligned} \tag{C}$$

But $$\sin^2 \omega t = \frac{1 - \cos 2\omega t}{2} \quad \text{and} \quad \sin^3 \omega t = \frac{1}{4} (3 \sin \omega t - \sin 3 \omega t) \tag{D}$$

Substituting Equation (D) in Equation (C)

$$i_c = G_1 I_{bm} \sin \omega t + G_2 I_{bm}^2 \frac{1 - \cos 2\omega t}{2} + \frac{G_3 I_{bm}^3}{4} (3 \sin \omega t - \sin 3 \omega t) + \cdots$$

$$= G_1 I_{bm} \sin \omega t + \frac{G_2 I_{bm}^2}{2} - \frac{G_2 I_{bm}^2}{2} \cos 2 \omega t + \frac{3}{4} G_3 I_{bm}^3 \sin \omega t - \frac{G_3 I_{bm}^3}{4} \sin 3 \omega t + \cdots$$

$$= \frac{G_2 I_{bm}^2}{2} + \left(G_1 I_{bm} + \frac{3}{4} G_3 I_{bm}^3 \right) \sin \omega t - \frac{G_3 I_{bm}^3}{4} \sin 3 \omega t - \frac{G_2 I_{bm}^2}{2} \cos 2 \omega t + \cdots \tag{E}$$

Equation (E) shows that the output current has only odd sine components and even cosine components.

Example 7.10

A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as follows:

$B_0 = 1.5$ mA $\quad B_3 = 4$ mA
$B_1 = 120$ mA $\quad B_4 = 2$ mA
$B_2 = 10$ mA $\quad B_5 = 1$ mA

(a) Determine the percentage total harmonic distortion.
(b) Assume that a 2nd identical transistor is used along with a suitable transformer to provide push-pull operation. Use the above harmonic amplitudes to determine the new total harmonic distortion.
(c) If $R_L = 25\ \Omega$, calculate the total power output in each case.

Solution

(a) From Equation (7.77), total harmonic distortion is given by

$$D = \sqrt{D_2^2 + D_3^2 + D_4^2 + D_5^2} \qquad \text{(A)}$$

$$D_2 = \frac{|B_2|}{|B_1|} = \frac{10}{120} = 0.0833 \text{ or } 8.33\%$$

$$D_3 = \frac{|B_3|}{|B_1|} = \frac{4}{120} = 0.0333 \text{ or } 3.33\%$$

$$D_4 = \frac{|B_4|}{|B_1|} = \frac{2}{120} = 0.0166 \text{ or } 1.66\%$$

$$D_5 = \frac{|B_5|}{|B_1|} = \frac{1}{120} = 0.0083 \text{ or } 0.83\%$$

Substituting in Equation (A),

$$D = \sqrt{0.0833^2 + 0.0333^2 + 0.0166^2 + 0.0083^2}$$
$$= 0.0916 \text{ or } 9.16\%$$

(b) With push-pull connection, *even* harmonic distortion becomes zero (see Section 7.7)

$$\therefore \quad D_2 = D_4 = 0$$

From Equation (A), the total harmonic distortion is

$$D = \sqrt{D_3^2 + D_5^2}$$
$$= \sqrt{0.0333^2 + 0.0083^2} = 0.0343 \text{ or } 3.43\%$$

Observe that in push-pull configuration, the total harmonic distortion is only 30% of the single ended configuration.

(c) The total power output from Equation (7.83) is

$$P = P_1 (1 + D^2) \tag{B}$$

where $P_1 = \dfrac{B_1^2 R_L}{2}$ from Equation (7.79)

$$\therefore \quad P_1 = \frac{(120 \times 10^{-3})^2 \times 25}{2} = 0.18 \text{ W}$$

For part (a), $D = 0.0916$

$$\therefore \quad P_1 = 0.18 (1 + 0.0916^2) = 0.1815 \text{ W}$$

For (b) $D = 0.0343$

$$\therefore \quad P_1 = 0.18 (1 + 0.0343^2) = 0.1802 \text{ W}$$

Example 7.11

Calculate the harmonic distortion components and the total harmonic distortion for an output signal having fundamental amplitude of 3 V, second harmonic amplitude of 0.3 V, third harmonic amplitude of 0.15 V and fourth harmonic amplitude of 0.06 V. Also find the power delivered by the fundamental component of output voltage if $R_L = 15\Omega$.

Solution

Given $A_1 = 3$ V $A_2 = 0.3$ V $A_3 = 0.15$ V $A_4 = 0.06$ V.

$$D_2 = \frac{|A_2|}{|A_1|} = \frac{0.3}{3} = 0.1 \text{ or } 10\%$$

$$D_3 = \frac{|A_3|}{|A_1|} = \frac{0.15}{3} = 0.05 \text{ or } 5\%$$

$$D_4 = \frac{|A_4|}{|A_1|} = \frac{0.06}{3} = 0.02 \text{ or } 2\%$$

$\therefore$ Total harmonic distortion is

$$D = \sqrt{D_2^2 + D_3^2 + D_4^2}$$

$$= \sqrt{0.1^2 + 0.05^2 + 0.02^2}$$

$$D = 0.1135 \text{ or } 11.35\%$$

Power delivered by the fundamental component of output voltage

$$P_1 = \frac{A_1^2}{2R_L} = \frac{(3\text{V})^2}{(2)(15\Omega)} = 0.3 \text{ W}$$

Example 7.12

The following readings are obtained for a power amplifier.

$$V_{CE\,(\min)} = 2.4 \text{ V} \quad V_{CE\,(\max)} = 20 \text{ V} \quad V_{CEQ} = 10 \text{ V}$$

Calculate the second harmonic distortion.

Solution

From Equation (7.65) using voltages in place of currents, the second harmonic voltage is given by

$$A_2 = \frac{V_{CE(\max)} + V_{CE(\min)} - 2\,V_{CEQ}}{4}$$

$$= \frac{20 + 2.4 - (2 \times 10)}{4} = 0.6 \text{ V}$$

From Equation (7.64), in terms of voltages, the fundamental output voltage is

$$A_1 = \frac{V_{CE(\max)} - V_{CE(\min)}}{2} = \frac{20 - 2.4}{2} = 8.8 \text{ V}$$

$\therefore$ Second harmonic distortion is

$$D_2 = \frac{|A_2|}{|A_1|} = \frac{0.6}{8.8} = 0.0682 \text{ or } 6.82\,\%$$

Example 7.13

The following readings are obtained for a power amplifier

$$V_{CEQ} = 10 \text{ V} \quad V_{\max} = 14 \text{ V} \quad V_{\min} = 6 \text{ V}$$

Calculate the second harmonic distortion.

Solution

Since, the output is taken between collector and emitter,

$$V_{\max} = V_{CE(\max)} = 14 \text{ V}$$
$$V_{\min} = V_{CE(\min)} = 6 \text{ V}$$

Fundamental component of output voltage is

$$\therefore \quad A_1 = \frac{V_{CE(\max)} - V_{CE(\min)}}{2} = \frac{14 - 6}{2} = 4 \text{ V}$$

$$A_2 = \frac{V_{CE(\max)} + V_{CE(\min)} - 2\,V_{CEQ}}{4} = \frac{14 + 6 - 20}{4} = 0$$

$\therefore$ Second harmonic distortion is zero.

In this example, since the output voltage swing is symmetric about V_{CEQ}, the amplifier is linear and hence second harmonic distortion is zero.

Example 7.14

For a given power amplifier the output current varies as follows: $I_{max} = 2.5$ A, $I_{min} = 1.8$ A with $I_{CQ} = 2$ A and $R_L = 8\ \Omega$. Find

(a) Second harmonic distortion,
(b) Power delivered by the fundamental component of output current to the load,
(c) Total power delivered to the load.

Solution

$$I_{max} = I_{C(max)} = 2.5 \text{ A}$$
$$I_{min} = I_{C(min)} = 1.8 \text{ A}$$
$$I_{CQ} = 2 \text{ A} \qquad R_L = 8\ \Omega$$

(a) 2nd harmonic component of current is

$$B_2 = \frac{I_{C(max)} + I_{C(min)} - 2I_{CQ}}{4} = \frac{2.5 + 1.8 - (2 \times 2)}{4} = 0.075 \text{ A}$$

$$B_1 = \frac{I_{C(max)} - I_{C(min)}}{2} = \frac{2.5 - 1.8}{2} = 0.35 \text{ A}$$

$\therefore$ Second harmonic distortion

$$D_2 = \frac{|B_2|}{|B_1|} = \frac{0.075}{0.35} = 0.214 \text{ or } 21.4\%$$

(b) Power delivered by the fundamental

$$P_1 = \frac{B_1^2 R_L}{2}$$

$$= \frac{0.35^2 \times 8}{2} = 0.49 \text{ W}$$

(c) Total power delivered to the load

$$P = P_1 + P_2$$

$$P_2 = \frac{B_2^2 R_L}{2} = \frac{0.075^2 \times 8}{2} = 0.0225 \text{ W}$$

Now $P = 0.49 + 0.0225 = 0.5125$ W.

Example 7.15

For a power amplifier the output current variations are $I_{C(max)} = 5$ A, $I_{C(min)} = 1$ A with $I_{CQ} = 3$ A and $R_L = 5\ \Omega$. Find,

(a) Second harmonic distortion,
(b) Power delivered by the fundamental component of output current and
(c) Total power delivered to the load.

Solution

Output current is the same as collector current

$$\therefore \qquad I_{C(\max)} = 5 \text{ A and } I_{C(\min)} = 1 \text{ A}$$

(a) Fundamental component of current is

$$B_1 = \frac{I_{C(\max)} - I_{C(\min)}}{2} = \frac{5-1}{2} = 2 \text{ A}$$

2nd harmonic component of current is

$$B_2 = \frac{I_{C(\max)} + I_{C(\min)} - 2\, I_{CQ}}{4} = \frac{5+1-(2\times 3)}{4} = 0 \text{ A}$$

$$\therefore \qquad D_2 = \frac{|B_2|}{|B_1|} = 0$$

This is expected since the output current is symmetrical and the amplifier is linear.

(b) Power delivered by the fundamental.

$$P_1 = \frac{B_1^2 R_L}{2} = \frac{2^2 \times 5}{2} = 10 \text{ W}$$

(c) Power delivered by the second harmonic is 0 W.

$\therefore$ Total power delivered to the load $P = P_1 + P_2 = 10$ W.

Example 7.16

The following distortion readings are available for a power amplifier.

$D_2 = 0.2$ $\quad D_3 = 0.02$ $\quad D_4 = 0.06$

with $I_1 = 3.3$ A and $R_C = 4\ \Omega$

(a) Calculate the THD.
(b) Determine the fundamental power component.
(c) Calculate the total power.

Solution

(a) Total harmonic distortion (THD) is

$$D = \sqrt{D_2^2 + D_3^2 + D_4^2}$$

$$= \sqrt{(0.2)^2 + (0.02)^2 + (0.06)^2} = 0.2097 \text{ or } 20.97\ \%$$

(b) Fundamental component of current is

$$I_1 = B_1 = 3.3 \text{ A}$$

$$R_C = R_L = 4\ \Omega$$

$$P_1 = \frac{B_1^2}{2} R_L = \frac{(3.3\,\text{A})^2}{2}(4\ \Omega) = 21.78\ \text{W}$$

(c) $$P = P_1(1 + D^2) = (21.78\ \text{W})\,[1 + (0.2097)^2] = 22.74\ \text{W}$$

◆ 7.5 CONVERSION EFFICIENCY

Power amplifiers convert the dc power of the supply V_{CC} into ac (signal) power at the load. The ratio of the ac power delivered to the load to the dc power supplied to the power amplifier is called the **conversion efficiency** or theoritical efficiency. Since, power conversion takes place in the collector circuit of the power transistor, it is also referred to as the collector circuit efficiency. This is a figure of merit for the power amplifier and denoted by η

$$\%\,\eta = \frac{\text{ac or signal power delivered to the load}}{\text{dc power supplied to the amplifier}} \times 100\,\%$$

$$\%\,\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\,\% \tag{7.85}$$

From Equation (7.10)

$$P_{o(\text{ac})} = \frac{V_{CE(p)}\, I_{C(p)}}{2}$$

The dc power input is given by

$$P_{i\,(dc)} = V_{CC}\, I_{CQ}$$

Substituting in Equation (7.85)

$$\%\,\eta = \frac{V_{CE(p)}\, I_{C(p)}}{2\ V_{CC}\, I_{CQ}} \times 100\,\% \tag{7.86}$$

or $$\%\,\eta = 50\ \frac{V_{CE(p)}\, I_{C(p)}}{V_{CC}\, I_{CQ}}\ \% \tag{7.87}$$

Let us now obtain the conversion efficiency of the series fed and the transformer coupled class A power amplifiers.

7.5.1 Conversion Efficiency of Class A Series-fed Power Amplifier

Refer Fig. 7.8 in Section 7.2.1.

$$V_{CE(p)} = \frac{V_{CE(\max)} - V_{CE(\min)}}{2}$$

Substituting in Equation (7.87)

$$\%\,\eta = \frac{50\left[V_{CE(\max)} - V_{CE(\min)}\right] I_{C(p)}}{2 V_{CC}\, I_{CQ}}\ \%$$

$$\text{or} \qquad \%\,\eta = \frac{25\left[V_{CE(\max)} - V_{CE(\min)}\right] I_{C(p)}}{V_{CC}\, I_{CQ}}\,\%$$

With reference to Fig. 7.8, $I_{C(p)}$ at best can be equal to I_{CQ} for distortionless output as shown in Fig. 7.14.

Substituting $I_{C(p)} = I_{CQ}$ in the above equation.

$$\%\,\eta = \frac{25\left[V_{CE(\max)} - V_{CE(\min)}\right]}{V_{CC}}\,\%$$

From the above equation and Fig. 7.14 it is easy to see that efficiency is maximum when

$$V_{CE(\min)} = 0 \text{ and } V_{CE(\max)} = V_{CC}$$

$$\therefore \qquad \%\,\eta_{\max} = 25\,\% \tag{7.88}$$

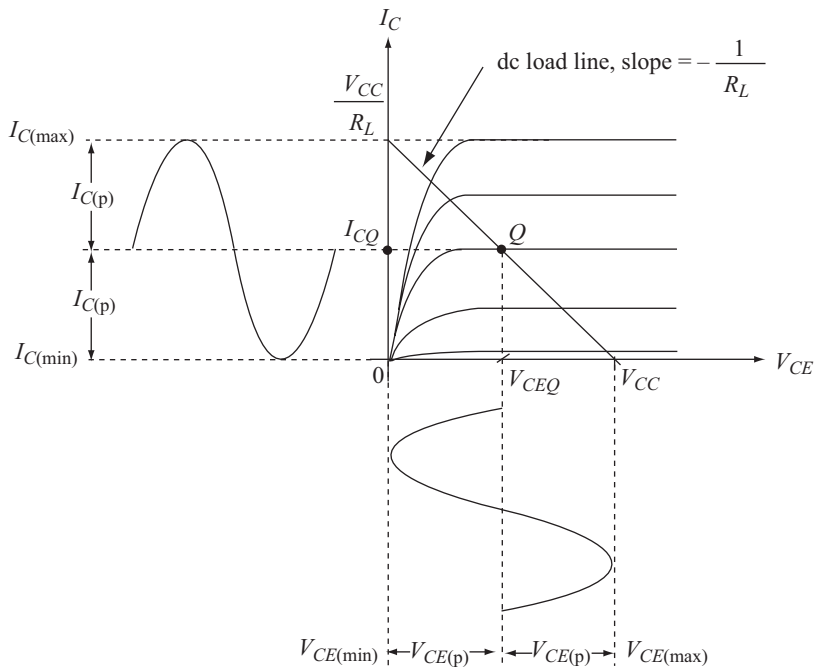


Fig. 7.14 Maximum values of current and voltage for distortionless output

This is the maximum obtainable efficiency for a series-fed class A power amplifier.

The low value of efficiency results from the continuous power dissipation in the collector circuit of the transistor.

7.5.2 Conversion Efficiency of Transformer-Coupled Class A Power Amplifier

Refer Fig. 7.12 in section 7.2.2. From Equations (7.35) and (7.36).

$$V_{CC} = \frac{V_{CE(\max)} + V_{CE(\min)}}{2} \quad \text{and} \quad V_{CE(p)} = \frac{V_{CE(\max)} - V_{CE(\min)}}{2} \tag{7.89}$$

With reference to Fig. 7.12, $I_{C(p)}$ at best can be equal to I_{CQ} for distortionless output.

Substituting $I_{CQ} = I_{C(p)}$ and Equation (7.89) in Equation (7.87)

$$\%\,\eta = \frac{50 V_{CE(p)}\, I_{C(p)}}{V_{CC}\, I_{CQ}}\,\%$$

$$= 50 \times \frac{\left[\dfrac{V_{CE(\max)} - V_{CE(\min)}}{2}\right]}{\left[\dfrac{V_{CE(\max)} + V_{CE(\min)}}{2}\right]}\,\%$$

$$\%\,\eta = 50 \times \frac{V_{CE(\max)} - V_{CE(\min)}}{V_{CE(\max)} + V_{CE(\min)}}\,\% \tag{7.90}$$

Maximum efficiency can be obtained if $V_{CE(\min)} = 0$

$$\therefore \qquad \%\,\eta_{\max} = 50\,\% \tag{7.91}$$

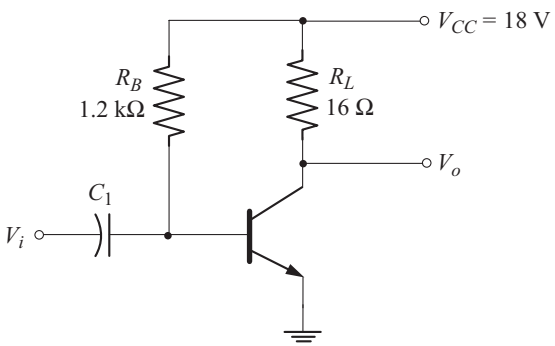
Thus the maximum attainable efficiency for a transformer-coupled class A power amplifier is 50%. It is double that of the series-fed class A power amplifier.

The higher value of efficiency results from the reduced power dissipation in the collector circuit which is due to the smaller value of dc primary resistance $R_{1\,(dc)}$.

Example 7.17

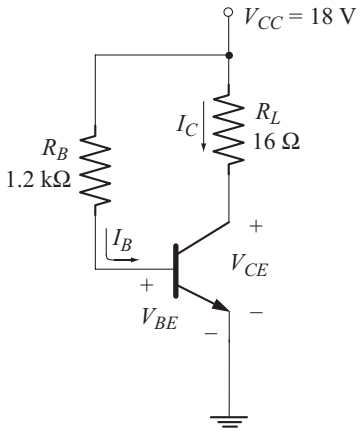
(a) Calculate the input power, output power and efficiency of the amplifier shown for an input voltage that results in a base current of 5 mA rms. Assume silicon transistor with $\beta = 40$ and $V_{BE} = 0.7$ V.

(b) Show under zero signal condition that the dc power input to the circuit is the sum of dc power dissipated in the load, and power dissipated in the collector.



Solution

(a) The dc equivalent circuit is shown below.



$$I_B = I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = 14.42\text{ mA}$$

$$I_C = I_{CQ} = \beta I_{BQ} = 40 \times 14.42\text{ mA} = 576.8\text{ mA}$$

Applying KVL to the collector circuit.

$$V_{CC} = I_C R_L + V_{CE}$$

$$\therefore \quad V_{CE} = V_{CEQ} = V_{CC} - I_{CQ} R_L$$

$$= 18\text{ V} - (576.8\text{ mA})\,(16\ \Omega) = 8.77\text{ V}$$

DC input power

$$P_{i(dc)} = V_{CC} \times I_{CQ}$$

$$= 18\text{ V} \times 576.8\text{ mA}$$

$$P_{i(dc)} = 10.4\text{ W} \qquad \text{(A)}$$

rms base current is given as

$$I_{B(\text{rms})} = 5\text{ mA}$$

$\therefore$ rms collector current is

$$I_{C(\text{rms})} = \beta\ I_{B(\text{rms})} = (40)\ (5\text{ mA}) = 200\text{ mA}$$

Peak collector current or peak load current is

$$I_{C(p)} = \sqrt{2} \times \text{rms collector current}$$

$$I_{C(p)} = \sqrt{2}\, I_{C(\text{rms})} = \sqrt{2} \times 200\text{ mA}$$

$$I_{C(p)} = 282.8\text{ mA}$$

ac power delivered to the load is

$$P_{o(\text{ac})} = \frac{I_{C(p)}^2 R_L}{2} = \frac{(282.8\,\text{mA})^2 (16\,\Omega)}{2} = 0.64\ \text{W} \qquad \text{(B)}$$

Conversion efficiency

$$\%\,\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\,\% = \frac{0.64\,\text{W}}{10.4\,\text{W}} \times 100\,\% = 6.15\,\%$$

(b) The dc power dissipated in the load

$$P_{L(dc)} = I_{CQ}^2 R_L = (576.8\ \text{mA})^2 \times 16\ \Omega = 5.3\ \text{W} \qquad \text{(C)}$$

Power dissipated in the collector

$$P_C = V_{CEQ} I_{CQ} = (8.77\ \text{V})\ (576.8\ \text{mA}) = 5.1\ \text{W} \qquad \text{(D)}$$

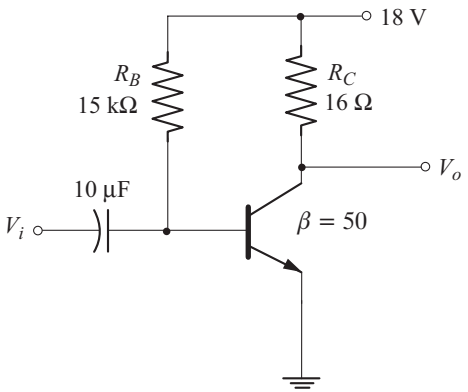
From equations (A), (C) and (D), observe that

$$P_{i(dc)} = P_{L(dc)} + P_C$$

Example 7.18

In the circuit shown below, the input signal results in a peak base current of 1 mA

(a) Calculate the ac output power
(b) Calculate the dc input power dissipated by the circuit
(c) Calculate the efficiency.



Solution

(a)

$$I_{B(p)} = 1\ \text{mA}$$

$$I_{C(p)} = \beta\, I_{B(p)} = (50)\ (1\ \text{mA}) = 50\ \text{mA}$$

$$P_{o(\text{ac})} = \frac{I_{C(p)}^2}{2} R_C = \frac{(50\,\text{mA})^2}{2} (16\ \Omega) = 20\ \text{mW}$$

(b)
$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\,\text{V} - 0.7\,\text{V}}{15\,\text{k}\Omega} = 1.153\ \text{mA}$$
$$I_{CQ} = \beta\ I_{BQ} = (50)\ (1.153\ \text{mA}) = 57.65\ \text{mA}$$
$$P_{i(dc)} = V_{CC}\, I_{CQ} = (18\ \text{V})\ (57.65\ \text{mA}) = 1.037\ \text{W}$$

(c)
$$\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} = \frac{20\,\text{mW}}{1.037\,\text{W}} = 0.0193 \text{ or } 1.93\%$$

Example 7.19

For the circuit of previous example,

(a) calculate the maximum output power
(b) if R_B is adjusted so that the Q point lies at the centre of the DC load line, calculate the input power for a maximum output power of 1.5 W. What is the efficiency in this case?

Solution

(a)
$$P_{o(\text{ac})} = \frac{V_{CE(p)}^2}{2R_C} = \frac{I_{C(p)}^2}{2} R_C$$
$$I_{CQ} = 57.65\ \text{mA} \quad \text{as before.}$$

To obtain maximum undistorted output, $I_{C(p)}$ should not exceed I_{CQ}

i.e. $$I_{C(p)} = I_{CQ} = 57.65\ \text{mA}$$

Maximum ac output power is

$$P_{o(\text{ac})} = \frac{I_{CQ}^2}{2} R_C = \frac{(57.65\,\text{mA})^2}{2}\ (16\ \Omega) = 26.59\ \text{mW}$$

(b) Since the Q point is at the centre

$$V_{CEQ} = \frac{V_{CC}}{2} = \frac{18\,\text{V}}{2} = 9\ \text{V}$$
$$I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_C} \quad [\text{From KVL equation of collector ciruit}]$$
$$= \frac{18\,\text{V} - 9\,\text{V}}{16\,\Omega} = 0.5625\ \text{A}$$
$$P_{i(dc)} = V_{CC}\, I_{CQ} = (18\ \text{V})\ (0.5625\ \text{A}) = 10.125\ \text{W}$$
$$\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} = \frac{1.5\,\text{W}}{10.125\,\text{W}} = 0.1482 \text{ or } 14.82\%$$

Note :

For the biasing condition given in part (b), the ac power delivered to the load is maximum when

$$V_{CE(p)} = V_{CEQ} \text{ and } I_{C(p)} = I_{CQ}$$

Under this condition the maximum ac output power is

$$p_{o\,(\text{ac})} = \frac{V_{CE(p)}\, I_{C(p)}}{2} = \frac{(9\,\text{V})(0.5625\,\text{A})}{2} = 2.53\ \text{W}$$

The corresponding efficiency is,

$$\eta = \frac{2.53\,\text{W}}{10.125\,\text{W}} \approx 0.25 \text{ or } 25\%$$

which is equal to the ideal value.

Therefore to obtain maximum efficiency when the Q point is at the centre of the dc load line, the input signal strength should be large enough to result in

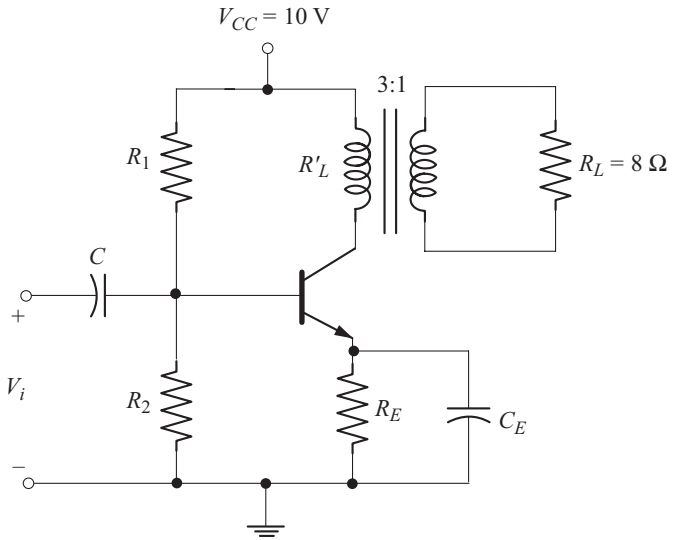
$$V_{CE(p)} = V_{CEQ} \quad \text{and} \quad I_{C(p)} = I_{CQ}$$

Otherwise the efficiency will be smaller than 25% even if the Q point is at the centre of the dc load line.

Example 7.20

For the circuit shown, the dc base current is 5 mA and the ac input signal results in a peak base current swing of 4 mA. Assume silicon transistor with $\beta = 30$. Find

(a) ac power delivered to the load
(b) dc power drawn by the circuit
(c) conversion efficiency



Solution

Given,

$$I_{BQ} = 5 \text{ mA} \quad I_{B(p)} = 4 \text{ mA} \qquad \beta = 30 \qquad \frac{N_1}{N_2} = 3$$

For transformer-coupled class A power amplifier

$$V_{CEQ} = V_{CC} = 10 \text{ V} \qquad \text{(see Fig. 7.12)}$$
$$I_{CQ} = \beta I_{BQ} = 30 \times 5 \text{ mA} = 150 \text{ mA}$$

Peak collector current

$$I_{C(p)} = \beta I_{B(p)} = 30 \times 4 \text{ mA} = 120 \text{ mA}$$

(a) From Equation (7.40), ac power delivered to the load is

$$P_{o(\text{ac})} = \frac{V_{CE(p)}^2}{2R_L'} = \frac{I^2{}_{C(p)}}{2} R_L'$$

But $$R_L' = R_L \left(\frac{N_1}{N_2}\right)^2 = (8\ \Omega)\ (3)^2 = 72\ \Omega$$

$\therefore$ $$P_{o(\text{ac})} = \frac{(120\,\text{mA})^2\,(72\,\Omega)}{2} = 0.52 \text{ W}$$

(b) dc power drawn by the circuit is

$$P_{i(dc)} = V_{CC}\, I_{CQ} = (10 \text{ V})\ (150 \text{ mA}) = 1.5 \text{ W}$$

(c) Conversion efficiency

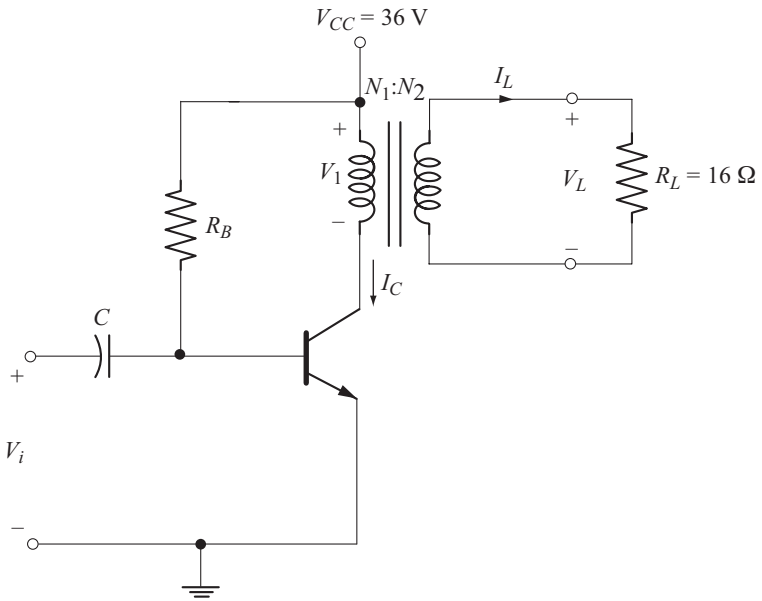
$$\%\,\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\,\%$$
$$= \frac{0.52\,\text{W}}{1.5\,\text{W}} \times 100\% = 34.7\%$$

Example 7.21

A transformer-coupled class A amplifier drives a 16 Ω loud speaker through a 4:1 transformer. With V_{CC} = 36 V the circuit delivers 2 W to the load. Find,

(a) power across the transformer primary,
(b) rms voltage across the load,
(c) rms voltage across the transformer primary,
(d) rms values of load current and primary current, and
(e) conversion efficiency if the dc collector current is 150 mA.

Solution



$$\frac{V_1}{V_L} = \frac{N_1}{N_2} = \frac{I_L}{I_C} \tag{A}$$

Given,

$$\frac{N_1}{N_2} = 4 \quad R_L = 16\ \Omega \quad V_{CC} = 36\ \text{V} \quad I_{CQ} = 150\ \text{mA}$$

Power delivered to the load R_L is, $P_L = 2$ W

(a) Power across transformer primary.

Assuming 100 % transformer efficiency, the power across transformer primary is

$$p_{pri} = p_{o(\text{ac})} = P_L = 2\ \text{W} \tag{B}$$

(b) rms voltage across the load

$$P_L = \frac{V_{L(\text{rms})}^2}{R_L}$$

$$\therefore \quad V_{L(\text{rms})} = \sqrt{P_L R_L} = \sqrt{(2\ \text{W})(16\Omega)} = 5.65\ \text{V}$$

(c) rms voltage across the transformer primary.

From Equation (A)

$$\frac{V_{1(\text{rms})}}{V_{L(\text{rms})}} = \frac{N_1}{N_2} = 4$$

$$\therefore \quad V_{1(\text{rms})} = 4\, V_{L(\text{rms})} = (4)\ (5.65\ \text{V}) = 22.6\ \text{V}$$

(d) rms load and primary current

$$P_L = I^2_{L\,(\text{rms})} \cdot R_L$$

$$\therefore \quad I_{L(\text{rms})} = \sqrt{\frac{P_L}{R_L}} = \sqrt{\frac{2\,\text{W}}{16\,\Omega}} = 353.55\ \text{mA}$$

From Equation (A) $$\frac{I_{L(\text{rms})}}{I_{C(\text{rms})}} = \frac{N_1}{N_2} = 4$$

$$\therefore \quad I_{C(\text{rms})} = \frac{I_{L(\text{rms})}}{4} = \frac{353.55\,\text{mA}}{4} = 88.39\ \text{mA}$$

(e) Conversion efficiency

$$\%\,\eta = \frac{p_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\% \qquad \text{(C)}$$

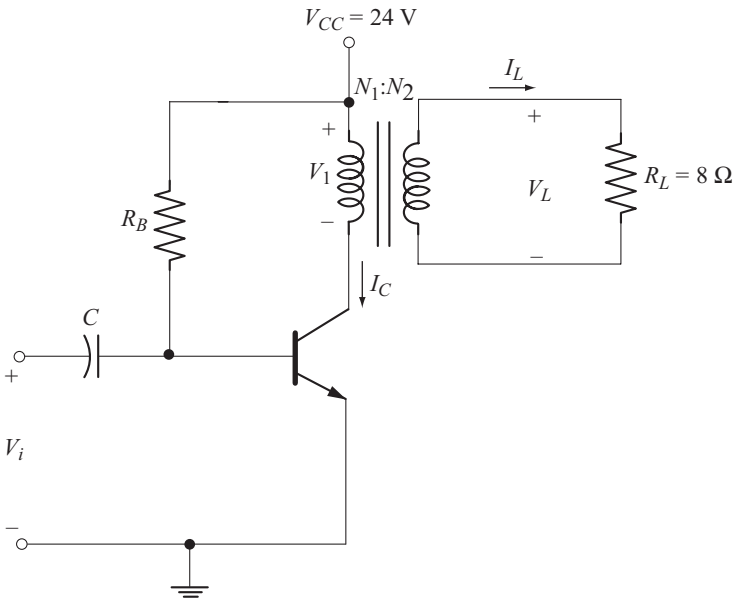
$$P_{i(dc)} = V_{CC}\, I_{CQ} = 36\ \text{V} \times 150\ \text{mA} = 5.4\ \text{W}$$

$\therefore$ From (B) and (C) $$\%\,\eta = \frac{2\,\text{W}}{5.4\,\text{W}} \times 100 = 37.03\%$$

Example 7.22

A transformer-coupled class A amplifier drives a load of 8 Ω through a 3:1 transformer. With V_{CC} = 24 V, the circuit delivers 2 W to the load. The transformer efficiency is 80%. Find,

(a) power across the transformer primary,
(b) rms voltage across load and transformer primary
(c) rms values of load current and primary current
(d) conversion efficiency if dc collector current is 260 mA.



Solution

$$\frac{V_1}{V_L} = \frac{N_1}{N_2} = \frac{I_L}{I_C} \quad \text{(A)}$$

Given, $\frac{N_1}{N_2} = 3$ $\eta_{TFR} = 0.8$ or 80% $R_L = 8\ \Omega$

$V_{CC} = 24$ V $I_{CQ} = 260$ mA $P_L = 2$ W

(a) $$\eta_{\text{TFR}} = \frac{P_L}{P_{o(\text{ac})}}$$

$$P_{pri} = P_{o(\text{ac})} = \frac{P_L}{0.8} = \frac{2\,\text{W}}{0.8} = 2.5\ \text{W}$$

(b) $$V_{L\,(\text{rms})} = \sqrt{P_L R_L} = \sqrt{(2\,\text{W})(8\Omega)} = 4\ \text{V}$$

(c) $$\frac{V_{1(\text{rms})}}{V_{L(\text{rms})}} = \frac{N_1}{N_2} = 3$$

$$\therefore V_{I(\text{rms})} = 3\,V_{L(\text{rms})} = 3 \times 4\ \text{V} = 12\ \text{V}$$

(d) rms load current

$$I_{L(\text{rms})} = \sqrt{\frac{P_L}{R_L}} = \sqrt{\frac{2\,\text{W}}{8\Omega}} = 0.5\ \text{A}$$

$$\frac{I_{L(\text{rms})}}{I_{C(\text{rms})}} = \frac{N_1}{N_2} = 3$$

rms primary current

$$I_{C(\text{rms})} = \frac{I_{L(\text{rms})}}{3} = \frac{0.5\,\text{A}}{3} = 0.1667\ \text{A}$$

(e) Conversion efficiency

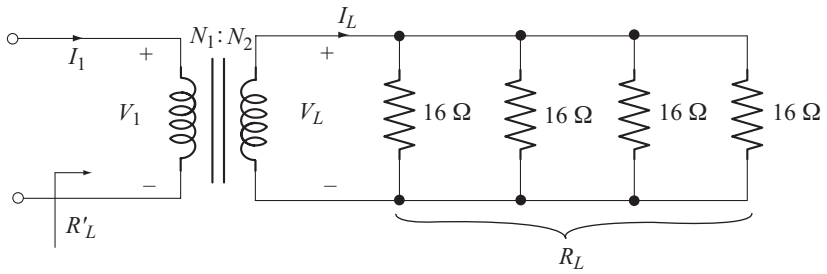
$$\%\,\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\%$$

$$P_{i(dc)} = V_{CC} \times I_{CQ} = 24\ \text{V} \times 260\ \text{mA} = 6.24\ \text{W}$$

$$\therefore \quad \%\,\eta = \frac{2.5\,\text{W}}{6.24\,\text{W}} \times 100\,\% = 40\,\%$$

Example 7.23

Find the turns ratio of the transformer required to connect four parallel 16 Ω loud speakers so that they appear as an 8 kΩ effective load.



Solution

$$R_L = (16\ \Omega \parallel 16\ \Omega \parallel 16\ \Omega \parallel 16\ \Omega) = \frac{16\Omega}{4} = 4\ \Omega$$

Given, $R'_L = 8\ \text{k}\Omega$

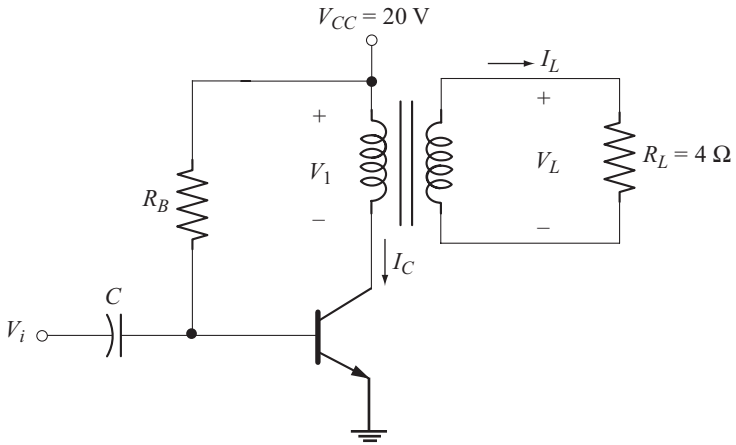
$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L$$

$$\therefore \quad \frac{N_1}{N_2} = \sqrt{\frac{R'_L}{R_L}} = \sqrt{\frac{8000\Omega}{4\Omega}} = \sqrt{2000} = 44.7$$

Example 7.24

A transformer-coupled class A power amplifier is required to deliver a maximum of 5 W to a 4 Ω load. The quiescent point is adjusted for symmetrical clipping and the collector supply voltage is $V_{CC} = 20$ V. Assuming ideal characteristics and taking $V_{CE(\text{min})} = 0$, find

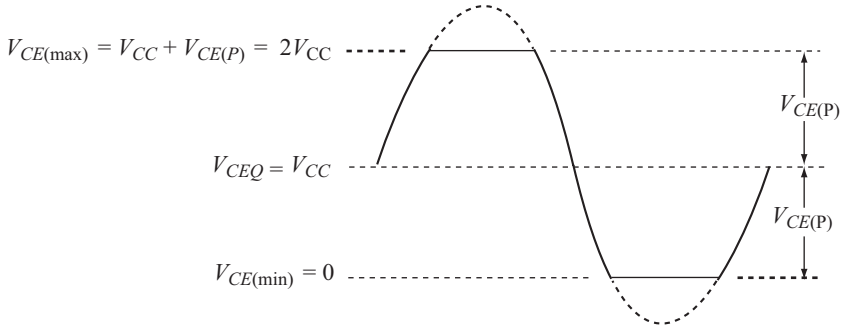
(a) the transformer turns ratio,
(b) peak collector current,
(c) quiescent operating point I_{CQ}, V_{CEQ}, and
(d) collector circuit efficiency.



Solution

Given, $V_{CC} = 20\text{ V} \quad R_L = 4\ \Omega \quad P_L = 5\text{ W} \quad V_{CE(\min)} = 0$

The output voltage waveform is shown below.



From the figure

$$V_{CE(p)} = V_{CC} = 20\text{ V}$$

(a) Assuming ideal transformer

$$P_{o(\text{ac})} = P_L = 5\text{ W}$$

But from Equation (7.40)

$$P_{o(\text{ac})} = \frac{V_{CE(p)}^2}{2R_L'}$$

$$\therefore \quad R_L' = \frac{V_{CE(p)}^2}{2P_{o(\text{ac})}} = \frac{(20\text{ V})^2}{2\times 5\text{ W}} = 40\ \Omega$$

$$R_L' = \left(\frac{N_1}{N_2}\right)^2 \times R_L$$

$$\Rightarrow \quad \left(\frac{N_1}{N_2}\right) = \sqrt{\frac{R_L'}{R_L}} = \sqrt{\frac{40\Omega}{4\Omega}} = \sqrt{10}$$

$$\therefore \quad N_1 : N_2 = \sqrt{10} : 1$$

(b) Peak collector current

$$P_{o(\text{ac})} = I_{C(\text{rms})}^2 R_L'$$

$$I_{C(\text{rms})}^2 = \sqrt{\frac{P_{o(\text{ac})}}{R_L'}} = \sqrt{\frac{5\text{ W}}{40\Omega}} = 0.353\text{ A}$$

Peak collector current

$$I_{C(p)} = \sqrt{2}\, I_{C(\text{rms})} = \sqrt{2} \times 0.353\text{ A} = 0.5\text{ A}$$

(c) Quiescent operating point

$$V_{CEQ} = V_{CC} = 20 \text{ V}$$
$$I_{CQ} = I_{C(p)} = 0.5$$

$\therefore$ Q-point is at (20 V, 0.5 A)

(d) Collector circuit efficiency

$$\%\,\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\,\%$$
$$P_{i(dc)} = V_{CC}\, I_{CQ} = 20 \text{ V} \times 0.5 \text{ A} = 10 \text{ W}$$
$$\therefore \quad \%\,\eta = \frac{5\,\text{W}}{10\,\text{W}} \times 100\,\% = 50\,\%$$

Observe that since we have assumed ideal conditions the conversion efficiency is 50% as expected.

Example 7.25

The following data is available for a class A transformer-coupled power amplifier.

$V_{CE(\text{max})}$	= 18.5 volts	$I_{C(\text{max})}$	= 250 mA
$V_{CE(\text{min})}$	= 1.5 volts	$I_{C(\text{min})}$	= 25 mA
V_{CC}	= 10 volts	I_{CQ}	= 140 mA
R_L	= 8 Ω		

Find:

(a) AC power delivered to the load
(b) Conversion efficiency
(c) Transformer turns ratio

Solution

(a) For a class A transformer-coupled power amplifier,

$$V_{CE(\text{max})} = V_{CC} + V_{CE(p)} \quad \text{(A)}$$
$$V_{CE(\text{min})} = V_{CC} - V_{CE(p)} \quad \text{(B)}$$

Solving for $V_{CE(p)}$ we get

$$V_{CE(p)} = \frac{V_{CE(\text{max})} - V_{CE(\text{min})}}{2} = \frac{18.5\,\text{V} - 1.5\,\text{V}}{2} = 8.5 \text{ V}$$

Similarly

$$I_{C(p)} = \frac{I_{C(\text{max})} - I_{C(\text{min})}}{2} = \frac{250\,\text{mA} - 25\,\text{mA}}{2} = 112.5 \text{ mA}$$

AC power delivered to the load

$$P_{o(\text{ac})} = \frac{V_{CE(p)}\, I_{C(p)}}{2}$$

$$= \frac{(8.5\,\text{V})(112.5\,\text{mA})}{2} = 0.478\ \text{W}$$

(b) $$\%\,\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\ \%$$

$$P_{i(dc)} = V_{CC} \times I_{CQ}$$

$$= (10\ \text{V})\ (140\ \text{mA}) = 1.4\ \text{W}$$

$$\therefore \quad \%\,\eta = \frac{0.478\,\text{W}}{1.4\,\text{W}} \times 100\ \% = 34.14\%$$

(c) $$V_{CE(p)} = I_{C(p)}\, R'_L$$

$$R'_L = \frac{V_{CE(p)}}{I_{C(p)}} = \frac{8.5\,\text{V}}{112.5\,\text{mA}} = 75.56\ \Omega$$

$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L$$

$$\frac{N_1}{N_2} = \sqrt{\frac{R'_L}{R_L}} = \sqrt{\frac{75.56\Omega}{8\Omega}} = 3.07$$

Example 7.26

Calculate the efficiency of transformer-coupled class A power amplifier for a collector dc supply of 15 V and outputs of

(a) $V_{CE(p)} = 3.75$ V

(b) $V_{CE(p)} = 7.5$ V

(c) $V_{CE(p)} = 15$ V

Comment on the result.

Solution

Given $$V_{CC} = 15\ \text{V}$$

The conversion efficiency of transformer-coupled class A power amplifier is given by

$$\%\,\eta = 50\left[\frac{V_{CE(\max)} - V_{CE(\min)}}{V_{CE(\max)} + V_{CE(\min)}}\right]\ \% \qquad \text{(A)}$$

where $$V_{CE(\max)} = V_{CC} + V_{CE(p)} \qquad \text{(B)}$$

$$V_{CE(\min)} = V_{CC} - V_{CE(p)} \quad \text{(C)}$$

(a) $V_{CE(p)} = 3.75$ volts

$$\begin{aligned} V_{CE(\max)} &= V_{CC} + V_{CE(p)} \\ &= 15\text{ V} + 3.75\text{ V} \\ &= 18.75\text{ V} \\ V_{CE(\min)} &= V_{CC} - V_{CE(p)} \\ &= 15\text{ V} - 3.75\text{ V} \\ &= 11.25\text{ V} \\ \%\,\eta &= 50 \times \frac{18.75\text{ V} - 11.25\text{ V}}{18.75\text{ V} + 11.25\text{ V}} \\ &= 12.5\% \end{aligned}$$

(b) $V_{CE(p)} = 7.5$ V

$$\begin{aligned} V_{CE(\max)} &= 15\text{ V} + 7.5\text{ V} \\ &= 22.5\text{ V} \\ V_{CE(\min)} &= 15\text{ V} - 7.5\text{ V} \\ &= 7.5\text{ V} \\ \%\,\eta &= 50 \times \frac{22.5\text{ V} - 7.5\text{ V}}{22.5\text{ V} + 7.5\text{ V}} = 25\% \end{aligned}$$

(c) $V_{CE(p)} = 15$ V

$$\begin{aligned} V_{CE(\max)} &= 15\text{ V} + 15\text{ V} = 30\text{ V} \\ V_{CE(\min)} &= 15\text{ V} - 15\text{ V} = 0\text{ V} \\ \%\,\eta &= 50 \times \frac{30\text{ V} - 0}{30\text{ V} + 0} = 50\% \end{aligned}$$

From the above calculations we find that, efficiency increases with increase in $V_{CE(p)}$ and a maximum efficiency of 50% is obtained when, $V_{CE(p)} = V_{CC} = 15$ V.

◆ 7.6 CLASS B PUSH-PULL POWER AMPLIFIER

As mentioned in Section 7.1.2 in class B power amplifier, the *Q*-point is located at cutoff. This means that the base-emitter voltage is at zero volts.

As a result the transistor conducts current for only one-half cycle of the signal cycle. To obtain output for the full cycle of the signal it is necessary to use two transistors, one conducting during the positive half cycle and the other during the negative half cycle as shown in Fig. 7.15. The configuration of Fig. 7.15(a) requires two dc power supplies where as a single dc power supply is sufficient for the configuration of Fig. 7.15(b).

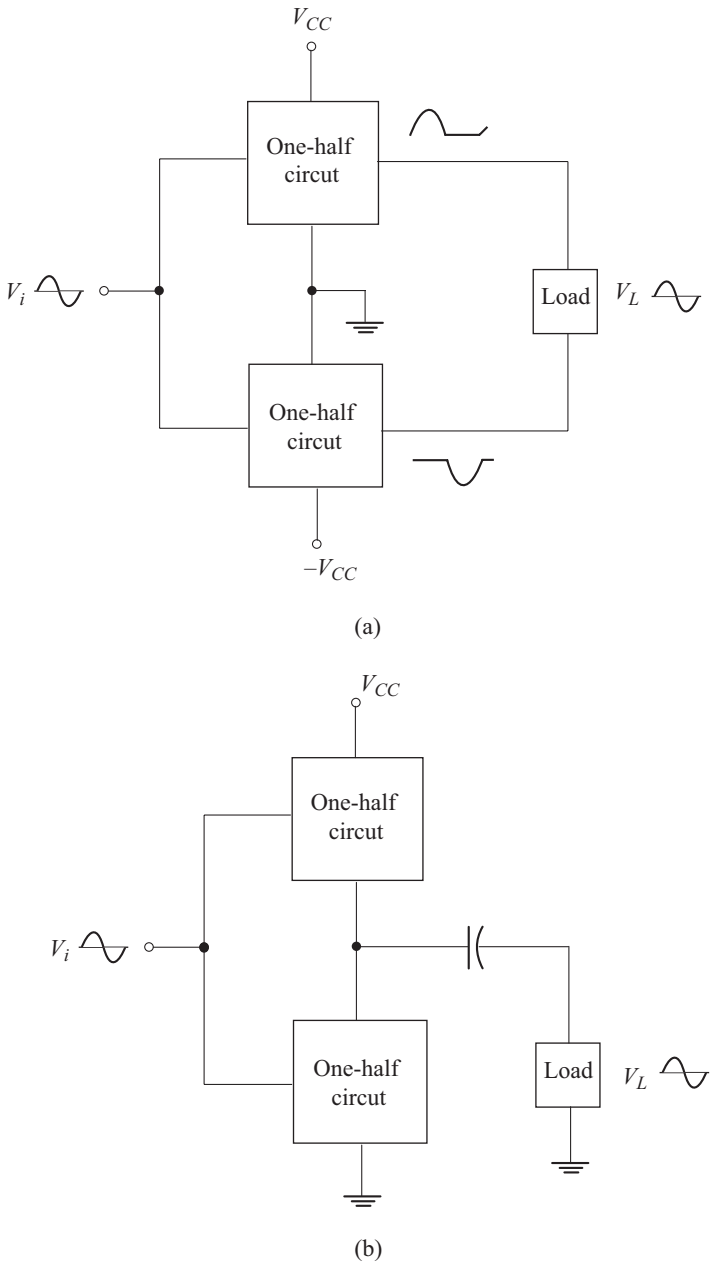


Fig. 7.15 Push pull amplifier
(a) Using two dc power supplies (b) Using single dc power supply

7.6.1 Operation of Class B Push-pull Power Amplifier

Figure 7.16 shows the circuit of class B push-pull power amplifier. Push-pull configuration is used to eliminate harmonic distortion introduced by the non-linearity of the dynamic transfer characteristic of the amplifying device.

The input transformer is a 1 : 1 : 1 transformer which is used to provide two equal voltages which are 180° out of phase with each other. The voltage divider network consisting of R_1 and R_2 is used to keep Q_1 and Q_2 in the verge of conduction. Note that the Q point is slightly above cut-off and as a result there will be no cross-over distortion. The output transformer is used to provide impedance matching between the amplifier output and the load.

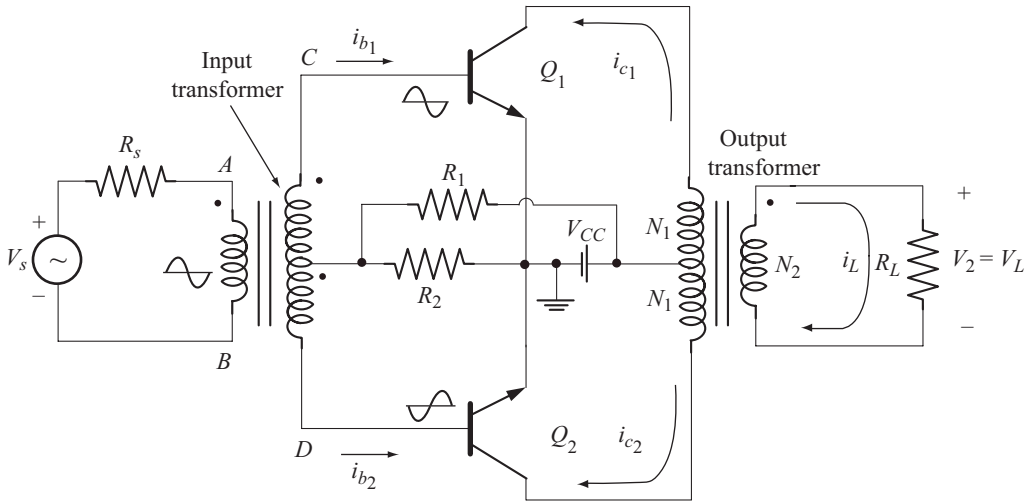


Fig. 7.16 Class B push-pull power amplifier

During the positive half cycle of the input signal v_s, the voltage at C is positive going while the voltage at D is negative going. Since the transistors are biased at cutoff, the base-emitter junction of Q_1 gets forward biased whereas the base-emitter junction of Q_2 goes further below cut-off. Thus i_{c_1} increases above zero (note that $I_{CQ} = 0$) while i_{c_2} is zero.

$$i_L = \frac{N_1}{N_2} i_{c_1} \tag{7.92}$$

It is easy to see that during the negative half cycle of the input signal v_s, Q_1 is *off* and Q_2 conducts.

$$i_L = -\frac{N_1}{N_2} i_{c_2} \tag{7.93}$$

The negative sign for i_L is due to the fact that i_{c_1} and i_{c_2} are in opposite directions.

Combining equations (7.92) and (7.93) we can write

$$i_L = \begin{cases} \dfrac{N_1}{N_2} i_{c_1} & \text{for } 0 \le \omega t \le \pi \\ -\dfrac{N_1}{N_2} i_{c_2} & \text{for } \pi \le \omega t \le 2\pi \end{cases}$$

$$\text{or} \qquad i_L = \frac{N_1}{N_2}\,[i_{c_1} - i_{c_2}] \tag{7.94}$$

The input and output voltage and current waveforms are in Fig. 7.17.

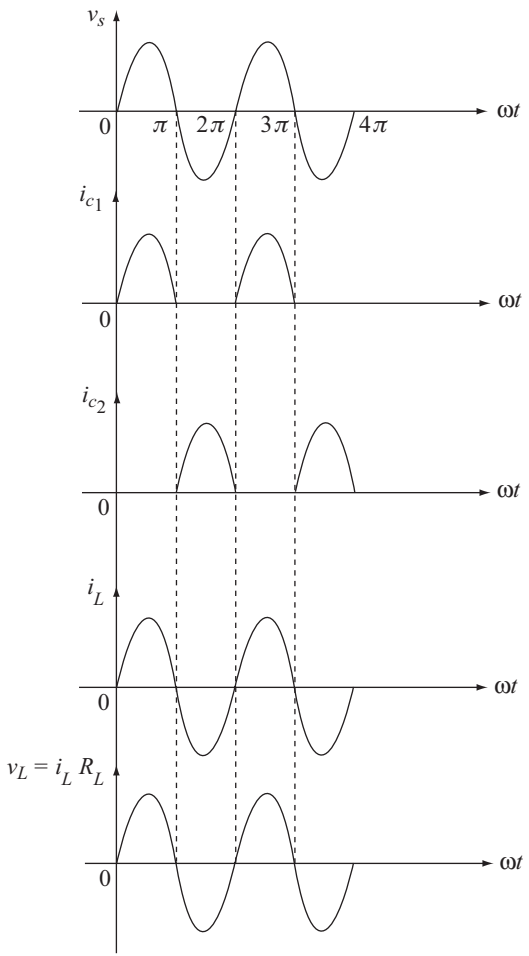


Fig. 7.17 Input and Output waveforms of class B push-pull amplifier

Elimination of Even Harmonic Distortion with Push-pull Operation

From Equation (7.72) total instantaneous collector current of transistor Q_1 is

$$i_{C_1} = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\,\omega t + B_3 \cos 3\,\omega t + B_4 \cos 4\,\omega t + \cdots \tag{7.95}$$

Observe in the circuit of Fig. 7.16 that i_{c_1} and i_{c_2} are flowing in opposite directions. Therefore, they differ in phase by 180°.

$$\text{Hence} \qquad i_{c_2}(\omega t) = i_{c_1}(\omega t + \pi) \tag{7.96}$$

Therefore, the total instantaneous collector current of transistor Q_2 can be obtained by replacing ωt by $(\omega t + \pi)$ in Equation (7.95)

$$i_{C_2} = I_{CQ} + B_0 + B_1 \cos(\omega t + \pi) + B_2 \cos 2(\omega t + \pi) + B_3 \cos 3(\omega t + \pi) + B_4 \cos 4(\omega t + \pi) + \cdots \quad (7.97)$$

$$\therefore \quad i_{C_2} = I_{CQ} + B_0 + B_1 \cos(\omega t + \pi) + B_2 \cos(2\omega t + 2\pi) + B_3 \cos(3\omega t + 3\pi) + B_4 \cos(4\omega t + 4\pi) + \cdots \quad (7.98)$$

We know that

$$\cos(\theta + n\pi) = \begin{cases} \cos\theta & \text{for even } n \\ -\cos\theta & \text{for odd } n \end{cases} \quad (7.99)$$

Applying Equation (7.99) to Equation (7.98), we have

$$i_{C_2} = I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + B_4 \cos 4\omega t + \cdots \quad (7.100)$$

From Equation (7.94)

$$i_L = \frac{N_1}{N_2} \{ (I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + B_4 \cos 4\omega t + \cdots) - (I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + B_4 \cos 4\omega t + \cdots)\} \quad (7.101)$$

$$\therefore \quad i_L = \frac{N_1}{N_2}(2B_1 \cos \omega t + 2B_3 \cos 3\omega t + \cdots) \quad (7.102)$$

or

$$i_L = \frac{2N_1}{N_2}(B_1 \cos \omega t + B_3 \cos 3\omega t + \cdots) \quad (7.103)$$

Observe from, Equation (7.103) that the output current is free from even harmonic components. The principal source of distortion is the third harmonic component which is very small in comparison with the fundamental. These results are possible only if the transistors Q_1 and Q_2 are identical. If their characteristics differ, then complete cancellation of even harmonic components will not take place.

Advantages of push-pull configuration :

Following are the advantages of push-pull configuration.

- The output current is free from even harmonic components and therefore the circuit gives more output per transistor for a specified amount of distortion.
- There is no dc current in the primary winding of the output transformer. This eliminates core saturation. Core saturation introduces non linear distortion, which arises from the curvature of the transformer magnetisation curve. Note that core saturation may occur in class A single ended transformer coupled amplifier as indicated in Section 7.2.2.
- V_{CC} is generally obtained form an ac source using rectifier and filter. Inadequate filtering gives rise to ripple voltages in V_{CC}. In the push-pull configuration the ripple currents produced by these ripple voltages are in opposite directions in the primary of the output transformer and therefore cancel out.

7.6.2 Phase Splitting Circuits

In the push pull amplifier circuit of Fig. 7.16, the input transformer was used to provide two signals of equal magnitude and opposite polarity. An alternate circuit which can be used for this purpose is shown in Fig. 7.18.

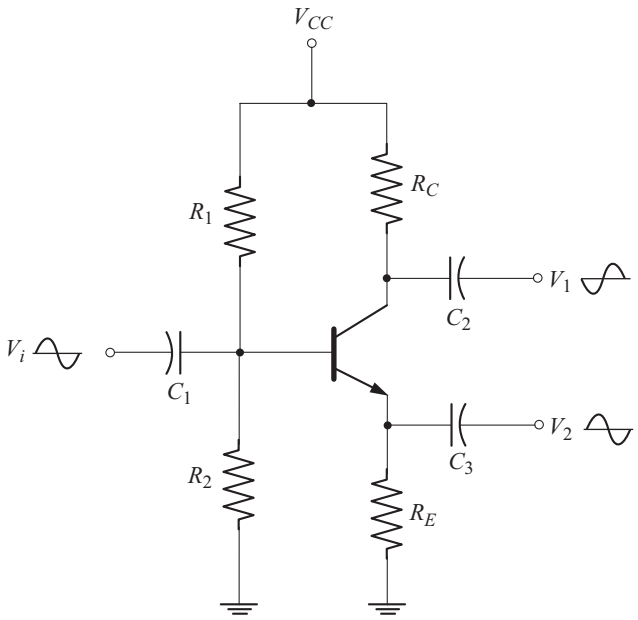


Fig. 7.18 BJT phase splitting circuit

Due to voltage follower action,

$$V_2 \approx V_i$$

Since the emitter resistor is unbypassed, the voltage gain of the CE stage is

$$\frac{V_1}{V_i} \approx -\frac{R_C}{R_E}$$

If R_C is taken equal to R_E, then

$$V_1 \approx -V_i \tag{7.104}$$

Note that V_1 and V_i are equal in magnitude but opposite in phase. Thus the voltages V_1 and V_2 are equal in magnitude with 180° phase shift between them. Another phase splitting circuit using op-amp is shown in Fig. 7.19.

The inverting amplifier introduces 180° phase shift where as the phase shift introduced by the voltage follower is zero degrees. Thus V_1 and V_2 are 180° outof phase.

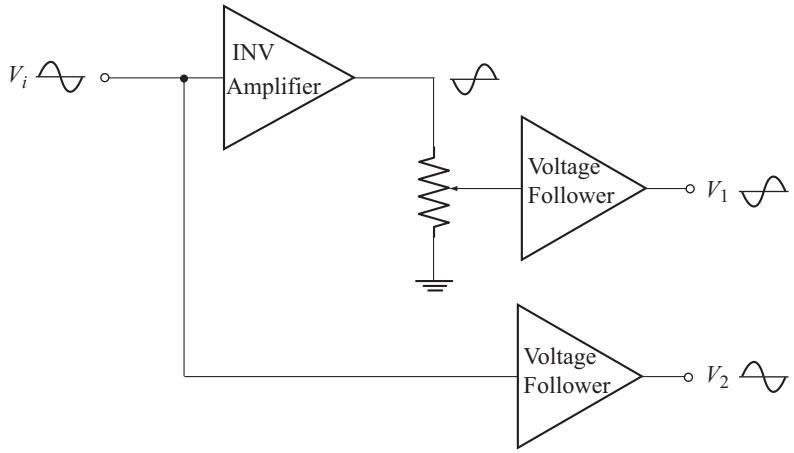


Fig. 7.19 Phase splitting network using op-amp

7.6.3 Conversion Efficiency of Class B Push-pull Power Amplifier

Assuming that the dynamic transfer curve is linear, the output waveforms can be constructed as shown in Fig. 7.20 for a single transistor, say Q_1.

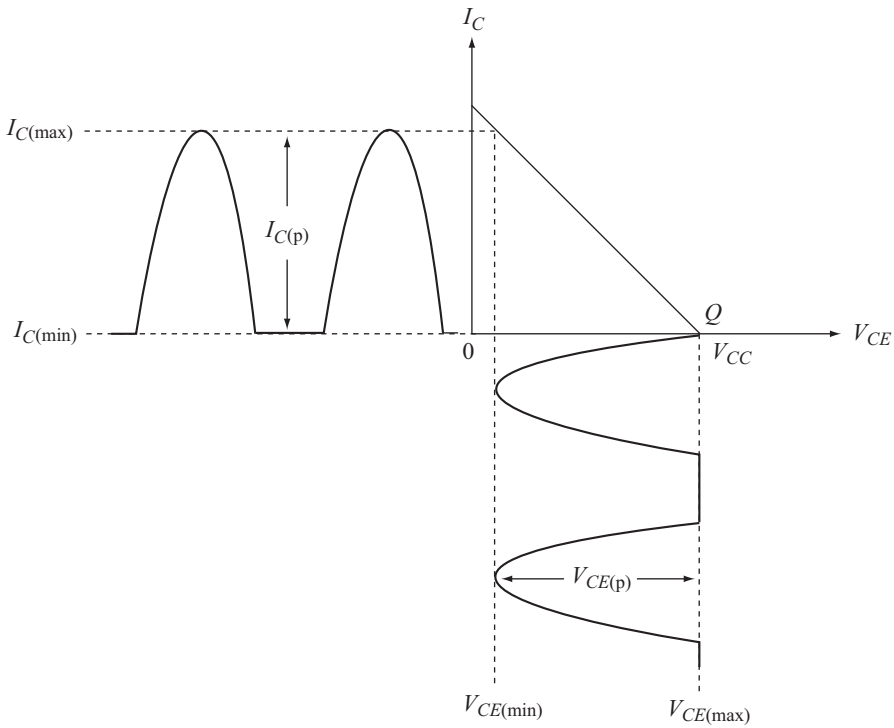


Fig. 7.20 Output voltage and current waveforms in a single transistor of class B push-pull amplifier

The conversion efficiency is given by

$$\% \eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\% \tag{7.105}$$

AC Output Power [$P_{o(\text{ac})}$]

$$P_{o(\text{ac})} = \frac{V_{CE(p)} I_{C(p)}}{2} \tag{7.106}$$

From Fig. 7.20, $V_{CE(p)} = V_{CE(\max)} - V_{CE(\min)}$

But $V_{CE(\max)} = V_{CC}$

$\therefore$ $V_{CE(p)} = V_{CC} - V_{CE(\min)}$ (7.107)

DC input power [$P_{i(\text{dc})}$]

The dc power input to the power amplifier is given by

$$P_{i(dc)} = V_{CC} I_{dc} \tag{7.108}$$

where I_{dc} is the average or the dc current drawn from the power supply V_{CC}. Note that the collector current waveform of each transistor is a half rectified sinusoid with a peak value, $I_{C(p)}$.

Thus the average current in each transistor is $\frac{I_{C(p)}}{\pi}$. Since there are two transistors, the dc current drawn from the supply V_{CC}, by both the transistors is

$$\therefore \quad I_{dc} = 2 \text{ [average current in each transistor]}$$

$$= \frac{2 I_{C(p)}}{\pi} \tag{7.109}$$

Using this relation in Equation (7.108) we have

$$P_{i(dc)} = \frac{2}{\pi} V_{CC} I_{C(p)} \tag{7.110}$$

Using Equations (7.106) and (7.110) in Equation (7.105) we get

$$\% \eta = \frac{\left(\frac{V_{CE(p)} I_{C(p)}}{2} \right)}{\frac{2}{\pi} V_{CC} I_{C(p)}} \times 100\%$$

$$\% \eta = \frac{\pi}{4} \frac{V_{CE(p)}}{V_{CC}} \times 100\% \tag{7.111}$$

Efficiency is maximum when

$$V_{CE(p)} = V_{CC} \tag{7.112}$$

This condition occurs when

$$V_{CE(\min)} = 0 \quad \text{[From equation 7.107]}$$

Using Equation (7.112) in Equation (7.111) we have

$$\%\,\eta_{\max} = \frac{\pi}{4} \times 100\,\% = 78.54\,\% \tag{7.113}$$

Observe that the efficiency is higher than that of class A transformer coupled power amplifier which is 50%. This increase in the efficiency results from the fact that in the class B push-pull power amplifier, under no signal condition, there is no power dissipation since $I_{CQ} = 0$ and therefore no current is drawn from V_{CC}.

7.6.4 Power Dissipated by Output Transistors

In class B push-pull power amplifier, the dc power drawn from the source, V_{CC}, is equal to the sum of the ac power developed at the collector and the power dissipated in the collector circuit of the output transistors.

$$P_{i(dc)} = P_{o(\text{ac})} + P_{2Q} \tag{7.114}$$

or

$$P_{2Q} = P_{i(dc)} - P_{o(\text{ac})} \tag{7.115}$$

where P_{2Q} is the power dissipated by the two output power transistors. The power dissipated by each transistor is then

$$P_Q = \frac{P_{2Q}}{2} \tag{7.116}$$

P_{2Q} is also called as the collector dissipation, since the power is dissipated in the collector circuit of the transistors.

7.6.5 Maximum Power Considerations

Now let us calculate the maximum ac output power, maximum dc input power and maximum power dissipation in the output transistors.

Maximum ac Output Power

The ac output power is given by

$$P_{o(\text{ac})} = \frac{V_{CE(p)}\, I_{C(p)}}{2} \tag{7.117}$$

where,

$$I_{C(p)} = \frac{V_{CE(p)}}{R'_L} \tag{7.118}$$

where, R_L' is the load resistance reflected to primary.
Using Equation (7.118) in (7.117), we get

$$P_{o(\text{ac})} = \frac{V_{CE(p)}^2}{2R'_L} \tag{7.119}$$

The ac output power is maximum when, $V_{CE(p)} = V_{CC}$. Now the maximum ac output power is

$$P_{o(\text{ac})\max} = \frac{V_{CC}^2}{2R_L'} \tag{7.120}$$

The corresponding peak ac current is

$$I_{C(p)} = \frac{V_{CC}}{R_L'} \tag{7.121}$$

Maximum dc Power Input

The dc input power is given by

$$P_{i(dc)} = V_{CC} I_{dc} \tag{7.122}$$

where $I_{dc} = \frac{2}{\pi} I_{C(p)}$

I_{dc} is maximum when $I_{C(p)} = \frac{V_{CC}}{R_L'}$

Now the maximum dc current is

$$I_{dc(\max)} = \frac{2}{\pi} \frac{V_{CC}}{R'_L} \tag{7.123}$$

Using this relation in Equation (7.122) we get

$$P_{i(dc)\,\max} = \frac{2}{\pi} \frac{V_{CC}^2}{R'_L} \tag{7.124}$$

Maximum Circuit Efficiency

$$\%\,\eta_{\max} = \frac{P_{o(\text{ac})\max}}{P_{i(\text{dc})\max}} \times 100\%$$

$$= \frac{\frac{V_{CC}^2}{2R_L'}}{\frac{2}{\pi}\frac{V_{CC}^2}{R_L'}} \times 100\%$$

$$\%\,\eta_{\max} = \frac{\pi}{4} \times 100\% = 78.54\% \tag{7.125}$$

Note that to obtain maximum efficiency, the input signal should result in maximum output swing i.e., $V_{CE(p)} = V_{CC}$. Otherwise efficiency will be less than 78.54%.

Maximum Power Dissipation

For class B operation, the maximum power dissipated by the two output transistors occurs when

$$V_{CE(p)} = \frac{2}{\pi} V_{CC} = 0.636\, V_{CC} \tag{7.126}$$

The maximum power dissipation is given by

$$P_{2Q(\max)} = \frac{2\,V_{CC}^2}{\pi^2\,R_L'} \tag{7.127}$$

These results are derived in example (7.27).

It is important to note that

- Maximum ac output power occurs when $V_{CE(p)} = V_{CC}$
- Maximum power dissipation in the output transistors occurs when $V_{CE(p)} = 0.636\,V_{CC}$

Thus maximum power dissipation in the output transistors does not occur when the ac output power is maximum but it occurs at an ac output power which is less than its maximum value.

Example 7.27

Show that in class B push pull power amplifier:

(a) The maximum power dissipated by the two output transistors occurs when

$$V_{CE(p)} = 0.636\,V_{CC}$$

(b) The maximum transistor power dissipation is,

$$P_{2Q(\max)} = \frac{2\,V_{CC}^2}{\pi^2\,R_L'}$$

(c) $$P_{2Q(\max)} = 0.4\,P_{o(\text{ac})\,\max}$$

Solution

(a) In class B push-pull power amplifier, the dc power drawn from the source V_{CC} is the sum of the ac power developed at the collector and the power dissipated in the collector circuit.

$$P_{i(dc)} = P_{o(\text{ac})} + P_{2Q} \tag{A}$$

where P_{2Q} is the power dissipated in the collector circuit

$$\therefore \quad P_{2Q} = P_{i(dc)} - P_{o(\text{ac})} \tag{B}$$

From Equation (7.110)

$$P_{i(dc)} = \frac{2}{\pi}\,V_{CC}\,I_{C(p)}$$

But $$I_{C(p)} = \frac{V_{CE(p)}}{R_L'}$$

$$\therefore \quad P_{i(dc)} = \frac{2\,V_{CC}\,V_{CE(p)}}{\pi R_L'} \tag{C}$$

Also $$P_{o(\text{ac})} = \frac{V_{CE(p)}\,I_{C(p)}}{2}$$

$$\text{or} \qquad P_{o(\text{ac})} = \frac{V_{CE(p)}^2}{2\,R'_L} \tag{D}$$

Substituting equations (C) and (D) in Equation (B).

$$P_{2Q} = \frac{2V_{CC}\,V_{CE(p)}}{\pi\,R'_L} - \frac{V_{CE(p)}^2}{2\,R'_L} \tag{E}$$

Collector dissipation is zero under the folllowing two conditions

1. When $V_{CE(p)} = 0$

This happens under zero signal condition

2. When $\dfrac{2V_{CC}\,V_{CE(p)}}{\pi\,R'_L} = \dfrac{V_{CE(p)}^2}{2\,R'_L}$

$$\Rightarrow \qquad V_{CE(p)} = \frac{4}{\pi}\,V_{CC}$$

Thus, the collector dissipation is zero at $V_{CE(p)} = 0$ and $V_{CE(p)} = \dfrac{4}{\pi}V_{CC}$. The maximum collector dissipation occurs at a value of $V_{CE(p)}$ in the range $0 < V_{CE(p)} < \dfrac{4}{\pi}\,V_{CC}$

Let us now find the value of $V_{CE(p)}$ corresponding to maximum power dissipation by setting

$$\frac{dP_{2Q}}{dV_{CE(p)}} = 0$$

From Equation (E)

$$\frac{dP_{2Q}}{dV_{CE(p)}} = \frac{2\,V_{CC}}{\pi\,R'_L} - \frac{V_{CE(p)}}{R'_L} = 0$$

$$\therefore \qquad V_{CE(p)} = \frac{2\,V_{CC}}{\pi} = 0.636\,V_{CC} \tag{F}$$

(b) The maximum collector dissipation, $P_{2Q\ \max}$ is obtained by substituting Equation (F) in Equation (E)

$$P_{2Q\,\max} = \frac{2V_{CC}}{\pi\,R'_L}\left(\frac{2V_{CC}}{\pi}\right) - \left(\frac{1}{2\,R'_L}\right)\left(\frac{2V_{CC}}{\pi}\right)^2$$

$$= \frac{4\,V_{CC}^2}{\pi^2\,R'_L} - \frac{2\,V_{CC}^2}{\pi^2\,R'_L}$$

$$\therefore \qquad P_{2Q\ (\max)} = \frac{2\,V_{CC}^2}{\pi^2\,R'_L} \tag{G}$$

Using Equation (E), the plot of P_{2Q} versus $V_{CE(p)}$ is shown in Fig. A.

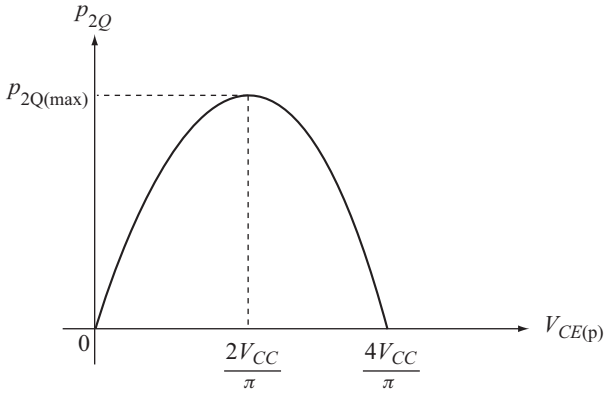


Fig. A Plot of P_{2Q} versus $V_{CE(p)}$ for class B push-pull power amplifier

From Fig. A, we observe that

(i) At zero signal ($V_{CE(p)} = 0$) collector dissipation is zero

(ii) The collector dissipation increases and reaches a maximum when $V_{CE(p)} = \frac{2V_{CC}}{\pi}$

(iii) The collector dissipation then decreases and becomes zero once again when $V_{CE(p)} = \frac{4V_{CC}}{\pi}$

(c) From Equation (7.120)

$$P_{o(\text{ac})\max} = \frac{V_{CC}^2}{2R_L'} \tag{H}$$

From equations (G) and (H)

$$\frac{P_{2Q(\max)}}{P_{o(\text{ac})\max}} = \frac{\left(\frac{2V_{CC}^2}{\pi^2 R_L'}\right)}{\left(\frac{V_{CC}^2}{2R_L'}\right)} = \frac{4}{\pi^2}$$

$$\therefore \quad \frac{p_{2Q(\max)}}{p_{o(\text{ac})\max}} \approx 0.4$$

or $$P_{2Q(\max)} = 0.4\, P_{o(\text{ac})\max} \tag{I}$$

We are now going to make a very interesting observation. Suppose it is required to deliver a maximum of 20 W to the load from a class B push-pull power amplifier. From Equation (I), the maximum collector dissipation is 8 W, which is equally shared by Q_1 and Q_2. Thus, the collector dissipation in each transistor is 4 W, which is 1/5 of the total ac power delivered to the load.

Thus in class B push-pull power amplifier, the ac power delivered to the load is five times the collector dissipation in each transistor.

7.6.6 Class B Push-pull Power Amplifier using Complementary Symmetry Transistor Pair

Figure 7.21 shows the circuit of class B push-pull power amplifier using complementary symmetry transistor pair. Q_1 is an npn transistor and Q_2 is a pnp transistor. The transistors Q_1 and Q_2 are assumed to have identical characteristics. Note that both the transistors are biased at cut-off, since no dc bias is applied to the base-emitter circuit.

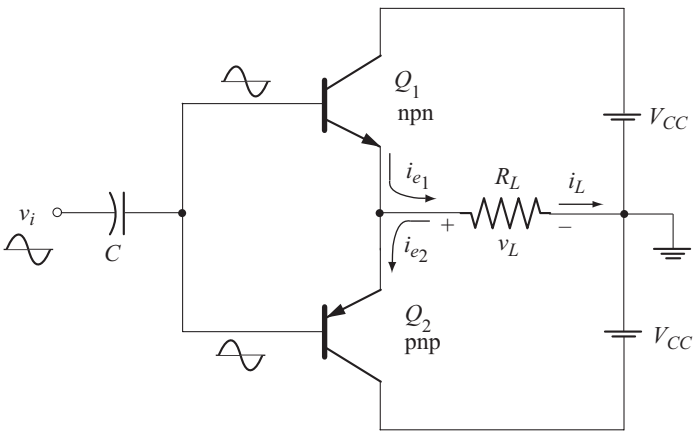


Fig. 7.21 Complementary symmetry push-pull circuit

During the positive half cycle of the input signal v_i, Q_1 will be biased in to conduction and Q_2 remains off.

$$\therefore \qquad i_L = i_{e_1}$$

The negative half cycle of v_i, biases Q_2 into conduction and Q_1 remains off.

$$\therefore \qquad i_L = -i_{e_2}$$

Combining these,

$$i_L = \begin{cases} i_{e_1} & \text{for } 0 \le \omega t \le \pi \\ -i_{e_2} & \text{for } \pi \le \omega t \le 2\pi \end{cases} \tag{7.128}$$

It is important to note that, both Q_1 and Q_2 are operating as emitter followers, with a voltage gain nearing unity. As a result the load voltage is essentially the same as the input voltage.

The analysis given in sections 7.6.3 to 7.6.5 for transformer coupled class B push-pull power amplifier can be directly applied to this circuit. Since the circuit operates without output transformer we have to apply the following modifications.

$$V_{CE\,(p)} = V_{L(p)}$$

$$I_{C\,(p)} = I_{L\,(p)}$$

and $$R'_L = R_L$$

The output voltage and current waveforms are same as that given in Fig. 7.17 for transformer coupled class B push-pull power amplifier, with i_{c_1} and i_{c_2} replaced by i_{e_1} and i_{e_2} respectively.

The advantages of this circuit are:

Due to the absence of input and output transformers the circuit is

- Simple
- Less expensive
- Less bulky and
- light weight.

The main drawbacks of this circuit are:

- The circuit requires two dc power supplies.
- Since both transistors are biased at cut-off cross over distortion is present.
- It is very difficult to get matched transistor pair.
- Poor impedance matching due to the absence of output transformer.
- Even harmonic distortion may be expected if the two transistors are not perfectly matched.
- The ripple content of the dc supply, which is present due to inadequate filtering, will reach the load.

7.6.7 Practical Complementary-Symmetry Class B Push-pull Circuit using Darlington Transistors

Figure 7.22 shows the circuit of practical complementary-symmetry class B push-pull circuit using darlington transistors. During the positive half cycle of v_i, the npn Darlington transistor conducts and the *pnp* Darlington transistor conducts for the negative half cycle of v_i. The waveforms of Fig. 7.17 applies to this circuit also.

The main features of this circuit are:

- The biasing resistors R_1 and R_2 keep the Darlington transistors in the verge of conduction. As a result, cross over distortion is absent.
- The low output impedance of the Darlington transistors properly match the low impedance of the load which is usually a loud speaker.
- The Darlington transistors provide higher output current.
- A small amount of negative feedback provided through the emitter resistors R_E (typically 1 Ω) helps to keep the harmonic distortion at a minimum.

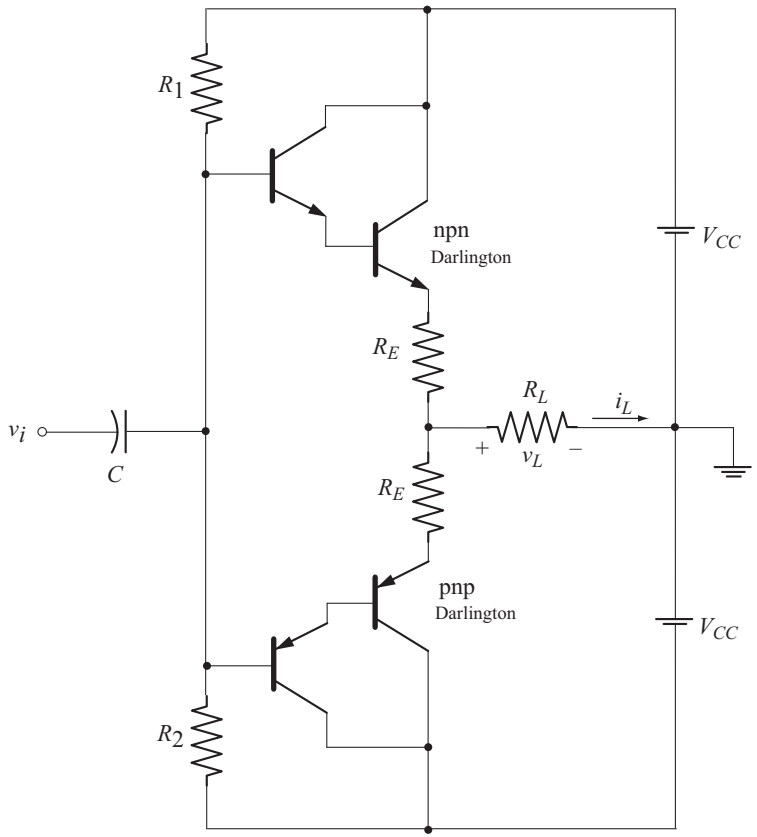


Fig. 7.22 Circuit of practical complementary-symmetry class B push-pull circuit

7.6.8 Quasi-Complementary Class B Push-pull Power Amplifier

A practical power amplifier is required to deliver large current in to low impedance load. The current driving capacity of a pnp transistor is less than that of npn transistor. Hence it is preferable to use npn transistors for both high-current-output devices.

Figure 7.23 shows the circuit of quasi-complementary push-pull class B power amplifier. The push pull operation is provided by the complementary transistors Q_1 and Q_2. Q_3 and Q_4 are the matched output transistors.

During the positive half cycle of the input signal v_i, Q_1 is driven into conduction while Q_2 remains off. The load current is supplied by the Darlington transistor consisting of Q_1 and Q_3.

During the negative half cycle of v_1, Q_2 is driven into conduction while Q_1 remains off. Now the feedback pair comprising of Q_2 and Q_4 supplies the load current.

Biasing resistors R_1, R_2 and R_3 keeps the Darlington pair and the feedback pair in the verge of conduction. Resistor R_2 can be adjusted to minimize cross over distortion.

Both the Darlington pair and the feedback pair operates with low output impedance. This ensures a proper impedance matching between the amplifier output and the load. The quasi-complementary push-pull amplifier is the most popular form of power amplifier. The waveforms given in Fig. 7.17 are also applicable to this circuit.

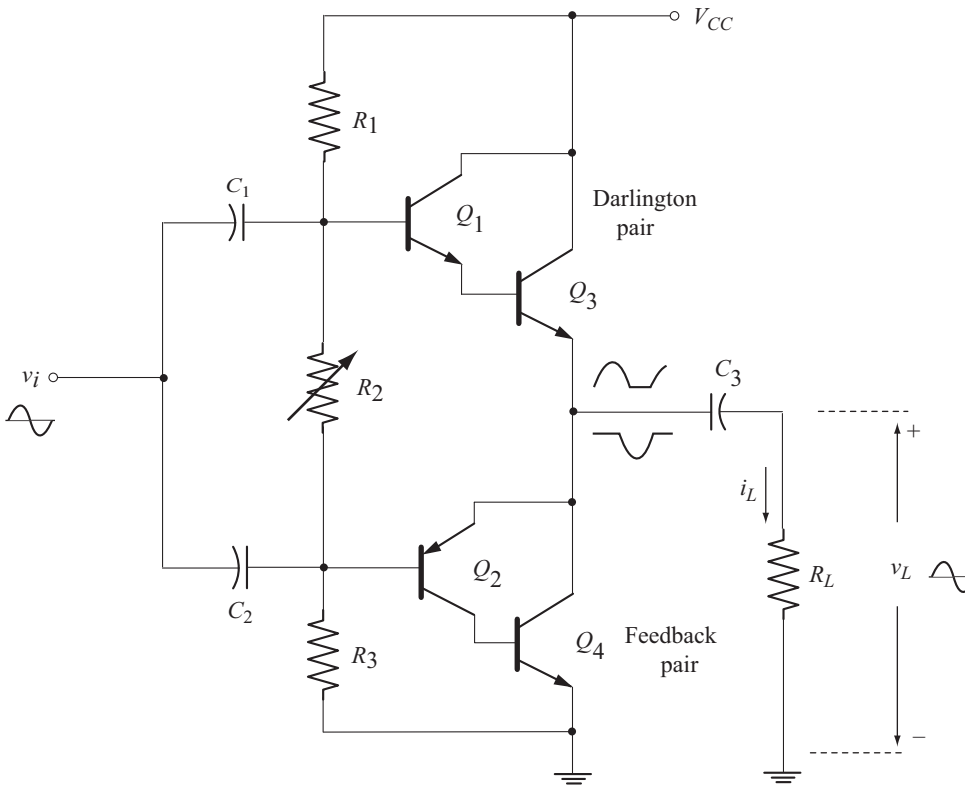


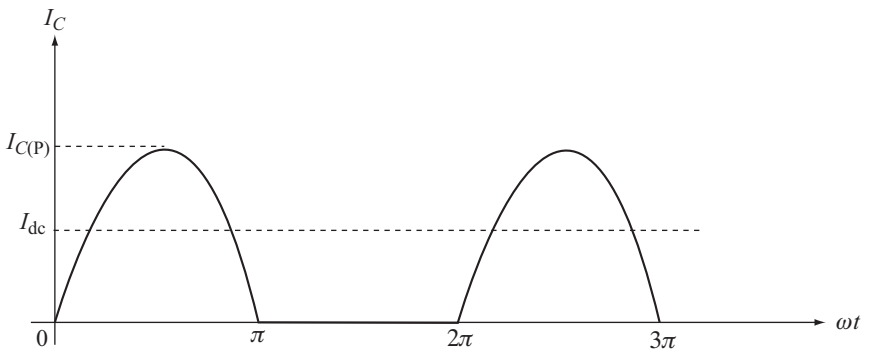
Fig. 7.23 Quasi-complementary class B push-pull power amplifier

Example 7.28

A single transistor is operating as an ideal class B amplifier with 1 kΩ load. A dc meter in the circuit reads 10 mA. How much signal power is delivered to the load.

Solution

Since a single transistor is being used, the collector current waveform is shown below.



Given $I_{dc} = 10$ mA

$R_L = 1$ kΩ

Since I_C is a half rectified sine wave.

$$I_{dc} = \frac{I_{C(p)}}{\pi}$$

$$\therefore \quad I_{C(p)} = \pi I_{dc} = 31.4 \text{ mA}$$

Power delivered to the load,

$$P_{o(\text{ac})} = I^2_{C\,(\text{rms})} R'_L$$

Since the output transformer is not specified, assume

$$R'_L = R_L$$

For half rectified sine wave,

$$I_{C(\text{rms})} = \frac{I_{C(\text{p})}}{2}$$

$$\therefore \quad P_{o(\text{ac})} = \frac{I^2_{C(p)}}{4} \times R_L = \frac{(31.4\,\text{mA})^2\,(1\text{k}\Omega)}{4}$$

or $P_{o(\text{ac})} = 0.246$ W.

Example 7.29

An ideal class B push–pull power amplifier with input and output transformers, has $V_{CC} = 20$ V, $N_2 = 2\ N_1$ and $R_L = 20\ \Omega$. The transistors have $h_{FE} = 20$. Let the input be sinusoidal. For the maximum output signal at $V_{CE(p)} = V_{CC}$, determine:

(a) the output signal power
(b) the collector dissipation in each transistor
(c) conversion efficiency

Solution

Refer Fig. 7.16

Given $V_{CC} = 20$ V

$R_L = 20\ \Omega$

$N_2 = 2N_1$

or $\frac{N_1}{N_2} = 0.5$

$V_{CE(p)} = V_{CC} = 20$ V

(a) $$P_{o(\text{ac})} = \frac{V_{CE(p)}^2}{2\,R_L'} \quad \text{(A)}$$

$$R_L' = \left(\frac{N_1}{N_2}\right)^2 R_L = 0.5^2 \times 20\ \Omega = 5\ \Omega$$

From Equation (A)

$$P_{o(\text{ac})} = \frac{(20\,\text{V})^2}{(2)(5\,\Omega)} = 40\ \text{W}$$

(b) $$P_{2Q} = P_{i(dc)} - P_{o(\text{ac})} \quad \text{(B)}$$

$$P_{i(dc)} = \frac{2}{\pi}\, V_{CC}\, I_{C(P)}$$

Using $$I_{C(p)} = \frac{V_{CE(p)}}{R_L'} = \frac{V_{CC}}{R_L'}$$

We get, $$P_{i(dc)} = \frac{2}{\pi}\,\frac{V_{CC}^2}{R_L'} = \frac{2}{\pi}\,\frac{(20\,\text{V})^2}{5\,\Omega} = 50.93\ \text{W}$$

From Equation (B),

$$P_{2Q} = 50.93\ \text{W} - 40\ \text{W} = 10.93\ \text{W}$$

$$P_Q = \frac{P_{2Q}}{2} = \frac{10.93\ \text{W}}{2} = 5.46\ \text{W}$$

(c) $$\%\,\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\,\% = \frac{40\,\text{W}}{50.93\,\text{W}} \times 100\,\%$$

$$\%\,\eta = 78.54\,\%\ \text{as expected}$$

Example 7.30

A class B push-pull amplifier operating with $V_{CC} = 25$ V provides a 22 V peak signal to an 8 Ω load. Find

(a) rms and peak load (output) currents.
(b) rms and peak collector currents.
(c) dc current drawn from the supply
(d) Input power
(e) Output power
(f) Circuit efficiency
(g) Power dissipation in the transistors

Solution

Given

$$V_{CC} = 25\ \text{V}$$

$$V_{L(p)} = 22\ \text{V (peak load voltage)}$$

$$R_L = 8\Omega$$

Note that the output transformer is not specified. For transformer less class B power amplifier

$$\begin{aligned} V_{CE(p)} &= V_{L(p)} \\ I_{C(p)} &= I_{L(p)} \\ R'_L &= R_L \end{aligned}$$

(a) peak load current is

$$I_{L(p)} = \frac{V_{L(p)}}{R_L} = \frac{22\,\text{V}}{8\Omega} = 2.75\ \text{A}$$

rms load current is

$$I_{L(\text{rms})} = \frac{I_{L(p)}}{\sqrt{2}} = \frac{2.75\,\text{A}}{\sqrt{2}} = 1.945\ \text{A}$$

(b) rms and peak collector currents are same as rms and peak load currents

$$\therefore \quad \begin{aligned} I_{C(\text{rms})} &= I_{L(\text{rms})} = 1.945\ \text{A} \\ I_{C(p)} &= I_{L(p)} = 2.75\ \text{A} \end{aligned}$$

(c) dc current drawn from the supply is

$$I_{dc} = \frac{2}{\pi} I_{C(p)} = \frac{2}{\pi} (2.75\ \text{A}) = 1.75\ \text{A}$$

dc current drawn by each transistor $= \frac{I_{dc}}{2} = 0.875\ \text{A}$

(d) Input power refers to the dc input power.

$$P_{i(dc)} = V_{CC} I_{dc} = (25\ \text{V})\ (1.75\ \text{A}) = 43.75\ \text{W}$$

(e) Output power refers to ac output power

$$P_{o(\text{ac})} = \frac{V_{CE(p)} I_{C(p)}}{2} = \frac{(22\,\text{V})(2.75\,\text{A})}{2} = 30.25\ \text{W}$$

(f) Circuit efficiency refers to conversion efficiency

$$\%\,\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\,\% = \frac{30.25\,\text{W}}{43.75\,\text{W}} \times 100\,\% = 69.143\,\%.$$

(g) Power dissipation in the output transistors is

$$P_{2Q} = P_{i(dc)} - P_{o(\text{ac})} = 43.75\ \text{W} - 30.25\ \text{W} = 13.5\ \text{W}$$

Power dissipation in each transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{13.5\,\text{W}}{2} = 6.75\ \text{W}$$

Example 7.31

For a class B push-pull power amplifier with $V_{CC} = 25$ V driving an 8 Ω load, find

(a) Maximum input power
(b) Maximum output power
(c) Maximum circuit efficiency
(d) Maximum collector dissipation and
(e) The input voltage at which maximum power dissipation occurs.

Solution

Given

$$V_{CC} = 25 \text{ V}$$
$$R_L = 8\ \Omega$$

Since output transformer is not specified, assume

$$R'_L = R_L = 8\ \Omega$$

(a) From Equation (7.124), the maximum input power is

$$P_{i(dc)\max} = \frac{2}{\pi}\frac{V_{CC}^2}{R'_L} = \frac{2}{\pi}\frac{(25\text{V})^2}{8\Omega} = 49.74 \text{ W}$$

(b) From Equation (7.120) the maximum output power is

$$P_{o(\text{ac})\max} = \frac{V_{CC}^2}{2\,R'_L} = \frac{(25\text{V})^2}{(2)(8\Omega)} = 39.06 \text{ W}$$

(c) Maximum circuit efficiency is

$$\%\,\eta_{\max} = \frac{P_{o(\text{ac})\max}}{P_{i(\text{dc})\max}} \times 100\,\%$$
$$= \frac{39.06 \text{ W}}{49.74 \text{ W}} \times 100\,\% = 78.53\,\% \text{ as expected}$$

(d) From Equation (7.127), the maximum collector dissipation is

$$P_{2Q(\max)} = \frac{2}{\pi^2}\frac{V_{CC}^2}{R'_L} = \frac{2}{\pi^2}\frac{(25\text{V})^2}{8\Omega} = 15.83 \text{ W}$$

Maximum collector dissipation in each transistor is

$$P_{Q(\max)} = \frac{P_{2Q(\max)}}{2} = \frac{15.83\text{W}}{2} = 7.915 \text{ W}$$

(e) From Equation (7.126), the input voltage at which maximum power dissipation occurs is

$$V_{i(p)} = V_{CE(p)} = (0.636)\ V_{CC}$$
$$= (0.636)\ (25 \text{ V}) = 15.9 \text{ V}$$

Example 7.32

Calculate the efficiency of class B push-pull power amplifier for a supply voltage of $V_{CC} = 22$ V, driving a 4 Ω load with peak output voltages of

(a) $V_{L(p)} = 22$ V
(b) $V_{L(p)} = 20$ V
(c) $V_{L(p)} = 4$ V
(d) Compare and comment on the results.

Solution

Given $V_{CC} = 22$ V

Since output transformer is not specified

$$R'_L = R_L = 4\ \Omega$$

From Equation (7.111),

$$\%\,\eta = \frac{\pi}{4}\,\frac{V_{CE(p)}}{V_{CC}} \times 100\,\%$$

For transformerless circuit, $V_{CE(p)} = V_{L(p)}$

$$\therefore \quad \%\,\eta = \frac{\pi}{4}\,\frac{V_{L(p)}}{V_{CC}} \times 100\,\% \qquad \text{(A)}$$

(a) $V_{L(p)} = 22$ V

$$\%\,\eta = \frac{\pi}{4}\left[\frac{22\,\text{V}}{22\,\text{V}}\right]100\,\% = 78.54\,\%$$

(b) $V_{L(p)} = 20$ V

$$\%\,\eta = \frac{\pi}{4}\left[\frac{20\,\text{V}}{22\,\text{V}}\right] \times 100\,\% = 71.4\,\%$$

(c) $V_{L(p)} = 4$ V

$$\%\ \eta = \frac{\pi}{4}\left[\frac{4\,\text{V}}{22\,\text{V}}\right] \times 100\,\% = 14.27\,\%$$

(d) Observe from Equation (A) that, efficiency increases with $V_{L(p)}$ and becomes maximum i.e., 78.54 % when $V_{L(p)} = V_{CC}$

Example 7.33

In a class B amplifier, $V_{CE(\min)} = 1$ V and $V_{CC} = 18$ V. Calculate the collector circuit efficiency.

Solution

Given $V_{CC} = 18$ V $\quad V_{CE(\min)} = 1$ V

$$\%\,\eta = \frac{\pi}{4}\,\frac{V_{CE(p)}}{V_{CC}} \times 100\,\%$$

From Equation (7.107),

$$V_{CE(p)} = V_{CC} - V_{CE(\min)}$$
$$= 18\text{ V} - 1\text{ V} = 17\text{ V}$$

Now
$$\%\,\eta = \frac{\pi}{4}\,\frac{17\text{ V}}{18\text{ V}} \times 100\% = 74.18\,\%$$

Example 7.34

Calculate the power dissipated in the individual transistors of a class B push-pull power amplifier if $V_{CC} = 20$ V and $R_L = 4\ \Omega$.

Solution

Given
$$V_{CC} = 20\text{ V}$$

Since output transformer is not specified,

$$R'_L = R_L = 4\ \Omega$$

Collector dissipation

$$P_{2Q} = P_{i(dc)} - P_{o(\text{ac})} \qquad \text{(A)}$$

Since the output signal amplitude is not given, let us assume maximum power output

$$\therefore \quad V_{CE(p)} = V_{CC}$$

$$P_{o(\text{ac})} = \frac{V_{CE(p)}^2}{2R'_L} = \frac{V_{CC}^2}{2R_L} = \frac{(20\text{ V})^2}{(2)(4\Omega)} = 50\text{ W}$$

$$P_{i(dc)} = \frac{2}{\pi}\,V_{CC}\,I_{C(p)}$$

But
$$I_{C(p)} = \frac{V_{CE(p)}}{R'_L} = \frac{V_{CC}}{R_L}$$

$$\therefore \quad p_{i(dc)} = \frac{2\,V_{CC}^2}{\pi R_L} = \frac{2\times(20\text{ V})^2}{\pi\times 4\Omega} = 63.66\text{ W}$$

Substituting in Equation (A)

$$P_{2Q} = 63.66\text{ W} - 50\text{ W} = 13.66\text{ W}$$

Power dissipation in each transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{13.66\text{ W}}{2} = 6.83\text{ W}$$

Example 7.35

Calculate the peak power dissipated in each transistor of a class B push pull power amplifier if $V_{CC} = 15$ V and $R'_L = 5\ \Omega$

Solution

Given $V_{CC} = 15$ V $R'_L = 5\ \Omega$

Peak power dissipation in the output transistors is

$$P_{2Q\,(\max)} = \frac{2}{\pi^2}\ \frac{V_{CC}^2}{R'_L}$$

$$= \frac{2}{\pi^2}\ \frac{(15\,\text{V})^2}{5\ \Omega} = 9.12\ \text{W}$$

Peak power dissipation in each transistor is

$$P_{Q\,(\max)} = \frac{P_{2Q(\max)}}{2}$$

$$= \frac{9.12\,\text{W}}{2} = 4.56\ \text{W}$$

Example 7.36

A class B transformer-coupled push pull power amplifier is to supply 5W to a 18 Ω load with $V_{CC} = 30$ V. Assume transformer efficiency of 75%. Determine:

(a) Turns ratio of the output transformer
(b) Power dissipation in each transistor and
(c) Conversion efficiency

Solution

Given $V_{CC} = 30$ V

Power delivered to the load (secondary),

$$P_L = 5\ \text{W}$$

$$R_L = 18\ \Omega$$

$$\eta_{\text{TFR}} = 0.75$$

$$\eta_{\text{TFR}} = \frac{\text{Power delivered to secondary}}{\text{Power developed in primary}}$$

$$= \frac{P_L}{P_{o(\text{ac})}}$$

$$\therefore \quad P_{o\,(\text{ac})} = \frac{P_L}{\eta_{\text{TFR}}} = \frac{5\,\text{W}}{0.75} = 6.67\ \text{W}$$

(a) $$R'_L = \left[\frac{N_1}{N_2}\right]^2 R_L$$

$$\therefore \quad \frac{N_1}{N_2} = \sqrt{\frac{R'_L}{R_L}} \tag{A}$$

But $$P_{o\,(\text{ac})} = \frac{V^2_{CE(p)}}{2\,R'_L} \tag{B}$$

$$V_{CE\,(p)} = V_{CC} - V_{CE\,(\min)}$$

Taking $V_{CE(\min)} = 0$, for maximum power output,

$$V_{CE(p)} = V_{CC} = 30\ \text{V}$$

From (B) $$R'_L = \frac{V^2_{CE(p)}}{2\,P_{o(\text{ac})}} = \frac{V^2_{CC}}{2\,P_{o(\text{ac})}} = \frac{(30\,\text{V})^2}{2\times 6.67\,\text{W}} = 67.47\ \Omega$$

Substituting in (A)

$$\frac{N_1}{N_2} = \sqrt{\frac{67.47\,\Omega}{18\,\Omega}} = 1.94$$

(b) $$P_{2Q} = P_{i(dc)} - P_{o(\text{ac})} \tag{C}$$

$$P_{i(dc)} = \frac{2}{\pi}\,V_{CC}\,I_{C(p)}$$

where $$I_{C(p)} = \frac{V_{CE\,(p)}}{R'_L} = \frac{V_{CC}}{R'_L}$$

$$\therefore \quad P_{i(dc)} = \frac{2\,V^2_{CC}}{\pi\,R'_L} = \frac{2\times(30\,\text{V})^2}{\pi\times 67.47\,\Omega} = 8.5\ \text{W}$$

Substituting in (C)

$$P_{2Q} = 8.5\ \text{W} - 6.67\ \text{W} = 1.83\ \text{W}$$

$$\therefore \quad P_Q = \frac{P_{2Q}}{2} = \frac{1.83\,\text{W}}{2} = 0.92\ \text{W}$$

(c) Conversion efficiency

$$\%\,\eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\,\%$$

$$\%\,\eta = \frac{6.67}{8.5} \times 100\,\% = 78.47\,\%$$

as expected for maximum power output condition.

Example 7.37

Analyse the operation of the push pull amplifier shown in Fig. (a).

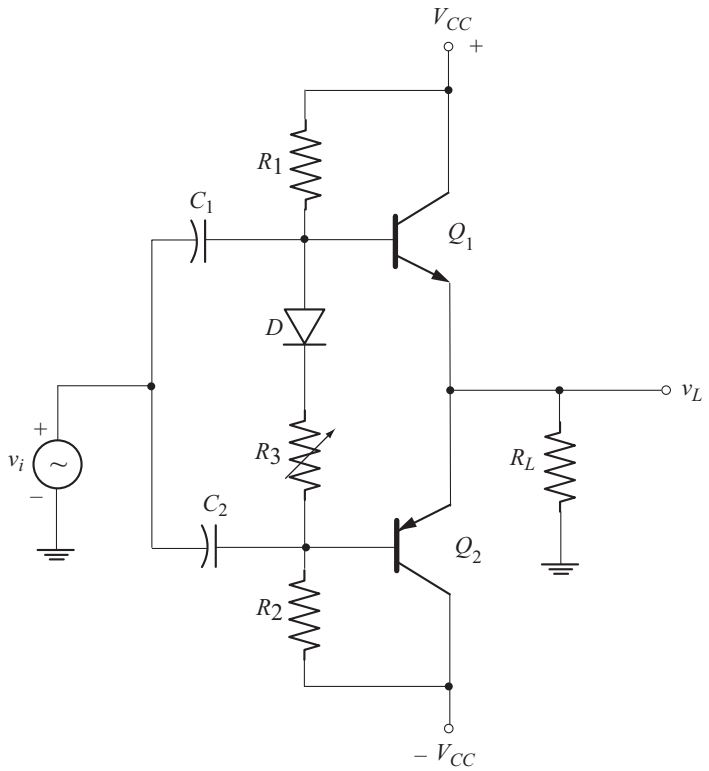


Fig. a

Solution

With R_1, R_2, R_3 and D removed, the circuit becomes class B push pull power amplifier without input and output transformer as shown in Fig. (b). Note that this circuit is complementary push-pull class B power amplifier shown in Fig. 7.21 of section 7.6.6.

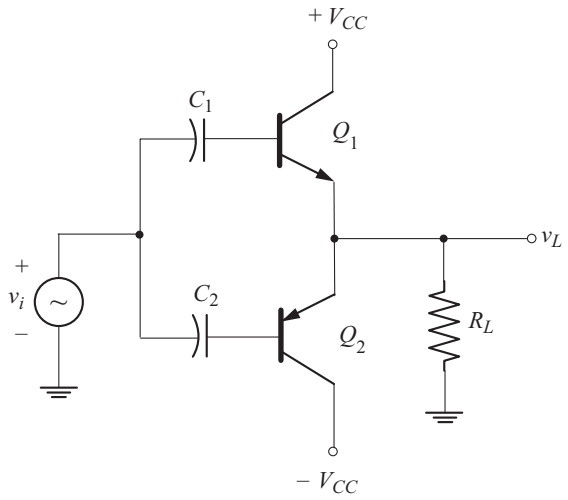


Fig. b

In the circuit of Fig. (b), since $V_{BE} = 0$ for both Q_1 and Q_2, they are biased at cut-off, which results in cross-over distortion as described in Section 7.1.3. To eliminate cross-over distortion, the transistors should be biased slightly above cut-off to an extent of the base-emitter cut in voltage, typically 0.7 V for silicon transistors.

In the given circuit of Fig. (a), the drop across diode D provides the required forward bias for the base-emitter junction of both the transistors. The diode D_2 is forward biased though resistors R_1 and R_2 connected between V_{CC} and $-V_{CC}$. R_3 is adjusted to minimize cross over distortion.

For ac operation, with reference to Fig. (a), the dc voltages $+V_{CC}$ and $-V_{CC}$ are grounded and the capacitors C_1 and C_2 are shorted. Therefore the collectors of the two transistors are at ground potential. For each transistor, the input is applied between base and ground (collector is at ground) and the output is taken between emitter and ground. Therefore, Q_1 and Q_2 act as emitter -followers. As a result, $v_o = v_i$.

Example 7.38

In the circuit of Example 7.36 Let $\pm V_{CC} = \pm 30$ V, $R_L = 8\ \Omega$, $R_1 = R_2 = R_3 = 100\ \Omega$, $C_1 = C_2 = 100\ \mu$F. If the rms input voltage is 8 V, calculate

(a) rms and peak load (output) voltages
(b) rms and peak load (output) currents
(c) dc current drawn from the supply
(d) dc input power
(e) ac output power
(f) conversion efficiency and
(g) power dissipated in each transistor

Solution

Given $\pm V_{CC} = \pm 30$ V $\Rightarrow$ $V_{CC} = 30$ V

$R'_L = R_L = 8\ \Omega$ [No output transformer]

rms input voltage $V_{i\,(\text{rms})} = 8$ V

(a) Since Q_1 and Q_2 are configured as emitter followers, as explained in Example 7.37

rms load voltage = rms input voltage.

ie. $V_{L(\text{rms})} = V_{i(\text{rms})} = 8$ V

Peak load voltage is

$$V_{L(p)} = \sqrt{2}\, V_{L(\text{rms})} = \left(\sqrt{2}\right)(8\text{ V}) = 11.31\text{ V}$$

(b) rms load current is

$$I_{L(\text{rms})} = \frac{V_{L(\text{rms})}}{R_L} = \frac{8\text{ V}}{8\,\Omega} = 1\text{ A}$$

Peak load current is

$$I_{L\,(p)} = \frac{V_{L(P)}}{R_L} = \frac{11.31\text{V}}{8\,\Omega} = 1.414\text{ A}$$

(c) dc current drawn from the supply is

$$I_{dc} = \frac{2}{\pi} I_{C(p)}$$

For transformer less circuit

$$I_{C(p)} = I_{L(p)} \text{ and}$$
$$V_{CE(p)} = V_{L(p)}$$
$$\therefore \quad I_{dc} = \frac{2}{\pi} I_{L(p)} = \frac{2}{\pi} (1.414 \text{ A}) = 0.9 \text{ A}$$

dc current through each transistor is

$$\frac{I_{dc}}{2} = \frac{0.9\text{A}}{2} = 0.45 \text{ A}$$

(d) dc input power is

$$P_{i(dc)} = V_{CC} I_{dc} = (30 \text{ V}) (0.9 \text{ A}) = 27 \text{ W}$$

(e) ac output power is

$$P_{o(\text{ac})} = \frac{V_{CE(p)} I_{C(p)}}{2} = \frac{V_{L(p)} I_{L(p)}}{2}$$
$$= \frac{(11.31\text{V})(1.414\text{A})}{2} = 8 \text{ W}$$

Alternatively, $P_{o(\text{ac})} = V_{L(\text{rms})} I_{L(\text{rms})} = (8 \text{ V}) (1 \text{ A}) = 8 \text{ W}$

(f) Conversion efficiency is

$$\% \eta = \frac{P_{o(\text{ac})}}{P_{i(\text{dc})}} \times 100\% = \frac{8\text{W}}{27\text{W}} \times 100\% = 29.63\%$$

(g) power dissipation in both transistors is

$$P_{2Q} = P_{i(dc)} - P_{o(\text{ac})} = 27 \text{ W} - 8 \text{ W} = 19 \text{ W}$$

Power dissipation in each transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{19\text{W}}{2} = 9.5 \text{ W}$$

Example 7.39

In the circuit of Example 7.37 let $V_{CC} = 30$ V, $R_L = 8\ \Omega$. Find

(a) Maximum dc input power
(b) Maximum ac output power
(c) Maximum conversion efficiency
(d) Input voltage for maximum power operation
(e) Power dissipated by the output transistors at this voltage

Solution

Given

$$V_{CC} = 30\text{ V}$$
$$R'_L = R_L = 8\ \Omega \qquad [\text{No output transformer}].$$

(a) From Equation (7.124), the maximum dc input power is

$$P_{i(dc)\,\max} = \frac{2}{\pi}\,\frac{V_{CC}^2}{R_L} = \frac{2}{\pi}\,\frac{(30\text{ V})^2}{8\Omega} = 71.62\text{ W}$$

(b) From Equation (7.120), the maximum ac output power is

$$P_{o(\text{ac})\,\max} = \frac{V_{CC}^2}{2R_L} = \frac{(30\text{ V})^2}{(2)(8\Omega)} = 56.25\text{ W}$$

(c) Maximum conversion efficiency is

$$\%\,\eta_{\max} = \frac{P_{o(\text{ac})\max}}{P_{i(\text{dc})\max}} \times 100\,\% = \frac{56.25\text{ W}}{71.62\text{ W}} \times 100\,\%$$
$$= 78.54\,\%\text{ as expected}$$

(d) Output voltage for maximum power operation is

$$V_{L(p)} = V_{CE(p)} = V_{CC} = 30\text{ V}$$

Since Q_1 and Q_2 are emitter followers, the corresponding input voltage is

$$V_{i(p)} = V_{L(p)} = 30\text{ V}$$

(e) Collector dissipation in both transistors at this input voltage is

$$P_{2Q} = P_{i(dc)\max} - P_{o(\text{ac})\max}$$
$$= 71.62\text{ W} - 56.25\text{ W} = 15.37\text{ W}$$

Power dissipation in each transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{15.37\text{ W}}{2} = 7.685\text{ W}$$

Example 7.40

For the circuit of example 7.39, calculate the maximum power dissipated by the output transistors and the input voltage at which this occurs. Comment on the result.

Solution

Given

$$V_{CC} = 30\text{ V}$$
$$R'_L = R_L = 8\ \Omega$$

From Equation (7.127), the maximum power dissipation in the output transistors is

$$P_{2Q\,(\max)} = \frac{2\,V_{CC}^2}{\pi^2\,R_L} = \frac{2\,(30\,\text{V})^2}{\pi^2(8\,\Omega)} = 22.79\ \text{W}$$

Maximum power dissipation in each transistor is

$$P_{Q(\max)} = \frac{P_{2Q(\max)}}{2} = \frac{22.79\,\text{W}}{2} = 11.395\ \text{W}$$

From Equation (7.126), the corresponding output voltage is

$$V_{L(p)} = V_{CE(p)} = 0.636\ V_{CC} = (0.636)\ (30\ \text{V}) = 19.08\ \text{V}$$

Due to emitter follower action the corresponding input voltage is

$$V_{i(p)} = V_{L(p)} = 19.08\ \text{V}$$

From the results of example 7.39, we find when $V_{i(p)} = 30$ V, the ac power output is maximum and the corresponding total power dissipation is 15.37 W.

In the present example, we found that, the total power dissipation has a maximum value of 22.79 W when $V_{i(p)} = 19.08$ V, which does not correspond to maximum power output.

Thus as stated earlier the maximum power dissipation in the output transistors does not occur when the circuit is delivering maximum power output but it occurs at an output power which is smaller than the maximum value.

◆ 7.7 CLASS D POWER AMPLIFIER

A class *D* power amplifier is designed to operate with digital or pulse-type signals. It has an efficiency of more than 90% which is highly desirable for a power amplifier. The name class *D* arises from the fact that, the circuit is designed to operate with digital or pulse-type signals.

Figure 7.24 shows the block diagram of class *D* power amplifier.The sinusoidal input signal V_i is compared with saw tooth waveform in a comparator. The comparator output switches from low to high level whenever the voltage level of sawtooth waveform goes above the voltage level of the input waveform. The comparator output switches from high to low level when the sawtooth voltage level falls below the input voltage level. Thus the output of comparator is a digital waveform as shown in Fig. 7.25.

The high output of comparator turns on the amplifiers transistor devices which are usually power BJTs or power MOSFETs. The transistors are turned off by the low output of comparator. The transistors provide output current only when they are turned on with little power loss due to their low on-state voltage. Once again the output of the amplifier is a pulse-type signal. The low-pass filter converts the pulse-type signal back to sinusoidal signal. It is important to note that the output signal is a large amplitude sinusoid whose frequency is same as the input sinusoid. The circuit operates with veryhigh efficiency since most of the power applied to the amplifier is transferred to the load. A small amount of feedback is applied to improve the linearity of the circuit.

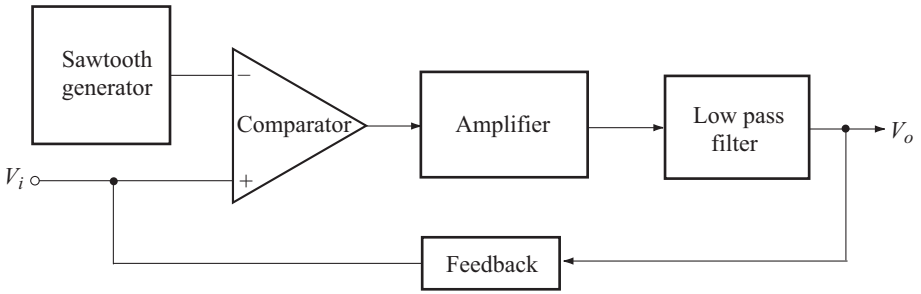


Fig. 7.24 Block diagram of class D power amplifier

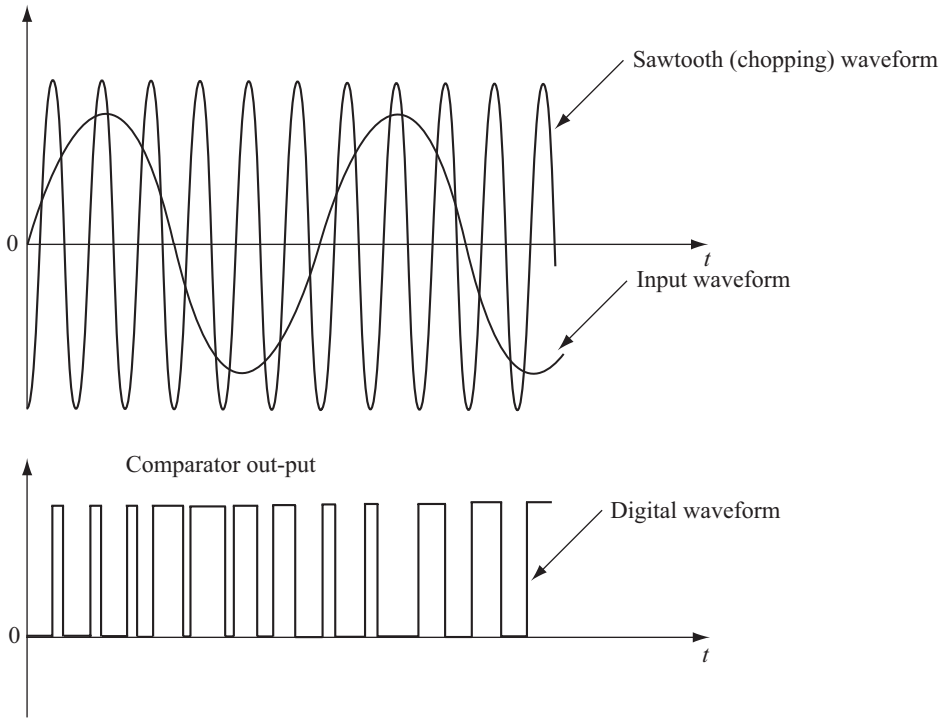


Fig. 7.25 Waveforms in class-D power amplifier

◆ 7.8 POWER TRANSISTOR HEAT SINKING

Due to power dissipation in the power transistor, the temperature of the collector-base junction rises. If the junction temperature exceeds the maximum permissible value, the transistor will get destroyed due to thermal runaway. Thus the temperature of the collector-base junction places an upper limit on the allowable power dissipation. Typical maximum junction temperature for silicon transistors is 150–200°C and for germanium transistor, it is 100 – 110°C. Note that the power dissipation capability of silicon transistors is higher than that of germanium transistor.

The average power dissipated in a transistor may be approximated by

$$P_D = V_{CE} I_C \tag{7.129}$$

It is important to note that, the power dissipation capacity of a transistor decreases with increase in junction temperature. This is called power derating. For instance, as specified in the data sheets, the maximum power dissipation of the transistor 2N1936 is 4 W at 25°C and it decreases to zero at a junction temperature of 175°C.

One way to increase the power rating of a transistor is to get rid of the heat faster. Heat sinks are used for this purpose. With heat sinks, the surface area of the transistor case increases which helps the heat to escape more easily into the surrounding air.

Figure 7.26(a) shows the push-on heat sink. When the heat sink is pushed on to the transistor case, heat radiates more quickly because of the increased surface area of the fins.

Figure 7.26(b) shows the power-tab transistor. The metal tab provides a path out of the transistor for heat. This metal tab can be fastened to the chassis of electronic equipment. Because the chassis is a massive heat sink, heat can easily escape from the transistor to the chassis.

In large power transistors, the collector is connected directly to the case as shown in Fig. 7.26(c) to allow the heat escape as easily as possible. The transistor case is then fastened to the chasis. To prevent the collector from shorting to the chassis ground, a thin insulating washer and a thermal conductive paste are used between the transistor case and the chassis.

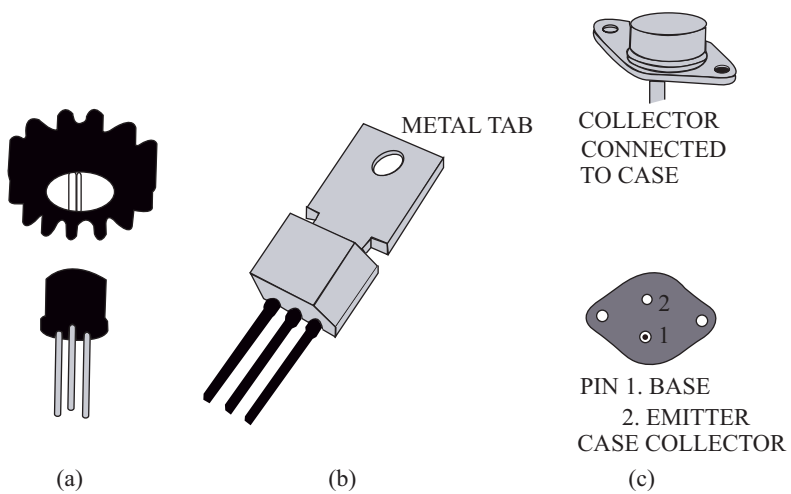


Fig. 7.26 (a) Push-on heat sink
(b) Power-tab transistor
(c) Power transistor with collector connected to case

Figure 7.27 shows a typical power derating curve for a silicon transistor. The curve shows that the power derating takes place linearly after a certain temperature specified by the manufacturer. Note that for silicon transistor the power dissipation reduces to 0 W at a case temperature of 200° C.

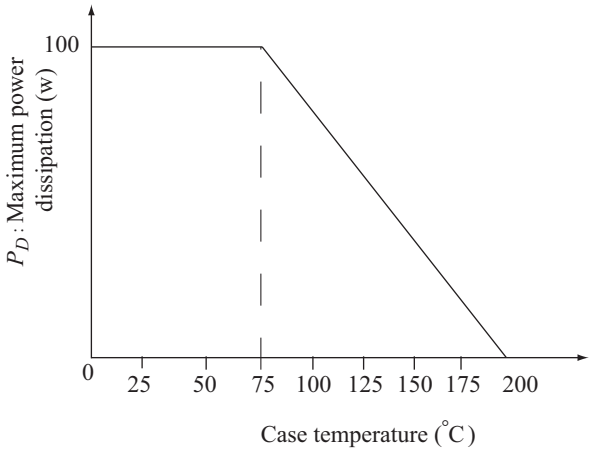


Fig. 7.27 Typical power derating curve for silicon transistor

The slope of power derating curve is called the derating factor denoted by, *D,* expressed in watts or milli watts per degree centigrade of temperature.

$$D = \frac{\text{Decrease in power rating}}{\text{Increase in case temperature}}$$

$$D = \frac{P_{D_o} - P_{D_1}}{T_1 - T_o} \tag{7.130}$$

where P_{Do} = Maximum power dissipation at temperature T_o

P_{D_1} = Maximum power dissipation at temperature T_1

For instance, From Fig. 7.27 we find that when the case temperature rises from 75 °C to 200 °C, the maximum power dissipation decreases from 100 W to 0 W.

$$\therefore \qquad D = \frac{100\,\text{W}}{200^\circ\text{C} - 75^\circ\text{C}} = 0.8\ \text{W/°C}$$

Example 7.41

A silicon transistor is rated for 100 W at 25 °C. Calculate the maximum dissipation at a case temperature of 125° C if the derating is required above 25° C with a derating factor of 0.5 W/°C.

Solution

$$P_{D_o} = 100\ \text{W} \quad T_o = 25\ °\text{C}$$

$$T_1 = 125\ °\text{C} \quad D = 0.5\ \text{W/°C}$$

$$D = \frac{P_{D_o} - P_{D_1}}{T_1 - T_o}$$

$$0.5\ \text{W/°C} = \frac{100\,\text{W} - P_{D_1}}{125^\circ\text{C} - 25^\circ\text{C}}$$

$$P_{D1} = 100\text{ W} - (100\text{ °C})\,(0.5\text{ W/°C})$$
$$= 50\text{ W}$$

Example 7.42

A silicon transistor is rated for 100 W at 25 °C. If the derating factor is 0.6 W/°C, calculate the maximum power dissipation at a case temperature of boiling temperature of water.

Solution

$P_{D_o} = 100$ W $\quad T_o = 25$ °C

$D = 0.6$ W / °C $\quad T_1 = 100$ ° C (Boiling temperature of water)

$$D = \frac{P_{D_o} - P_{D_1}}{T_1 - T_o}$$

$$0.6\text{ W / °C} = \frac{100\text{ W} - P_1}{100°\text{C} - 25°\text{C}}$$

$$P_1 = 100\text{ W} - (75\text{ °C})\,(0.6\text{ W/°C}) = 55\text{ W}$$

◆ 7.9 THERMAL ANALOGY OF A POWER TRANSISTOR

The heat produced at the collector-base junction passes through the transistor case to the heat sink and then radiates in to the surrounding air. The temperature of this air is known as the ambient temperature which is around 25 °C but it can be much higher on hot days.

Let T_J = Junction temperature

T_C = Case temperature

T_H = Heat sink temperature.

T_A = Ambient temperature.

All these temperatures are measured with respect to absolute zero.

If is found experimentally that the steady-state temperature rise at the collector junction is proportional to the power dissipated at the junction.

$$\left.\begin{aligned} &\text{ie} && T_j - T_A \propto P_D \\ &\text{or} && T_j - T_A = \theta_{JA} P_D \end{aligned}\right\} \tag{7.131}$$

$$\Rightarrow \qquad \theta_{JA} = \frac{T_j - T_A}{P_D} \tag{7.132}$$

θ_{JA} is the thermal resistance from junction to ambient (total thermal resistance). Since heat flows from junction to case, case to heat sink and then from heat sink to ambient, using electrical analogy of thermal resistances, we can write

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \tag{7.133}$$

where θ_{JC} = transistor thermal resistance (junction to case)

θ_{CS} = Insulator thermal resistance (case to heat sink)

θ_{SA} = heat-sink thermal resistance (heat sink to ambient)

Figure 7.28 Shows the electrical analogous circuit using the thermal resistances.

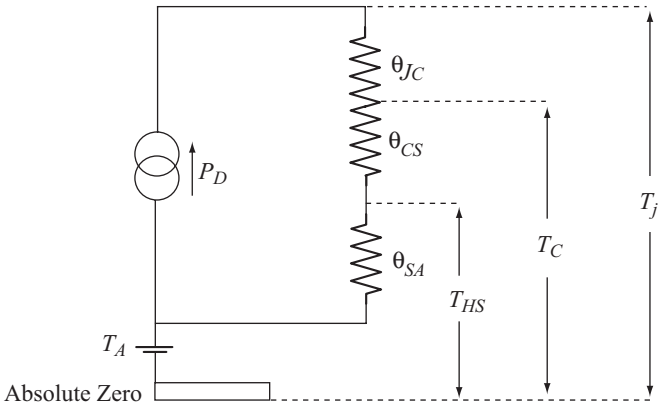


Fig. 7.28 Thermal-to-electrical analogy

From Equation (7.132)

$$T_j = P_D \theta_{JA} + T_A \tag{7.134}$$

Note that the junction temperature floats on the ambient temperature. Also higher the ambient temperature lower is the allowed value of device power dissipation. The following example illustrates how the heat sink increases the power handling capacity of the device for a given rise in junction temperature.

Example 7.43

A power transistor using heat sink is required to dissipate 50 W. The thermal resistance values are as follows.

$$\theta_{SA} = 2° \text{ C/W}$$
$$\theta_{CS} = 0.8° \text{ C/W}$$
$$\theta_{JC} = 0.5° \text{ C/W}$$

(a) Calculate the rise in Junction temperature.

(b) If $\theta_{JA} = 40°$ C/W without heat sink, what would be the rise in Junction temperature. Comment on the result.

Solution

(a) ***With heat sink***

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$
$$= 0.5°\text{ C/W} + 0.8°\text{ C/W} + 2°\text{ C/W} = 3.3°\text{ C/W}$$

Rise in Junction temperature is

$$T_j - T_A = P_D\,\theta_{JA} = (50\text{ W})\,(3.3°\text{ C/W}) = 165\ °\text{C}$$

(b) ***Without heat sink***

$$\theta_{JA} = 40°\text{ C/W}$$
$$T_j - T_A = (50\text{ W})\,(40°\text{ C/W}) = 2000°\text{ C !!!}$$

This excessive high temperature will certainly destroy the transistor.

Example 7.44

A silicon power transistor operating with heat sink has the following data.

Transistor rating: : 150 W at 25 °C
Transistor thermal resistance, θ_{JC} : 0.5°C/W
Insulator thermal resistance, θ_{CS} : 0.6° C/W
Heat-sink thermal resistance, θ_{SA} : 1.5° C/W

What maximum power can be dissipated if the ambient temperature is 40°C and $T_{j\max} = 200$ °C?

Solution

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$
$$= 0.5°\text{ C/W} + 0.6°\text{ C/W} + 1.5°\text{ C/W} = 2.6°\text{ C/W}$$
$$P_D = \frac{T_j - T_A}{\theta_{JA}} = \frac{200°\text{C} - 40°\text{C}}{2.6°\text{C/W}} = 61.54\text{ W}$$

Example 7.45

What maximum power can a silicon transistor dissipate into free air at an ambient temperature of 80° C. The junction temperature should not exceed 200° C. Take θ_{JA} 40° C/W.

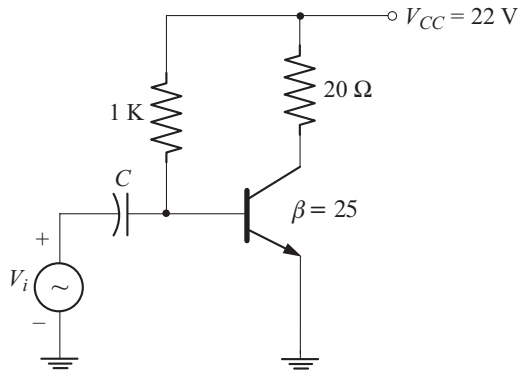
Solution

In this case the transistor operates without heat sink.

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$
$$= \frac{200°\text{C} - 80°\text{C}}{40°\text{ C/W}}$$
$$= 3\text{ W}$$

EXERCISE PROBLEMS

7.1 For the class A series-fed power amplifier shown below, calculate the dc input power, ac output power and efficiency. The input voltage v_i results in a base current of 7.07 mA(rms).



7.2 The following data is available for a class A series-fed Power amplifier.

$$V_{CE\max} = 14 \text{ V}, V_{CE\min} = 6 \text{ V}, \ I_{C\max} = 7 \text{ mA}, \ I_{C\min} = 3 \text{ mA}$$

(a) calculate the ac power delivered to the load.
(b) conversion efficiency if $V_{CC} = 10$ V and $I_C = 5$ mA.

7.3 What transformer turns ratio is required to match a 16 Ω speaker load so that the effective load resistance seen at the primary is 10 K?

7.4 A class B Power amplifier is delivering an output voltage of 10 V peak to a 8 Ω load. If the dc power supply is 30 V, calculate

(a) dc power input, (b) ac power delivered to the load. (c) conversion efficiency and (d) power dissipated in the collector of each transistor.

7.5 A class B Power amplifier is driving a load at 16 Ω. If the supply voltage $V_{CC} = 25$ V, calculate

(a) maximum ac power output
(b) maximum dc power input
(c) collector dissipation in each transistor.

7.6 A class B power amplifier has a dc supply voltage of $V_{CC} = 30$ V. Calculate the efficiency when the output voltage is

(a) 30 V peak (b) 15 V peak (c) 7.5 V peak

7.7 The following readings are obtained for a Power amplifier during measurement of distortion.

$$V_{CE\min} = 3 \text{ V}, V_{CE\max} = 25 \text{ V}, V_{CEQ} = 15 \text{ V}$$

Calculate the second harmonic distortion.

Chapter 8

OSCILLATORS

Oscillators are an important class of circuits and are used in almost every electronic systems. For example, oscillators are employed to produce sinusoidal signals that are used as carrier in radio and television broadcasts. Oscillators are also used to produce the square wave used as clocks in computers and other synchronous digital systems. This chapter covers the basic principle of operation and design aspects of RC, LC and crystal oscillators.

◆ 8.1 BASIC PRINCIPLE OF OSCILLATORS

An oscillator is a circuit designed to provide periodic output with no input signal. It requires only the DC power. An oscillator is basically an amplifier with positive feedback.

Fig 8.1 shows an amplifier, a feedback network and an inverting network not yet connected to form a closed loop.

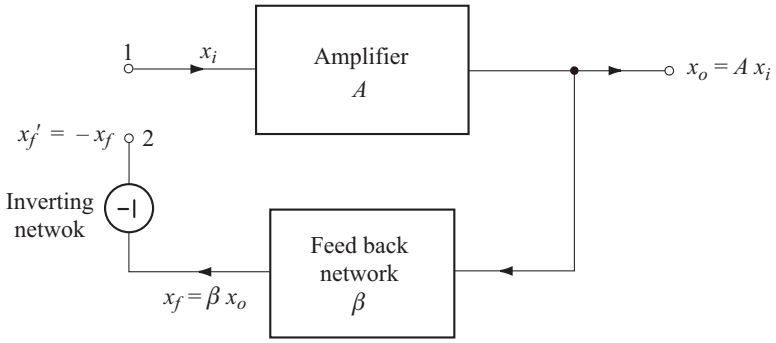


Fig. 8.1 Illustration of basic principle of oscillators

The amplifier provides an output signal x_o in response to the signal x_i applied directly to the amplifier input terminal. The output of the feedback network is $x_f = \beta\, x_o = A\,\beta\, x_i$ and the output of the inverting network is $x_f' = -x_f = -A\,\beta\, x_i$. Now

$$\text{Loop gain} = \frac{x_f'}{x_i} = \frac{-A\,\beta\, x_i}{x_i} = -A\,\beta \tag{8.1}$$

Let, the things be adjusted such that x_f' is identically equal to the externally applied input signal x_i. Now if the external source x_i is removed and terminal 2 is connected to terminal 1, as shown in Fig. 8.2, the amplifier will continue to give the same output as before. We say that the amplifier is producing an output on its own or it is oscillating.

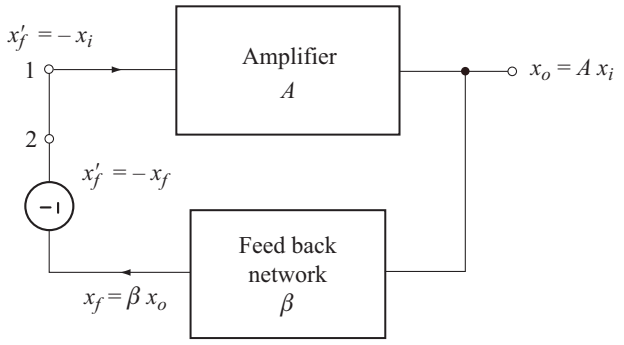


Fig. 8.2 Block diagram of oscillator

$x_f' = x_i$ means that, the instantaneous values of x_f' and x_i are exactly equal at all times. Since x_f' and x_i are in phase, the feedback is positive.

The condition $x_f' = x_i$ is satisfied only by the sine wave since, it preserves its shape when passed through any linear network. Thus the set up shown in Fig. 8.2 produces sinusoidal oscillations.

Substituting $x_f' = x_i$ in Equation (8.1) we have

$$\text{Loop gain} = -A\beta = 1 \tag{8.2}$$

$$-A\beta = 1 + j\,0 \quad \text{[Rectangular form]}$$

or

$$-A\beta = 1\,\underline{|0° \text{ or } 360°} \quad \text{[Polar form]} \tag{8.3}$$

In general

$$-A\beta = |-A\beta|\,\underline{|\theta} \tag{8.4}$$

Comparing Equations (8.3) and (8.4) we get

$$|-A\beta| = |A\beta| = 1 \tag{8.5}$$

and

$$\theta = \underline{|-A\beta} = 0° \text{ or } 360° \tag{8.6}$$

The conditions given in Equations (8.5) and (8.6) are called Barkhansen Criteria for sustained oscillations. These conditions are stated as follows.

- **The frequency at which a sinusoidal oscillator will operate is the frequency for which the phase shift θ of the loop gain is 0° or 360°.**
- **Oscillations will be sustained at the oscillator frequency if the magnitude of loop gain is equal to unity.**

◆ 8.2 PRACTICAL ASPECTS

- In practical oscillators, initially the magnitude of loop gain is set to a value slightly greater than unity. As a result the amplitude of oscillations begins to grow. When the amplitude reaches the desired level, the automic gain control mechanism reduces the gain so as to make the magnitude of loop gain become equal to unity.
- The frequency of oscillation is decided by the elements of the feedback network.
- The function of inverting network is performed by the feedback network itself. i.e., the feedback network introduces a phase shift of 180°.The amplifier produces a phase shift of 180°. As a result the total phase shift becomes 360° satisfying the angle criterion of Barkhausen.

◆ 8.3 CLASSIFICATION OF OSCILLATORS BASED ON THE ELEMENTS USED IN THE FEEDBACK NETWORK

Based on the elements used in the feedback network, oscillators can be classified as follows.

(a) RC oscillators
(b) LC oscillators
(c) Crystal oscillators.

- In RC oscillators, the feedback network uses RC components to generate oscillations. RC oscillators are used to generate oscillations in the audio frequency range. [20 Hz – 20 kHz].
- In LC oscillators, the feedback network employs LC components to generate oscillations. LC oscillators are used to generate oscillations in the radio frequency range [100 kHz – 100 MHz].
- In crystal oscillators, the feedback network uses piezo electric crystal to generate oscillations. Crystal oscillators are used to generate oscillations in the frequency range [10 kHz to 10 MHz].

◆ 8.4 RC-PHASE SHIFT OSCILLATOR

RC-phase shift oscillator is a low frequency oscillator. It is used to generate oscillations in the audio frequency range. The feedback network consists of three identical RC-sections as shown in Fig. 8.3.

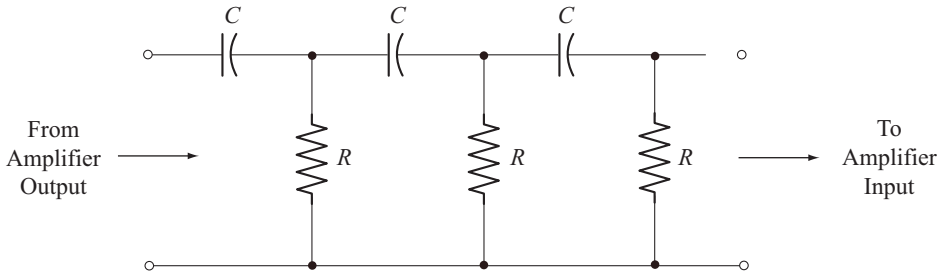


Fig. 8.3 Feedback network in RC-phase shift oscillator

Figure 8.4 (a) shows a single RC-section and its phasor diagram is shown in Fig. 8.4 (b).

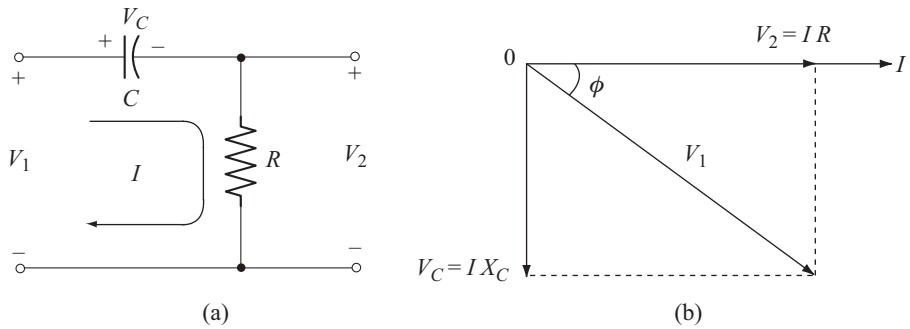


Fig. 8.4 (a) Single RC-section
(b) Phasor diagram

The phasor diagram is drawn taking the current I as the reference vector and using the fact that, in a resistor, the voltage and current are in phase and in a capacitor, the current leads the voltage by an angle 90°. Note that the voltage V_2 leads V_1 by an angle ϕ.

From the phasor diagram

$$\tan \phi = \frac{V_C}{V_2} = \frac{I X_C}{I R} = \frac{X_C}{R}$$

Using

$$X_C = \frac{1}{\omega C} = \frac{1}{2 \pi f_C}$$

$$\tan \phi = \frac{1}{2 \pi f R C} \tag{8.7}$$

The values of R and C are selected so as to give a phase shift of 60° at the desired frequency of oscillations. Since all the three RC-sections are identical, the total phase shift introduced by the feedback network is 180°.

◆ 8.5 TRANSISTOR RC-PHASE SHIFT OSCILLATOR

Figure 8.5 shows the circuit of transistor RC-phase shift oscillator. It consists of a single stage RC-coupled CE amplifier and a feedback network comprising of three identical RC-sections.

The input to the feedback network is the amplifier output voltage V_o and the output of the feedback network is the current I_f'. Note that the circuit employs voltage sampling and current mixing (shunt mixing). Hence the topology is voltage shunt feedback.

If the output voltage of the feedback network were directly connected to the amplifier input, the relatively low input resistance (h_{ie}) of the amplifier appreciably loads down the feedback network. Hence voltage shunt feedback is more suitable.

The resistor R' of the last RC-section is returned to the ground via the input resistance of amplifier stage. Thus the total resistance of the last RC-section is $R' + h_{ie}$. For the three RC-sections to be identical it is essential that

$$R = R' + h_{ie} \tag{8.8}$$

or

$$R' = R - h_{ie} \tag{8.9}$$

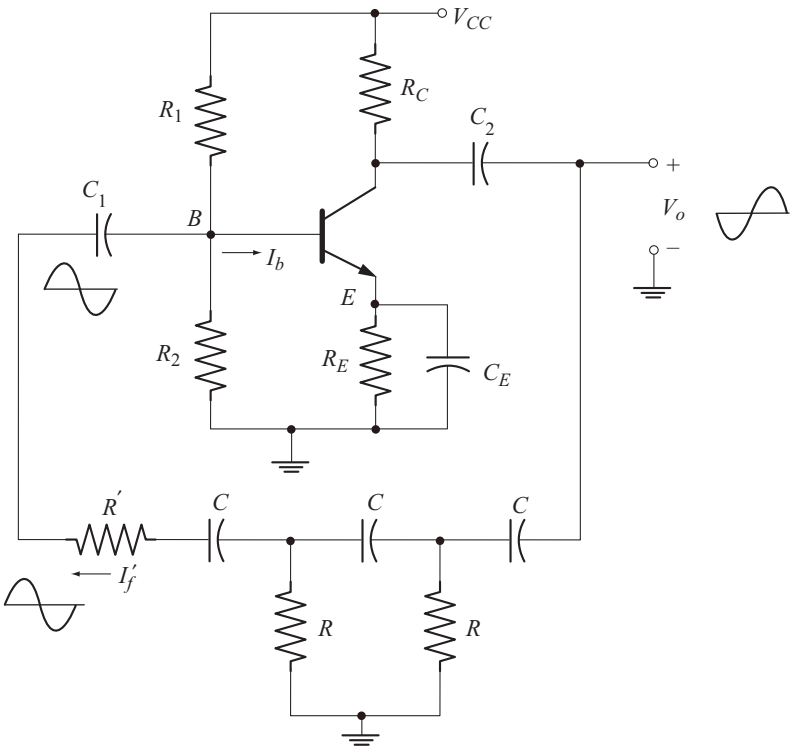


Fig. 8.5 Transistor RC-phase shift oscillator

The values of R and C are selected such that each RC-section gives a phase shift of 60° at the oscillator frequency. The total phase shift from the three RC-sections will be 180°. The CE stage introduces a phase shift of 180°. As a result the total phase shift around the loop is 360°, thus satisfying the angle criteria.

The frequency of oscillations is given by

$$f = \frac{1}{2\pi RC\sqrt{6+4k}} \tag{8.10}$$

where

$$k = \frac{R_C}{R} \tag{8.11}$$

$$\text{Loop gain} = \frac{x_f'}{x_i} = \frac{I_f'}{I_b} \tag{8.12}$$

For the magnitude of loop gain to be greater than unity, the short circuit current gain h_{fe} of the transistor must satisfy the condition

$$h_{fe} > 4k + 23 + \frac{29}{k} \tag{8.13}$$

The minimum value of h_{fe} can be obtained by differentiating h_{fe} with respect to k and equating the result to zero. This yields $h_{fe\,(\min)} = 44.5$ corresponding to $k = 2.7$.

A transistor with a small-signal common-emitter short circuit current gain less than 44.5 cannot be used in the phase-shift oscillator.

8.6 MERITS AND DEMERITS OF RC-PHASE SHIFT OSCILLATOR

The merits of RC-phase shift oscillator are:

- The circuit is simple and easy to design.
- The circuit is less bulky, light weight and less expensive due to the absence of inductor.
- It can be used to generate oscillations in the audio frequency range.
- It generates sinusoidal oscillations.

The demerits are:

- RC network has relatively low quality factor. This results in frequency drift when the circuit parameter values vary due to ageing, temperature, etc.. Hence this circuit has poor frequency stability.
- To generate high frequencies, the required feedback network capacitance becomes too small which will be comparable with the stray capacitances. Hence it has no marked advantage over LC oscillators at high frequencies.
- Variable frequency operation is obtained by changing the three capacitors simultaneously. Such a variation should keep the impedance of the phase shifting network constant and keeps the magnitude of β and $A\beta$ constant in order to have constant amplitude of oscillations at all frequencies. But it is very difficult to meet the above requirement over a wide frequency range.

Example 8.1

In an RC-phase shift oscillator $R = 1\ \text{k}\Omega$ $R_C = 1\ \text{k}\Omega$ and $C = 0.1\ \mu\text{F}$. Calculate the frequency of oscillations.

Solution

$$f = \frac{1}{2\pi RC\sqrt{6+4k}}$$

$$k = \frac{R_C}{R} = \frac{1\ \text{k}\Omega}{1\ \text{k}\Omega} = 1$$

$$f = \frac{1}{2\pi\,(1\ \text{k}\Omega)(0.1\ \mu\text{F})\sqrt{6+4}} = 503.29\ \text{Hz}$$

Example 8.2

In an RC-phase shift oscillator $R_C = 3.3\ \text{k}\Omega$ and $R = 1.5\ \text{k}\Omega$. Calculate the required value of C for a frequency of 2 kHz.

Solution

$$f = \frac{1}{2\pi RC\sqrt{6+4k}}$$

$$\Rightarrow \quad C = \frac{1}{2\pi fR\sqrt{6+4k}}$$

$$k = \frac{R_C}{R} = \frac{3.3\ \text{k}\Omega}{1.5\ \text{k}\Omega} = 2.2$$

$$C = \frac{1}{2\pi(2000)(1.5\ \text{k}\Omega)\sqrt{6+4(2.2)}} = 13.79\ \text{nF}$$

Example 8.3

An RC-phase shift oscillator uses a transistor with $h_{fe} = 100$. If $R_C = 10\ \text{k}\Omega$ and $R = 2\ \text{k}\Omega$. Will this circuit oscillate?

Solution

Condition for sustained oscillations is

$$h_{fe} > 4k + 23 + \frac{29}{k}$$

$$k = \frac{R_C}{R} = \frac{10\ \text{k}\Omega}{2\,\text{k}\Omega} = 5$$

$$h_{fe} > (4)(5) + 23 + \frac{29}{5}$$

$$h_{fe} > 48.8$$

Since the h_{fe} of the transistor is 100 which is greater than 48.8, the circuit oscillates.

Example 8.4

In an RC-phase shift oscillator $R_C = 5\ \text{k}\Omega$ and $R = 3.3\ \text{k}\Omega$. Find the range of values of C if it is required to vary the frequency from 100 Hz to 20 kHz.

Solution

$$f = \frac{1}{2\pi RC\sqrt{6+4k}}$$

$$\Rightarrow \quad C = \frac{1}{2\pi fR\sqrt{6+4k}}$$

$$k = \frac{R_C}{R} = \frac{5\ \text{k}\Omega}{3.3\ \text{k}\Omega} = 1.515$$

$$\sqrt{6+4k} = \sqrt{6 + (4)(1.515)} = 3.472$$

For $f = 100$ Hz

$$C = \frac{1}{2\pi (100)(3.3\ \text{k}\Omega)(3.472)} = 138.9\ \text{nF}$$

For $f = 20$ kHz

$$C = \frac{1}{2\pi (20{,}000)(3.3\,\text{k}\Omega)(3.472)} = 0.6945\ \text{nF}$$

Range of C value: 0.6945 nF to 138.9 nF

Example 8.5

Find the values of R_C, R, R' and C for an RC-phase shift oscillator for a frequency of oscillation of 1000 Hz. A transistor with $h_{fe} = 200$ and $h_{ie} = 2$ kΩ is available.

Solution

Selection of R and R′

$$R = R' + h_{ie}$$
$$R' = R - h_{ie}$$

For R' to be positive,

$$R > h_{ie}$$

i.e., $R > 2\ \text{k}\Omega$

Let $R = 2.7\ \text{k}\Omega$

Now $R' = 2.7\ \text{k}\Omega - 2\ \text{k}\Omega$

$R' = 700\Omega$

Selection of R_C

The condition to get sustained oscillations is

$$h_{fe} > 4k + 23 + \frac{29}{k}$$

$$200 > 4k + 23 + \frac{29}{k}$$

We are free choose the value of k to meet the above requirement.
With $k = 1$, we have

$$200 > 4 + 23 + 29$$
$$200 > 56$$

k =1 satisfies the condition for sustained oscillations.

$$k = \frac{R_C}{R} \qquad R_C = kR = 2.7\ \text{k}\Omega$$

$$C = \frac{1}{2\pi Rf\sqrt{6+4k}} = 18.6\text{nF}$$

Note: R_1, R_2 and R_E can be calculated using the biasing requirement.

Example 8.6

For the transistor RC-phase shift oscillator, derive:

(a) the expression for frequency of oscillations.
(b) the condition required for sustained oscillations.

Solution

(a) ***Expression for frequency of oscillations***

The output equivalent circuit of the phase-shift oscillator of Fig. 8.5 is shown in Fig. A. Note that the resistor R' is returned to ground via the input resistance h_{ie} of the amplifier stage. $\frac{1}{h_{oe}}$ is treated as an open circuit assuming $h_{oe} \approx 0$.

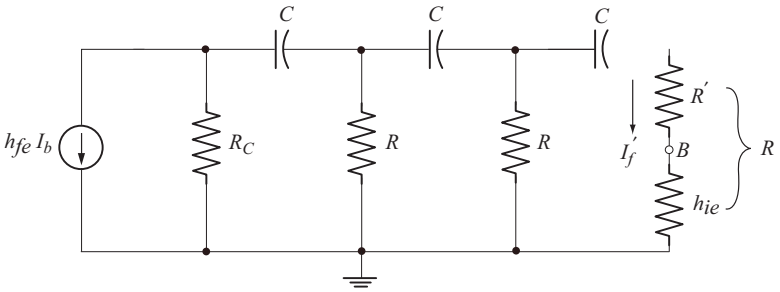


Fig. A

Let us convert the current source into its equivalent voltage source as shown in Fig. B.

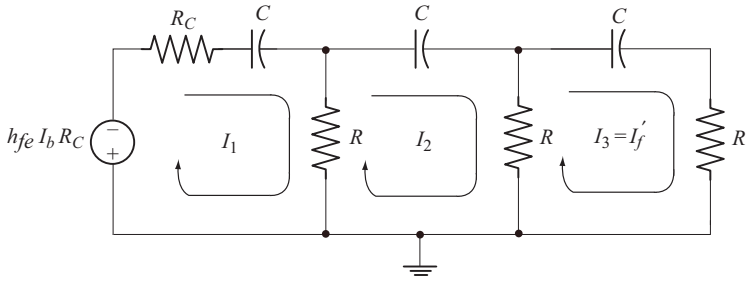


Fig. B

***Loop* 1**

$$-h_{fe} I_b R_C = I_1 [R_C + R - j X_C] - I_2 R \quad \text{(A)}$$

where $X_C = \dfrac{1}{\omega C}$

Dividing through out by R and taking

$$k = \frac{R_C}{R} \quad \text{and} \quad \alpha = \frac{X_C}{R} \quad \text{we have}$$

$$-h_{fe} I_b k = I_1 [k + 1 - j\,\alpha] - I_2 \quad \text{(B)}$$

***Loop* 2**

$$0 = -I_1 R + I_2 [2R - j X_C] - I_3 R$$

or $$0 = -I_1 + I_2 [2 - j\,\alpha] - I_3 \quad \text{(C)}$$

***Loop* 3**

$$0 = -I_2 R + I_3 [2R - j X_C]$$

or $$0 = -I_2 + I_3 [2 - j\,\alpha]$$

$$\Rightarrow \quad I_2 = I_3 [2 - j\,\alpha] \quad \text{(D)}$$

From Equation (C)

$$I_1 = I_2 [2 - j\,\alpha] - I_3$$

Substituting for I_2 from Equation (D) we have

$$I_1 = I_3 [2 - j\,\alpha]^2 - I_3$$

$$I_1 = I_3 [(2 - j\,\alpha)^2 - 1]$$

$$I_1 = I_3 [3 - \alpha^2 - j\,4\,\alpha] \quad \text{(E)}$$

Substituting Equations (D) and (E) in Equation (B) we have

$$-h_{fe} I_b k = I_3 [3 - \alpha^2 - j\,4\,\alpha] [k + 1 - j\,\alpha] - I_3 [2 - j\,\alpha]$$

$$-h_{fe} I_b k = I_3 \{[1 + 3k - (5 + k)\alpha^2] - j [(6 + 4k)\alpha - \alpha^3]\} \quad \text{(F)}$$

$$\text{Loop gain} = \frac{I_f'}{I_b} = \frac{I_3}{I_b}$$

From Equation (F)

$$\frac{I_3}{I_b} = \frac{-h_{fe} k}{\left[1 + 3k - (5 + k)\alpha^2\right] - j\left[(6 + 4k)\alpha - \alpha^3\right]} \quad \text{(G)}$$

For the loop gain to be real

$$(6 + 4k)\,\alpha - \alpha^3 = 0 \quad \text{(H)}$$

$$\alpha^2 = (6 + 4k) \quad \text{(I)}$$

$$\alpha = \sqrt{6+4k} \quad \text{(J)}$$

But $$\alpha = \frac{X_C}{R} = \frac{1}{\omega C R} = \frac{1}{2\pi f R C}$$

Using this relation in Equation (J) we have

$$\frac{1}{2\pi f R C} = \sqrt{6+4k}$$

$$f = \frac{1}{2\pi R C\sqrt{6+4k}} \quad \text{(K)}$$

(b) *Condition for sustained oscillations*

Substituting Equation (H) in Equation (G) we get

or $$\frac{I_3}{I_b} = \frac{-h_{fe}\, k}{1+3k-[5+k]\alpha^2} \quad \text{(L)}$$

$$\text{Dr} = 1 + 3k - [5 + k]\,\alpha^2$$

Using $\alpha^2 = 6 + 4k$ we have

$$\text{Dr} = 1 + 3k - [5 + k]\,[6 + 4k]$$

$$\text{Dr} = -[4k^2 + 23k + 29]$$

Now $$\frac{|I_3|}{|I_b|} = \frac{h_{fe}\, k}{4k^2 + 23k + 29}$$

$$= \frac{h_{fe}}{4k + 23 + \frac{29}{k}} \quad \text{(M)}$$

To get sustained oscillations the magnitude of loop gain should be greater than unity.

i.e., $$\frac{|I_3|}{|I_b|} > 1$$

$$\frac{h_{fe}}{4k + 23 + \frac{29}{k}} > 1$$

or $$h_{fe} > 4k + 23 + \frac{29}{k} \quad \text{(N)}$$

Example 8.7

Show that for oscillations to start in an RC-phase shift oscillator, the minimum h_{fe} value of the transistor should be 44.5.

Solution

The condition required for sustained oscillations is

$$h_{fe} > 4k + 23 + \frac{29}{k} \qquad \text{(A)}$$

h_{fe} is a function of k. Taking the equality condition in Equation (A), differentiating h_{fe} with respect to k and equating the result to zero we have

$$\frac{d\,h_{fe}}{d\,k} = 4 - \frac{29}{k^2} = 0$$

$$k^2 = \frac{29}{4} \quad \text{or} \quad k = 2.7$$

Using this value in Equation (A) we have

$$h_{fe} > 4\,(2.7) + 23 + \frac{29}{2.7}$$

$$h_{fe} > 44.5$$

$$\Rightarrow \quad h_{fe(\min)} = 44.5$$

◆ 8.7 WEIN BRIDGE OSCILLATOR

Wein bridge oscillator is an RC oscillator and is used to generate sinusoidal oscillations in the audio frequency range. Figure 8.6 shows the circuit of wein bridge oscillator.

It consists of an Op-Amp non inverting amplifier in the forward path and a lead-lag network in the feedback path. Series $R_1\,C_1$ network is a lead network and the parallel $R_2\,C_2$ network is the lag network. The name wein bridge is due to the fact that, the feedback resistors R_3 and R_4 of Op-Amp amplifier and the Lead-Lag network forms a bridge as shown in Fig. 8.7.

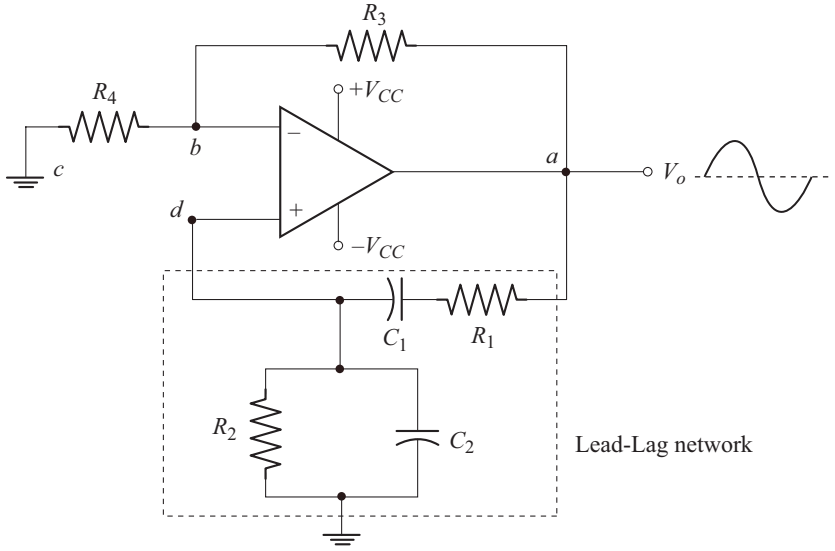


Fig. 8.6 Wein bridge oscillator using Op-Amp amplifier

At the oscillator frequency, the lead-lag network is designed to introduce zero degree phase shift. The Op-Amp non inverting amplifier introduces zero degree phase shift. Hence the total phase shift around the loop is zero.

The expression for the frequency of oscillation is obtained from the balancing condition of the bridge.

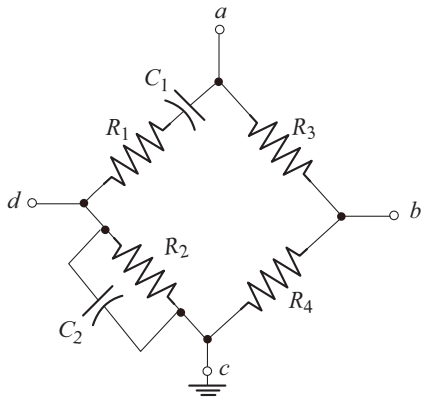


Fig. 8.7 Bridge circuit

The balancing condition is given by

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

and the frequency of oscillation is given by

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{8.14}$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$, then

$$f = \frac{1}{2\pi RC} \tag{8.15}$$

In order to obtain sustained oscillations the gain of the amplifier should be at least equal to 3

$$\therefore \quad 1 + \frac{R_3}{R_4} \geq 3$$

$$\text{or} \quad \frac{R_3}{R_4} \geq 2 \tag{8.16}$$

Example 8.8

The following component values are given for the wein bridge oscillator of the circuit of Fig. 8.6.

$R_1 = R_2 = 33\ \text{k}\Omega$ $\quad C_1 = C_2 = 0.001\ \mu\text{F}$

$R_3 = 47\ \text{k}\Omega$ $\quad R_4 = 15\ \text{k}\Omega$

(a) Will this circuit oscillate?
(b) Calculate the resonant frequency.
(c) Suggest the RC elements to increase the frequency by two fold.

Solution

(a) $$\frac{R_3}{R_4} = \frac{47\,\text{k}\Omega}{15\,\text{k}\Omega} = 3.13 > 2$$

The circuit oscillates since $\frac{R_3}{R_4} > 2$.

(b) $$R_1 = R_2 = R = 33\ \text{k}\Omega \qquad C_1 = C_2 = C = 0.001\ \mu\text{F}$$

$$f = \frac{1}{2\pi RC}$$

$$= \frac{1}{2\pi\,(33\ \text{k}\Omega)\,(0.001\ \mu\text{F})} = 4.82\ \text{kHz}$$

$$f = 2\,(4.82\ \text{kHz}) = 9.64\ \text{kHz}$$

$$f = \frac{1}{2\pi RC} \quad \Rightarrow \quad RC = \frac{1}{2\pi f}$$

Let us not change C

$$\therefore \qquad C = 0.001\ \mu\text{F}$$

Now $$R = \frac{1}{2\pi f C} = \frac{1}{2\pi\,(9.64\ \text{kHz})\,(0.001\ \mu\text{F})} = 16.5\ \text{k}\Omega$$

Example 8.9

Design the component values of wein bridge oscillator of Fig. 8.6 for a frequency of oscillations of 4 kHz.

Solution

Let $$R_1 = R_2 = R \quad \text{and} \quad C_1 = C_2 = C$$

$$f = \frac{1}{2\pi RC}$$

Select $$C = 0.01\ \mu\text{F}$$

$$R = \frac{1}{2\pi f C} = \frac{1}{2\pi(4\ \text{kHz})(0.01\ \mu\text{F})} = 3.97\ \text{k}\Omega$$

For sustained oscillations

$$\frac{R_3}{R_4} \geq 2$$

$$R_3 \geq 2R_4$$

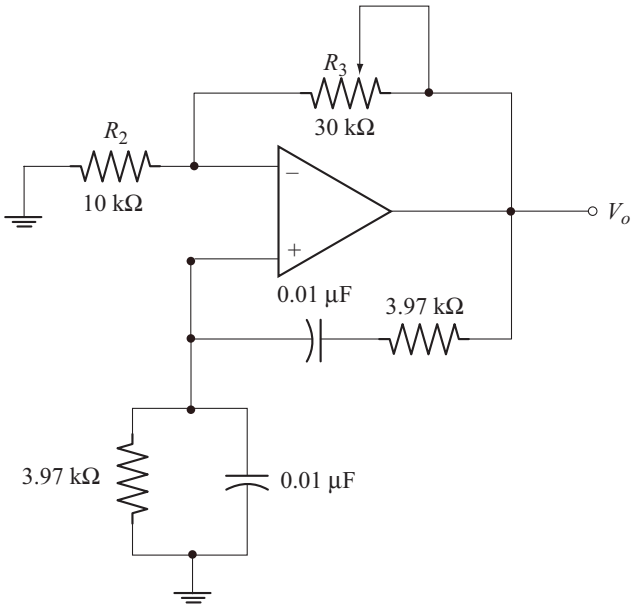
Let $R_4 = 10\ \text{k}\Omega$

then $R_3 \geq 20\ \text{k}\Omega$

Select $R_3 = 30\ \text{k}\Omega$

A 30 kΩ potentiometer can be used for R_3. R_3 is adjusted until undistorted sustained oscillations are obtained.

The circuit diagram is shown below.



Example 8.10

For the wein bridge oscillator of Fig. 8.6 derive the expressions for

(a) Frequency of oscillations

(b) Condition for sustained oscillations

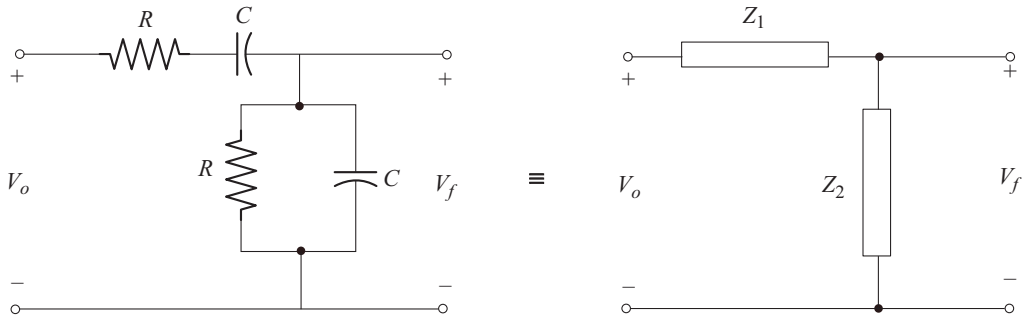
Solution

(a) ***Expression for Frequency of Oscillation***

The feedback network of wein bridge oscillator is shown below. We have taken $R_1 = R_2 = R$ and $C_1 = C_2 = C$.

Let $$Z_1 = R + \frac{1}{j\omega C}$$

$$Z_1 = \frac{1 + j\omega RC}{j\omega C} \qquad \text{(A)}$$



and $$Z_2 = R \parallel \frac{1}{j\omega C}$$

$$= \frac{(R)\left(\frac{1}{j\omega C}\right)}{R + \frac{1}{j\omega C}}$$

$$Z_2 = \frac{R}{1 + j\omega RC} \qquad \text{(B)}$$

Using voltage division rule we have

$$V_f = \frac{V_o\, Z_2}{Z_1 + Z_2}$$

Feedback factor is

$$\beta = \frac{V_f}{V_o} = \frac{Z_2}{Z_1 + Z_2}$$

$$\beta = \frac{\left[\frac{R}{1 + j\omega RC}\right]}{\left[\frac{1 + j\omega RC}{j\omega C}\right] + \left[\frac{R}{1 + j\omega RC}\right]}$$

$$= \frac{j\omega RC}{\left[1 + j\omega RC\right]^2 + j\omega RC}$$

$$= \frac{j\omega RC}{\left[1 - \omega^2 R^2 C^2\right] + j3\omega RC}$$

$$= \frac{j\omega RC}{j\left\{3\omega RC - j\left[1 - \omega^2 R^2 C^2\right]\right\}}$$

$$\beta = \frac{V_f}{V_o} = \frac{\omega RC}{3\omega RC + j\left[\omega^2 R^2 C^2 - 1\right]} \quad \text{(C)}$$

For zero phase shift between V_f and V_o, the required condition is

$$\omega^2 R^2 C^2 - 1 = 0 \quad \text{(D)}$$

or $\omega^2 R^2 C^2 = 1$

$\Rightarrow$ $\omega RC = 1$

$$\omega = \frac{1}{RC}$$

or $$f = \frac{1}{2\pi RC} \quad \text{(E)}$$

(b) *Condition for Sustained Oscillations*

Substituting equation (D) in equation (C) we get

$$\beta = \frac{1}{3} \quad \text{(F)}$$

For the oscillations to start the magnitude of loop gain must be at least equal to unity.

i.e., $|A\beta| \geq 1$

$$|A| \geq \frac{1}{\beta}$$

or $|A| \geq 3$ (G)

But for the Op-Amp non-inverting amplifier

$$|A| = A = 1 + \frac{R_3}{R_4}$$

Using this relation in equation (G) we have

$$1 + \frac{R_3}{R_4} \geq 3$$

or $$\frac{R_3}{R_4} \geq 2 \quad \text{(H)}$$

Example 8.11

List the similarities and differences between RC-phase shift and wein bridge oscillators.

Solution

The similarities and differences between the RC-phase shift and wein bridge oscillators are given in the following table.

S. No.	RC phase shift oscillator	Wein bridge oscillator
1.	This is an RC oscillator used to generate sinusoidal oscillations in the audio frequency range.	This is also an RC oscillator used to generate sinusoidal oscillations in the audio frequency range.
2.	The feedback network contains three identical RC sections.	The feedback network contains lead-lag network.
3.	Each RC section is designed to introduce 60° phases shift at the oscillator frequency. The total phase shift in the feedback network is 180°.	The feedback network introduces zero degree phase shift at the oscillator frequency.
4.	This circuit uses inverting amplifier which introduces a phase shift of 180°.	This circuit uses non-inverting amplifier with no phase shift.
5.	The frequency of oscillation is $f = \frac{1}{2\pi RC\sqrt{6+4k}}$	The frequency of oscillation is $f = \frac{1}{2\pi RC}$
6.	Condition for sustained oscillations is $h_{fe} > 4\,k + 23 + 29/k$	Condition for sustained oscillations is $A \geq 3$
7.	Variable frequency operation is obtained by varying all the three capacitors of the feedback network simultaneously	Variable frequency operation is obtained by varying both the feedback network capacitors simultaneously

◆ 8.8 LC OSCILLATORS (TUNED OSCILLATORS)

LC oscillators employ parallel LC circuit to generate sinusoidal oscillations. Parallel LC circuit is also called tuned circuit or resonant circuit. The frequency of oscillations is determined from the resonant condition of the tuned circuit. These oscillators exhibit high Q than RC oscillators resulting in good frequency stability. They use relatively small reactive elements in the tank circuit. They are used to generate oscillations in the frequency range from 100 kHz to hundreds of megahertz.

Figure 8.8 shows the basic configuration of LC oscillators. Based on the nature of the reactive elements X_1, X_2 and X_3 two types of LC oscillators are obtained as indicated in Table 8.1. The amplifier can be an FET amplifier, BJT amplifier or an Op-Amp amplifier.

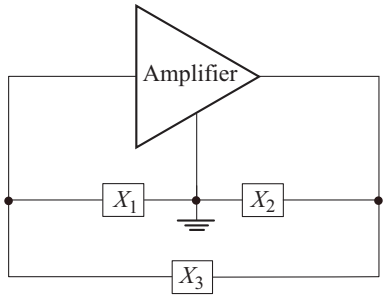


Fig. 8.8 Basic configuration of LC oscillators

Table 8.1

Oscillator type	Reactive element		
	X_1	X_2	X_3
Colpitts oscillator	C	C	L
Hartley oscillator	L	L	C

8.9 TRANSISTOR COLPITTS OSCILLATOR

Figure 8.9 shows the transistor colpitts oscillator. It consists of a CE amplifier which introduces a phase shift of 180°. Resistors R_1, R_2 and R_E are used to establish the desired operating point

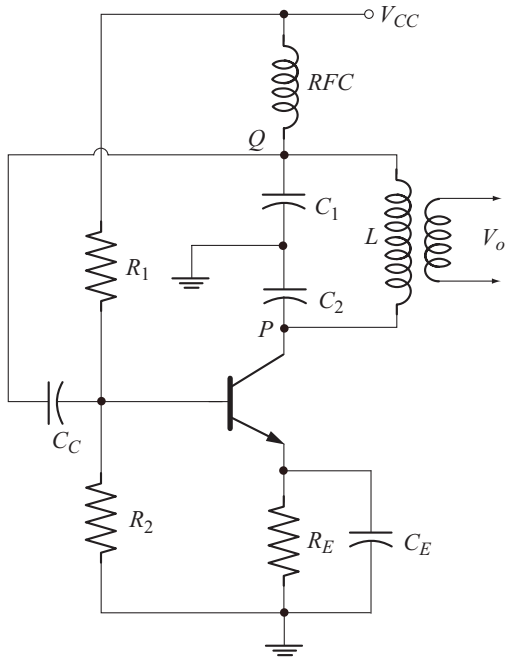


Fig. 8.9 Transistor colpitts oscillator

The feedback network consists of a tapped capacitive voltage divider C_1 and C_2 in parallel with the inductor L. The voltage across C_1 is fed back to the amplifier input through the coupling capacitor C_C.

RF choke is a large inductor. Its function is two fold:

- It acts as a dc short to the power supply V_{CC} i.e., it allows the dc current to easily pass through.
- It acts as an open circuit for ac. This ensures that the top end of the tank circuit is not connected to the ac ground.

Due to split capacitor arrangement, the tank circuit introduces 180° phase shift. As a result the oscillations at points *P* and *Q* are 180° out of phase. The total phase shift around the loop is 360° since the transistor amplifier introduces an additional phase shift of 180°.

The output is coupled to the load through a transformer. Transformer coupling has the following advantages:

- It provides electrical isolation between the oscillator output and load.
- It provides impedance matching between the oscillator output and the load.

The frequency of oscillations is given by

$$f = \frac{1}{2\pi\sqrt{L C_{eq}}} \tag{8.17}$$

where $$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{8.18}$$

The condition for sustained oscillations is

$$h_{fe} \geq \frac{C_2}{C_1} \tag{8.19}$$

Example 8.12

The following data are available for the colpitts oscillator of Fig 8.9.

$C_1 = 1$ nF $\quad C_2 = 99$ nF $\quad L = 1.5$ mH

$L_{RFC} = 0.5$ mH $\quad C_C = 10$ μF $\quad h_{fe} = 110$

(a) Calculate the frequency of oscillation

(b) Check to make sure that the condition for oscillation is satisfied.

Solution

At the oscillator frequency L_{RFC} acts as an open circuit and C_C acts as short circuit. Hence they do not appear in any of the calculations.

(a)
$$f = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{(1\text{ nF})(99\text{ nF})}{1\text{ nF} + 99\text{ nF}} = 0.99\text{ nF}$$

$$f = \frac{1}{2\pi\sqrt{(1.5\text{ mH})(0.99\text{ nF})}} = 130.6\text{ kHz}$$

(b) Condition for sustained oscillation is

$$h_{fe} \geq \frac{C_2}{C_1}$$

$$h_{fe} = 110$$

$$\frac{C_2}{C_1} = \frac{99 \text{ nF}}{1 \text{ nF}} = 99$$

Note that $h_{fe} > \frac{C_2}{C_1}$

The condition for oscillation is satisfied.

Example 8.13

In a transistor colpitts oscillator $C_1 = 1$ nF and $C_2 = 100$ nF. Find the value of L for a frequency of 100 kHz.

Solution

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\Rightarrow \quad L = \frac{1}{\left[2\pi f\right]^2 C_{eq}}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{(1 \text{ nF})(100 \text{ nF})}{1 \text{ nF} + 100 \text{ nF}} = 0.99 \text{ nF}$$

$$L = \frac{1}{\left[2\pi \times 100 \text{ kHz}\right]^2 \left[0.99 \text{ nF}\right]} = 2.55 \text{ mH}$$

Example 8.14

In a transistor colpitts oscillator $L = 1$ mH, $h_{fe} = 150$. Find the values of C_1 and C_2 required for a frequency of oscillation of 120 kHz.

Solution

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\Rightarrow \quad C_{eq} = \frac{1}{\left[2\pi f\right]^2 L} = \frac{1}{\left[2\pi \times 120 \text{ kHz}\right]^2 \left[1 \text{ mH}\right]} = 1.75 \text{ nF}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \qquad \text{(A)}$$

The condition for sustained oscillation is

$$h_{fe} \geq \frac{C_2}{C_1}$$

$$150 \geq \frac{C_2}{C_1}$$

or $\quad C_2 \leq 150\, C_1$

Let $C_2 = 100\ C_1$ (B)

Using this relation in Equation (A) we have

$$C_{eq} = \frac{100\ C_1^2}{101\ C_1}$$

$$\Rightarrow \quad C_1 = \frac{101}{100}\ C_{eq} = \left(\frac{101}{100}\right)(1.75\ \text{nF})$$

$$C_1 = 1.7675\ \text{nF}$$

From Equation (B)

$$C_2 = (100)\ (1.7675)$$

$$C_2 = 176.75\ \text{nF}$$

Example 8.15

A colpitts oscillator uses a transistor with $h_{fe} = 120$. Find the values of C_1, C_2 and L for a frequency of oscillation of 150 kHz.

Solution

Selection of C_1 and C_2

The smaller capacitor C_1 should be larger than the transistor parasitic capacitances and the stray wiring capacitances.

The parasitic and stray capacitances are in the order of few tens of pico Farad.

Let $C_1 = 1000\ \text{pF} = 1\ \text{nF}$

$$h_{fe} \geq \frac{C_2}{C_1}$$

$$C_2 \leq h_{fe}\ C_1$$

$$C_2 \leq 120\ C_1$$

Let $C_2 = 100\ C_1$

$$C_2 = (100)\ (1\ \text{nF}) = 100\ \text{nF}$$

Calculation of L

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\Rightarrow \quad L = \frac{1}{\left[2\pi f\right]^2 C_{eq}}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{(1\ \text{nF})(100\ \text{nF})}{101\ \text{nF}} = 0.99\ \text{nF}$$

Now $$L = \frac{1}{\left[2\pi \times 150 \times 10^3\right]^2 \left[0.99 \times 10^{-9}\right]} = 1.137\ \text{mH}$$

Example 8.16

For the transistor colpitts oscillator derive the expressions for

(a) Frequency of oscillations
(b) Condition for sustained oscillations

Solution

The small signal ac equivalent circuit on the output side of the colpitts oscillator of Fig. 8.9 is shown in Fig. A. The description for the construction of the equivalent circuit is given below.

- Inductor L appears between points P (collector) and Q.
- Point Q is returned to ground via the input resistance h_{ie} of the CE stage.
- $\frac{1}{h_{oe}}$ is treated as an open circuit assuming $h_{oe} \approx 0$.

RFC acts as an open circuit and C_C as short at the oscillator frequency.

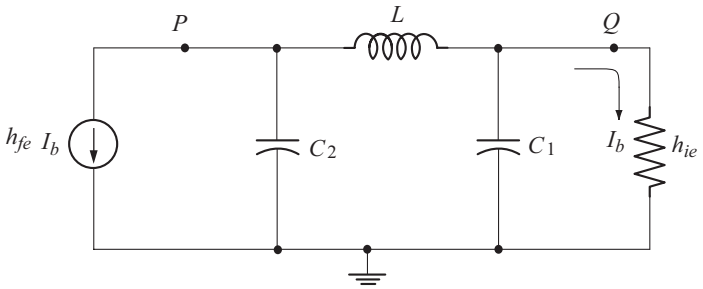


Fig. A

Let us convert the current source in parallel with C_2 into its equivalent voltage source. The resulting circuit is shown in Fig. B.

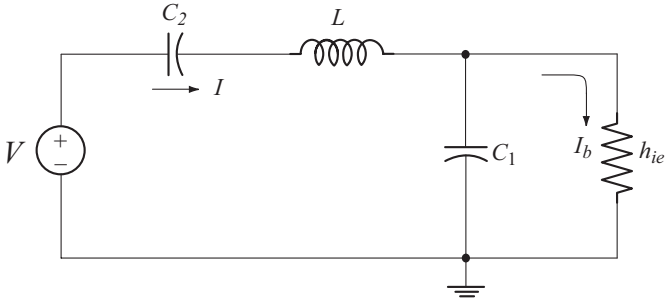


Fig. B

$$V = -h_{fe} I_b \left[\frac{1}{j\omega C_2}\right] \tag{A}$$

The negative sign is due to the fact that, current driven by the voltage source is upward but the actual direction of current in the current source is downward.

Using current division rule in the circuit of Fig. B, we have

$$I_b = \frac{I\left[\frac{1}{j\omega C_1}\right]}{\frac{1}{j\omega C_1} + h_{ie}}$$

$$I_b = \frac{I}{1 + j\omega C_1 h_{ie}} \quad \text{(B)}$$

Let $$Z = \frac{1}{j\omega C_1} \parallel h_{ie}$$

$$= \frac{\left[\frac{1}{j\omega C_1}\right] h_{ie}}{\frac{1}{j\omega C_1} + h_{ie}}$$

$$Z = \frac{h_{ie}}{1 + j\omega C_1 h_{ie}} \quad \text{(C)}$$

The simplified circuit is shown in Fig. C.

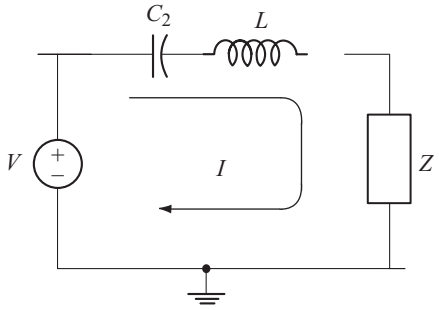


Fig. C

$$I = \frac{V}{\frac{1}{j\omega C_2} + j\omega L + Z} = \frac{V}{\frac{1 - \omega^2 LC_2}{j\omega C_2} + Z}$$

Substituting for V and Z we have

$$I = \frac{-h_{fe} I_b \left[\frac{1}{j\omega C_2}\right]}{\frac{1 - \omega^2 LC_2}{j\omega C_2} + \frac{h_{ie}}{1 + j\omega C_1 h_{ie}}}$$

$$I = \frac{-h_{fe} I_b \left[1 + j\omega C_1 h_{ie}\right]}{\left[1-\omega^2 L C_2\right]\left[1 + j\omega C_1 h_{ie}\right] + j\omega C_2 h_{ie}} \tag{D}$$

$$\begin{aligned} \text{Dr} &= 1 - \omega^2 L C_2 + j\omega C_1 h_{ie} - j\omega^3 L C_1 C_2 h_{ie} + j\omega C_2 h_{ie} \\ &= [1 - \omega^2 L C_2] + j h_{ie} [\omega C_1 + \omega C_2 - \omega^3 L C_1 C_2] \end{aligned}$$

Now, $$I = \frac{-h_{fe} I_b \left[1 + j\omega C_1 h_{ie}\right]}{\left[1-\omega^2 L C_2\right] + j h_{ie}\left[\omega C_1 + \omega C_2 - \omega^3 L C_1 C_2\right]} \tag{E}$$

Substituting this relation in equation (B) we have

$$I_b = \left[\frac{1}{1 + j\omega C_1 h_{ie}}\right]\left[\frac{-h_{fe} I_b \left[1 + j\omega C_1 h_{ie}\right]}{\left[1-\omega^2 L C_2\right] + j h_{ie}\left[\omega C_1 + \omega C_2 - \omega^3 L C_1 C_2\right]}\right]$$

$$1 = \frac{h_{fe}}{[\omega^2 L C_2 - 1] - j h_{ie}[\omega C_1 + \omega C_2 - \omega^3 L C_1 C_2]} \tag{F}$$

Since LHS is real, the right hand side should also be real. This requires that

$$h_{ie}[\omega C_1 + \omega C_2 - \omega^3 L C_1 C_2] = 0 \tag{G}$$

Since $h_{ie} \neq 0$, we have

$$\begin{aligned} \omega C_1 + \omega C_2 - \omega^3 L C_1 C_2 &= 0 \\ \omega [C_1 + C_2] &= \omega^3 L C_1 C_2 \\ 1 &= \omega^2 L \frac{C_1 C_2}{C_1 + C_2} \end{aligned} \tag{H}$$

$$\text{Let} \qquad C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{I}$$

Using this relation in equation (H) we have

$$1 = \omega^2 L C_{eq}$$

$$\text{or} \qquad \omega = \frac{1}{\sqrt{L C_{eq}}} \tag{J}$$

$$\text{or} \qquad f = \frac{1}{2\pi\sqrt{L C_{eq}}} \tag{K}$$

Using Equation (G) in Equation (F) we have

$$1 = \frac{h_{fe}}{\omega^2 L C_2 - 1}$$

$$h_{fe} = \omega^2 L C_2 - 1 \tag{L}$$

From Equation (H)

$$\omega^2 L\, C_2 = \frac{C_1 + C_2}{C_1} = 1 + \frac{C_2}{C_1}$$

$$\therefore \quad \omega^2 L\, C_2 - 1 = \frac{C_2}{C_1}$$

Now Equation (L) becomes

$$h_{fe} = \frac{C_2}{C_1}$$

In practical oscillators, to ensure sustained oscillations the ratio $\frac{C_2}{C_1}$ is kept smaller than h_{fe}

$$\therefore \quad h_{fe} \geq \frac{C_2}{C_1} \qquad \text{(M)}$$

8.10 TRANSISTOR HARTLEY OSCILLATOR

Figure. 8.10 shows the transistor Hartley oscillator. It consists of a CE amplifier which introduces a phase shift of 180°. Resistors R_1, R_2 and R_E are used to establish the desired operating point.

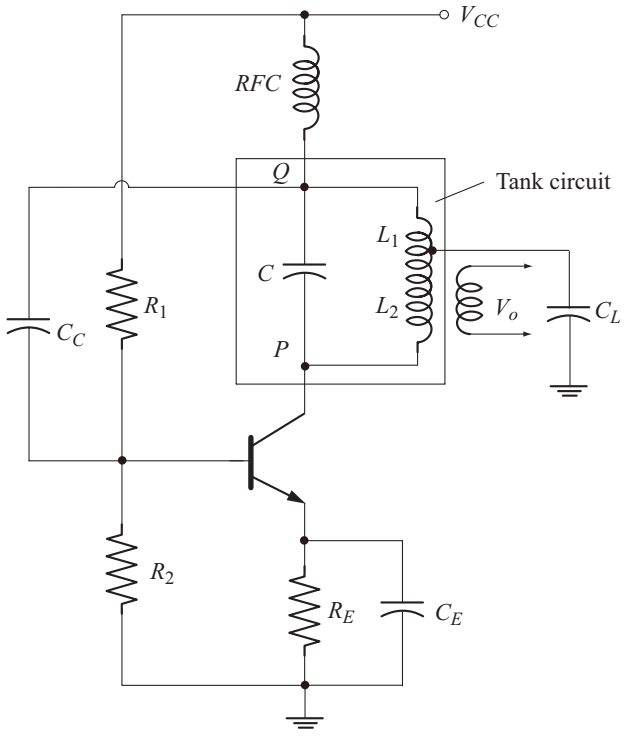


Fig. 8.10 Transistor Hartley oscillator

The feedback network consists of a tapped inductive voltage divider L_1 and L_2 in parallel with the capacitor C. The voltage across L_1 is fed back to the amplifier input through the coupling capacitor C_C.

RF choke is a large inductor. It serves two functions.

- It acts as a dc short to the power supply V_{CC} i.e., it allows the dc current to easily pass through.
- It acts as an open circuit for ac. This ensures that the top end of the tank circuit is not connected to the ac ground.

The capacitor C_L creates ac ground at the junction of L_1 and L_2.

Due to split inductor arrangement, the tank circuit introduces 180° phase shift. As a result the oscillations at points *P* and *Q* are 180° out of phase. The total phase shift around the loop is 360°, since the transistor amplifier introduces an additional phase shift of 180°.

The output is coupled to the load through a transformer. Transformer coupling has the following advantages:

- It provides electrical isolation between the oscillator output and the load.
- It provides impedance matching between the oscillator output and the load.

The frequency of oscillations is given by

$$f = \frac{1}{2\pi\sqrt{L_{eq}\,C}} \tag{8.20}$$

where $$L_{eq} = L_1 + L_2 + 2M \tag{8.21}$$

M is the mutual inductance between L_1 and L_2.

The condition for sustained oscillation is

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M} \tag{8.22}$$

Neglecting the mutual inductance, the condition for sustained oscillations is given by

$$h_{fe} \geq \frac{L_1}{L_2} \tag{8.23}$$

Example 8.17

The following circuit parameter values are given for the Hartley oscillator of Fig. 8.10.

$L_1 = 750\ \mu H$ $L_2 = 750\ \mu H$ $M = 150\ \mu H$

$L_{RFC} = 0.5\ mH$ $C = 150\ pF$ $C_L = 10\ \mu F$ $h_{fe} = 50$

(a) Calculate the frequency of oscillations.

(b) Check to make sure that the condition for oscillation is satisfied.

Solution

(a) $$f = \frac{1}{2\pi\sqrt{L_{eq}\,C}}$$

$$L_{eq} = L_1 + L_2 + 2M$$
$$= 750\ \mu H + 750\ \mu H + (2)(150\ \mu H) = 1800\ \mu H$$
$$f = \frac{1}{2\pi\sqrt{(1800\ \mu H)(150\ pF)}} = 306.29\ kHz.$$

(b) Condition for sustained oscillation taking mutual inductance into account is

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M}$$
$$h_{fe} = 50$$
$$\frac{L_1 + M}{L_2 + M} = \frac{750\ \mu H + 150\ \mu H}{750\ \mu H + 150\ \mu H} = 1$$

Note that $h_{fe} > \frac{L_1 + M}{L_2 + M}$

$\therefore$ The condition for oscillation is satisfied.

Example 8.18

In a transistor Hartley oscillator, $L_1 = 10\ \mu H$ $L_2 = 10\ \mu F$. Find the value of C required for an oscillating frequency of 150 kHz.

Solution

$$f = \frac{1}{2\pi\sqrt{L_{eq} C}}$$
$$\Rightarrow \quad C = \frac{1}{[2\pi f]^2 L_{eq}}$$
$$L_{eq} = L_1 + L_2 + 2M$$

Since M is not given we can take $M = 0$

$$L_{eq} = 10\ \mu H + 10\ \mu H = 20\ \mu H$$
$$C = \frac{1}{\left[2\pi \times 150 \times 10^3\right]^2 [20\ \mu H]} = 56.28\ nF$$

Example 8.19

In a transistor Hartley oscillator $C = 0.01\ \mu F$ and $h_{fe} = 50$. Find the values of L_1 and L_2 required for a frequency of oscillation of 150 kHz.

Solution

$$f = \frac{1}{2\pi\sqrt{L_{eq} C}}$$

$$L_{eq} = \frac{1}{\left[2\pi f\right]^2 C}$$

$$= \frac{1}{\left[2\pi \times 150 \times 10^3\right]^2 \left[0.01 \times 10^{-6}\right]} = 112.5\ \mu\text{H}$$

Neglecting mutual inductance

$$L_{eq} = L_1 + L_2$$

$$\therefore \quad L_1 + L_2 = 112.5\ \mu\text{H} \qquad \text{(A)}$$

Condition for oscillation to start is

$$h_{fe} \geq \frac{L_1}{L_2}$$

$$50 \geq \frac{L_1}{L_2}$$

$$\frac{L_1}{L_2} \leq 50$$

Let $$\frac{L_1}{L_2} = 10$$

$$\Rightarrow \quad L_1 = 10\, L_2 \qquad \text{(B)}$$

Using this relation in Equation (A) we have

$$11\, L_2 = 112.5\ \mu\text{H}$$

$$L_2 = 10.23\ \mu\text{H}$$

From Equation (B)

$$L_1 = 102.3\ \mu\text{H}$$

Example 8.20

A Hartley oscillator uses a transistor with $h_{fe} = 40$. Find the values of L_1, L_2 and C for a frequency of oscillations of 100 kHz.

Solution

Selection of C

Select C Larger than parasitic and stray capacitances

Let $$C = 10\ \text{nF} = 0.01\ \mu\text{F}$$

Calculation of L_1 and L_2

$$L_{eq} = \frac{1}{\left[2\pi f\right]^2 C}$$

$$= \frac{1}{\left[2\pi \times 100 \times 10^3\right]^2 \left[0.01 \times 10^{-6}\right]} = 253.3\ \mu H$$

Neglecting mutual inductance

$$L_{eq} = L_1 + L_2$$

$$\therefore \quad L_1 + L_2 = 253.3\ \mu H \qquad \text{(A)}$$

Condition for sustained oscillations is

$$h_{fe} \geq \frac{L_1}{L_2}$$

$$40 \geq \frac{L_1}{L_2}$$

or $$\frac{L_1}{L_2} \leq 40$$

Let $$\frac{L_1}{L_2} = 10$$

$$\Rightarrow \quad L_1 = 10\, L_2 \qquad \text{(B)}$$

Using this relation in Equation (A) we have

$$11\, L_2 = 253.3\ \mu H$$

$$L_2 = 23.02\ \mu H$$

From equation (B)

$$L_1 = 10\, L_2 = (10)\ (23.02\ \mu H)$$

$$L_1 = 230.2\ \mu H$$

Example 8.21

For the transistor Hartley oscillator derive the expressions for

(a) Frequency of oscillation
(b) Condition for sustained oscillation

Solution

The small signal ac equivalent circuit on the output side of the Hartley oscillator of Fig. 8.10 is shown in Fig. A.

The description for the construction of equivalent circuit is given below:

- Capacitor C appears between points P (collector) and Q.
- Point Q is returned to the ground via the input resistance h_{ie} of the CE stage.
- $\frac{1}{h_{oe}}$ is treated as an open circuit and C_L as short circuit at the oscillator frequency .
- Mutual Inductance between L_1 and L_2 is neglected.

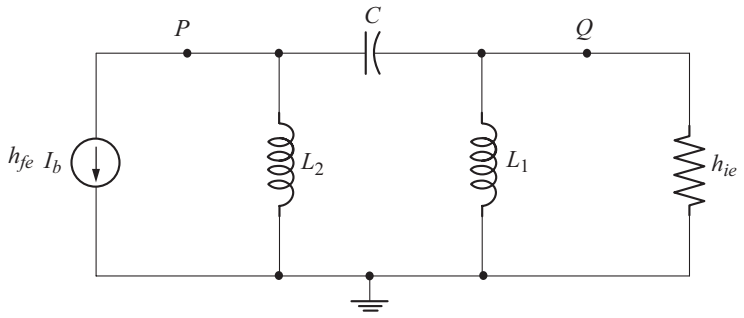


Fig. A

Let us convert the current source in parallel with L_2 into its equivalent voltage source as shown in Fig. B.

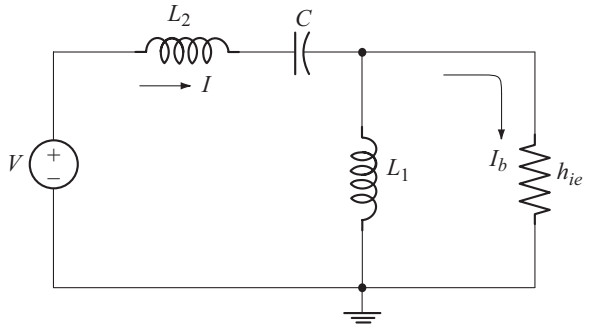


Fig. B

$$V = -h_{fe} I_b \ [j \omega L_2] \tag{A}$$

The negative sign is due to the fact that, current driven by the voltage source is upward but the actual direction of current in the current source is downward.

Using current division rule in the circuit of Fig. B, we get

$$I_b = \frac{I\left[j\omega L_1\right]}{h_{ie} + j\omega L_1} \tag{B}$$

Let $Z = j\omega L_1 \parallel h_{ie}$

$$Z = \frac{\left[j\omega L_1\right] h_{ie}}{h_{ie} + j\omega L_1} \tag{C}$$

The simplified circuit is shown in Fig. C.

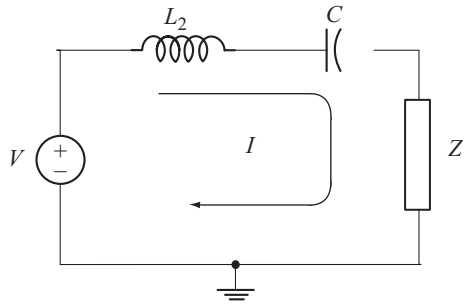


Fig. C

$$I = \frac{V}{j\omega L_2 + \frac{1}{j\omega C} + Z} = \frac{V}{\frac{1-\omega^2 L_2 C}{j\omega C} + Z}$$

Substituting for V and Z we have

$$I = \frac{-h_{fe} I_b \left[j\omega L_2 \right]}{\frac{1-\omega^2 L_2 C}{j\omega C} + \frac{j\omega L_1 h_{ie}}{h_{ie} + j\omega L_1}}$$

$$I = \frac{\left[-h_{fe} I_b\right]\left[j\omega L_2\right]\left[h_{ie} + j\omega L_1\right]\left[j\omega C\right]}{\left[1-\omega^2 L_2 C\right]\left[h_{ie} + j\omega L_1\right] + \left[j\omega L_1 h_{ie}\right]\left[j\omega C\right]} \quad \text{(D)}$$

$$\text{Dr} = \left[1 - \omega^2 L_2 C\right] h_{ie} + j\omega L_1 \left[1 - \omega^2 L_2 C\right] - \omega^2 L_1 C h_{ie}$$

$$= h_{ie}\left[1 - \omega^2 L_2 C - \omega^2 L_1 C\right] + j\omega L_1 \left[1 - \omega^2 L_2 C\right] \quad \text{(E)}$$

Substituting this relation in Equation (D) we get

$$I = \frac{\left[h_{fe} I_b\right]\left[\omega^2 L_2 C\right]\left[h_{ie} + j\omega L_1\right]}{h_{ie}\left[1-\omega^2 L_2 C - \omega^2 L_1 C\right] + j\omega L_1 \left[1-\omega^2 L_2 C\right]}$$

Substituting this relation in equation (B) we have

$$I_b = \left[\frac{j\omega L_1}{h_{ie} + j\omega L_1}\right]\left\{\frac{\left[h_{fe} I_b\right]\left[\omega^2 L_2 C\right]\left[h_{ie} + j\omega L_1\right]}{h_{ie}\left[1-\omega^2 L_2 C - \omega^2 L_1 C\right] + j\omega L_1 \left[1-\omega^2 L_2 C\right]}\right\}$$

$$1 = \frac{j h_{fe} \omega^3 L_1 L_2 C}{h_{ie}\left[1-\omega^2 L_2 C - \omega^2 L_1 C\right] + j\omega L_1 \left[1-\omega^2 L_2 C\right]}$$

Eliminating j from the numerator we have

$$1 = \frac{h_{fe}\,\omega^3 L_1 L_2 C}{-j\,h_{ie}\left[1-\omega^2 L_2 C-\omega^2 L_1 C\right]+\omega L_1\left[1-\omega^2 L_2 C\right]} \tag{F}$$

Since the LHS is real, the RHS should also be real.
This requires that

$$h_{ie}\,[\,1-\omega^2 L_2 C - \omega^2 L_1 C\,] = 0 \tag{G}$$

Since $h_{ie} \neq 0$, we have

$$1-\omega^2 L_2 C-\omega^2 L_1 C = 0$$

$$\omega^2 C\,[\,L_1 + L_2\,] = 1 \tag{H}$$

$$\text{Let} \qquad L_{eq} = L_1 + L_2 \tag{I}$$

$$\text{Now} \qquad \omega^2 C L_{eq} = 1$$

$$\text{or} \qquad \omega = \frac{1}{\sqrt{L_{eq} C}}$$

$$\text{or} \qquad f = \frac{1}{2\pi\sqrt{L_{eq} C}} \tag{J}$$

Condition for sustained oscillations

Substituting Equation (G) in Equation (F) we get

$$\text{or} \qquad 1 = \frac{h_{fe}\,\omega^3 L_1 L_2 C}{\omega L_1\left[1-\omega^2 L_2 C\right]} \tag{K}$$

From Equation (H)

$$\omega^2 L_1 C + \omega^2 L_2 C = 1$$

$$\Rightarrow \qquad 1 - \omega^2 L_2 C = \omega^2 L_1 C$$

Using this relation in Equation (K) we get

$$\text{or} \qquad h_{fe} = \frac{L_1}{L_2} \tag{L}$$

In practical oscillators, to ensure oscillations, the ratio $\frac{L_1}{L_2}$ is kept smaller than h_{fe}

$$\therefore \qquad h_{fe} \geq \frac{L_1}{L_2} \tag{M}$$

8.11 CRYSTAL OSCILLATOR

A crystal oscillator is basically a tuned circuit oscillator. It has the same circuit topology as the colpitts oscillator except that it uses a piezo electric crystal instead of an inductor. The crystal quartz usually has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate. Crystal oscillators are used in communication transmitters and receivers where high frequency stability is required.

8.12 PIEZO ELECTRIC EFFECT

Many naturally available crystals like Rochelle salt, tourmaline, quartz etc., exhibit piezoelectric effect. Piezoelectric effect is an electromechanical phenomenon. If the crystal is mechanically vibrated it develops an AC voltage across the ends of the face of the crystal. If an AC field is applied across the face of the crystal it vibrates mechanically. The natural resonant frequency of the crystal depends upon the dimensions of the crystal and also on the mechanical orientation of the crystal structure. The resonant frequency of the crystal is inversely proportional to the thickness of the crystal. Thus the frequency of oscillations increases as the thickness of the crystal decreases.

Quartz crystals are the natural choice in sinusoidal oscillators due to the following reasons:

- They are mechanically strong.
- They have good piezoelectric sensitivity.
- They are less expensive.

8.13 CHARACTERISTICS OF QUARTZ CRYSTALS

Figure 8.11(a) shows the piezoelectric crystal mounted between the plates and connected across an AC source of variable frequency. Figure 8.11(b) shows the electrical equivalent circuit of the mechanically vibrating crystal.

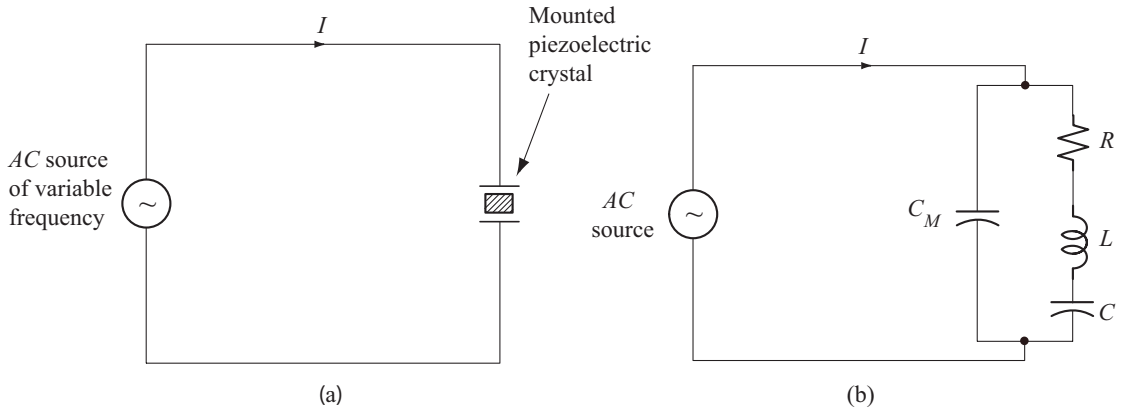


Fig. 8.11 Mounted piezoelectric crystal and its electrical equivalent circuit

L = Electrical equivalent inductance of crystal mass.
C = Electrical equivalent capacitance of the crystal compliance.
R = Electrical equivalent resistance of the crystal structure's internal friction.
C_M = Capacitance due to mechanical mounting of the crystal.

For a 2 MHz crystal the typical values of these parameters are:

$R = 82\ \Omega$ $\quad L = 0.52$ H
$C = 0.0122$ pF $\quad C_M = 4.27$ pF

This crystal has a quality factor of 80,000. Note that high quality factor implies, high frequency stability.

The frequency response of a crystal is obtained by plotting the current I through the crystal as a function of the frequency of ac source. Figure 8.12(a) shows the frequency response of the mounted crystal.

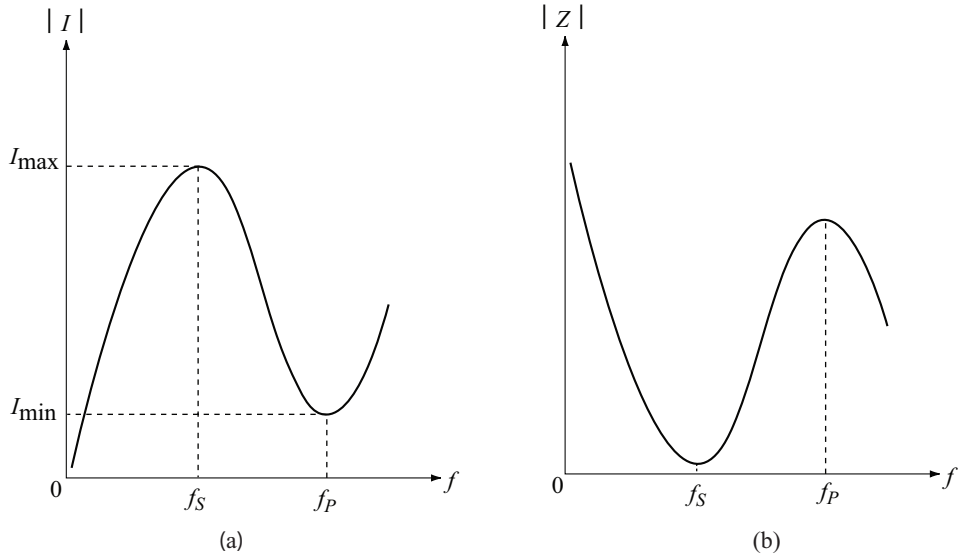


Fig. 8.12 (a) Frequency response of piezoelectric crystal
(b) Crystal impedance versus frequency

When the frequency of the ac source is equal to the frequency f_S, the current through the crystal becomes maximum (I_{max}). This condition is called the series resonance and f_S is called the series resonant frequency. Series resonance occurs when the reactance of L is equal to the reactance of C in the series RLC branch.

$$\text{i.e.,} \qquad \omega L = \frac{1}{\omega C}$$

$$\omega^2 = \frac{1}{LC}$$

$$\omega = \frac{1}{\sqrt{LC}}$$

$$f = f_S = \frac{1}{2\pi\sqrt{LC}} \tag{8.24}$$

Since the current is maximum, the impedance of the crystal is minimum.

When the frequency of the ac source is equal to the frequency $f_P > f_S$, the current through the crystal becomes minimum ($I_{\min}$). This condition is called parallel resonance and f_P is called the parallel resonant frequency. Parallel resonance occurs when the reactance of L is equal to the sum of the reactances of C_M and C.

i.e., $$\omega L = \frac{1}{\omega C_M} + \frac{1}{\omega C}$$

$$\omega^2 = \frac{1}{L}\left[\frac{1}{C_M} + \frac{1}{C}\right]$$

Taking $$\frac{1}{C_p} = \frac{1}{C_M} + \frac{1}{C} \tag{8.25}$$

or $$C_P = \frac{C_M C}{C_M + C} \tag{8.26}$$

We have, $$\omega^2 = \frac{1}{LC_P}$$

$$\omega = \frac{1}{\sqrt{LC_P}}$$

or $$f = f_p = \frac{1}{2\pi\sqrt{LC_P}} \tag{8.27}$$

Since the current is minimum, the impedance of the crystal is maximum.

Variation of $|Z|$ versus frequency is shown in Fig. 8.12(b).

Also since $C_M \gg C$, $$\frac{1}{C_M} \ll \frac{1}{C}$$

From Equation (8.25) we get

$$\frac{1}{C_p} \approx \frac{1}{C} \quad \Rightarrow \quad C_P \approx C$$

Now from Equation (8.27)

$$f_p \approx \frac{1}{2\pi\sqrt{LC}} = f_S \tag{8.28}$$

Note that f_P and f_S are very close to each other.

8.14 CRYSTAL REACTANCE

Figure 8.13 shows the variation of crystal reactance with frequency. Note that crystal exhibits inductive reactance only between f_S and f_P.

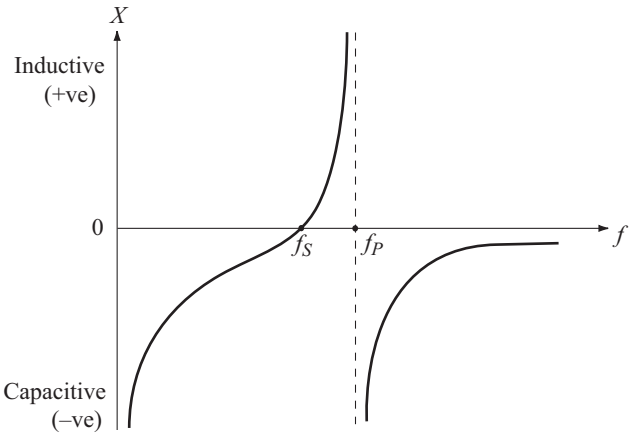


Fig. 8.13 Crystal reactance versus frequency

Since f_S is very close to f_P the crystal reactance is inductive only at $f_S \approx f_P$. When the inductor is replaced with the crystal in the colpitts oscillator, it oscillates only at that particular frequency of resonance where the crystal reactance is inductive.

8.15 TRANSISTOR CRYSTAL OSCILLATOR

The crystal can be operated either in the series resonant mode or in the parallel resonant mode. These two modes are discussed in the following sections.

8.15.1 Crystal Oscillator in Series Resonant Mode

Figure 8.14 shows the circuit of crystal oscillator in which the crystal is operated in series resonant mode.

The circuit uses a transistor CE stage. R_1, R_2 and R_E are selected so as to establish the desired Q point. C_E bypasses the emitter resistor R_E. The coupling capacitor C_C is selected such that it acts as a short circuit at the oscillator frequency. RFC acts as a short for dc current and open circuit for ac signal. Thus it prevents the oscillations from reaching the dc supply V_{CC}.

Crystal is used as series element in the feedback path, so that it operates in series resonant mode. Crystal has minimum impedance at the series resonant frequency f_S. Hence maximum feedback from collector to base occurs at this frequency. Thus oscillations are sustained at the series resonant frequency f_S.

Once the oscillations are set up the frequency of oscillations is held stabilized at f_S by the crystal. Changes in supply voltage, transistor device parameters etc have no effect on the circuit operating frequency. The frequency stability of the circuit is set by the frequency stability of the crystal, which is very high.

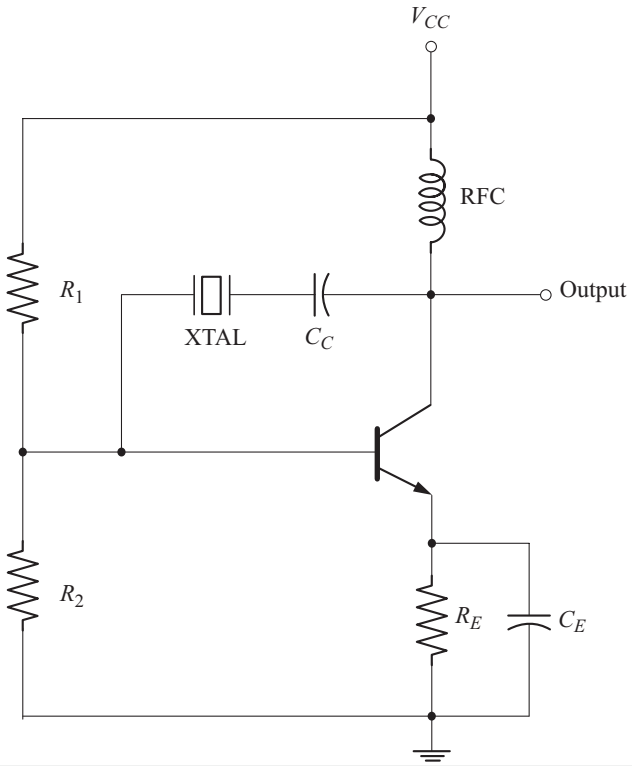


Fig. 8.14 Transistor crystal oscillator operating in series resonant mode

8.15.2 Crystal Oscillator in Parallel Resonant Mode

Figure 8.15 shows the circuit of crystal oscillator in which the crystal is operated in the parallel-resonant mode.

The purpose of R_1, R_2, R_E and RFC has been already explained in the previous section. Crystal is used as shunt element in the tank circuit so that it operates in the parallel resonant mode. Note that the tank circuit is same as that of colpitts oscillator with inductor replaced by the crystal.

Maximum voltage is developed across the crystal at its parallel resonant frequency since it has maximum impedance at this frequency. Also the crystal behaves as an inductor at its parallel resonant frequency. The crystal along with C_1 and C_2 gives the tank circuit effect at this frequency. Thus oscillations are sustained at the parallel resonant frequency f_P . Series combination of C_1 and C_2 acts as a voltage divider for the output voltage. The voltage across C_2 is fed to the emitter of the transistor. Note that the feedback voltage is maximum at the parallel resonant frequency of the crystal.

C_B is the bypass capacitor, which acts as a short circuit at the oscillator frequency, creating ac ground at the base. As a result, oscillations will not reach the base and there is no feedback at the base terminal.

The frequency of oscillations is held stabilized at f_P by the crystal. Changes in supply voltage, transistor device parameters etc have no effect on the circuit operating frequency. The frequency stability of the circuit is set by the frequency stability of the crystal, which is very high.

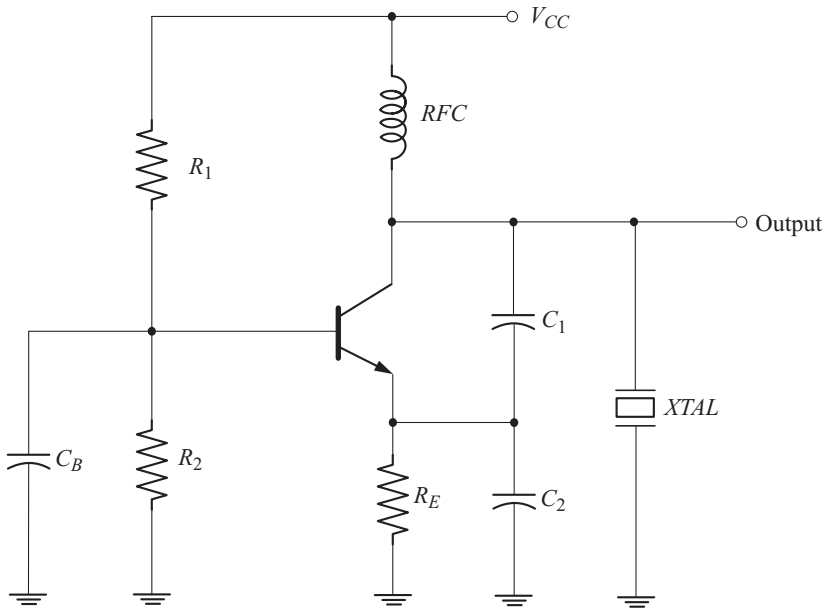


Fig. 8.15 Transistor crystal oscillator operating in parallel resonant mode

8.16 MERITS AND DEMERITS OF CRYSTAL OSCILLATOR

The merits of crystal oscillator are:

- The frequency stability of the crystal is very high. It is around one part in 10^6 i.e., 0.0001% per day. For example the frequency drift of a 1MHz crystal is 1Hz per day which is very neglible.
- Crystal with frequency upto 10 MHz can be constructed with very high frequency stability.
- The temperature stability of a crystal is very good. i.e., the frequency drift due to temperature change is negligibly small. Typically the frequency drift for 1°C rise in temperature of the crystal is around 10 – 12 Hz per mega hertz.
- Quartz crystals are readily available in nature. The crystal is very small in size, inexpensive and lighter in weight.
- Crystal replaces inductor in the tank circuit. As a result, crystal oscillator circuits are less bulky, inexpensive and lighter in weight.

The demerits of the crystal oscillator are:

- Crystals are very delicate and hence require careful handling.
- The thickness of the crystal is inversely proportional to the frequency. Hence higher frequency crystals are thinner in size and are mechanically weak.
- The frequency of the crystal depends on the crystal dimensions and how the crystal is cut. Hence for a given crystal, its frequency of oscillations is fixed. Whenever a new frequency of oscillation is required, the whole circuit is to be redesigned and the crystal is to be replaced.

8.17 APPLICATIONS OF CRYSTAL OSCILLATOR

Following are the some of the applications of crystal oscillators:

- To generate clock signal for computers and other synchronous digital systems.
- To generate carrier frequency in communication transmitters.
- To generate local oscillator frequency in communication receivers. Crystal kept in temperature controlled oven is used to generate highly precise clock which is used for time standards.

Example 8.22

A crystal has the following parameters:

$L = 0.334$ H $\quad C = 0.065$ pF
$C_M = 1$ pF $\quad R = 5.5$ kΩ

(a) Calculate the series resonant frequency.
(b) Calculate the parallel resonant frequency.
(c) By what percent does the parallel-resonant frequency exceed the series resonant frequency?
(d) Find the Q of the crystal.

Solution

(a) $$f_S = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{(0.334)(0.065\times10^{-12})}} = 1.08016 \text{ MHz}$$

$$\omega_S = 2\pi f_S = 6.7868 \text{ M rad /sec}$$

(b) $$f_P = \frac{1}{2\pi\sqrt{LC_P}}$$

$$C_P = \frac{CC_M}{C+C_M} = \frac{(0.065 \text{ pF})\,(1 \text{ pF})}{0.065 \text{ pF}+1 \text{ pF}} = 0.061 \text{ pF}$$

$$f_P = \frac{1}{2\pi\sqrt{(0.334)\,(0.061\times10^{-12})}} = 1.1150 \text{ MHz}$$

$$\omega_P = 2\pi f_P = 7.005 \text{ M rad /sec}$$

(c) % difference between f_P and $f_S = \frac{f_P - f_S}{f_S} \times 100\%$

$$= \frac{1.1150 - 1.08016}{1.08016} \times 100\ \% = 3.22\ \%$$

f_P is more than f_S by 3.22%

(d) $$Q = \frac{\omega_S L}{R} = \frac{\left(6.7868\times10^6\right)\left(0.334\right)}{\left(5.5\times10^3\right)} = 412.14$$

Example 8.23

(a) Prove that the ratio of the parallel to series resonant frequencies is given approximately by $1 + \dfrac{C}{2\,C_M}$.

(b) If $C = 0.04$ pF and $C_M = 2$ pF, by what percent is the parallel-resonant frequency greater than the series resonant frequency?

Solution

(a) $$f_S = \frac{1}{2\pi\sqrt{LC}}$$

$$f_P = \frac{1}{2\pi\sqrt{LC_P}}$$

$$\frac{f_P}{f_S} = \sqrt{\frac{C}{C_p}}$$

But $$C_P = \frac{C\,C_M}{C+C_M}$$

Now $$\frac{f_P}{f_S} = \sqrt{C\times\left[\frac{C+C_M}{C\;C_M}\right]}$$

$$\frac{f_P}{f_S} = \left[1+\frac{C}{C_M}\right]^{1/2} \qquad \text{(A)}$$

Since $\dfrac{C}{C_M} \ll 1$, we can write Equation (A) using binomial expansion as

$$\frac{f_P}{f_S} \approx 1 + \frac{C}{2\,C_M} \qquad \text{(B)}$$

(b) $C = 0.04$ pF $\quad C_M = 2$ pF

$$\frac{f_P}{f_S} = 1 + \frac{0.04\text{ pF}}{2\times 2\text{ pF}} = 1.01$$

$f_P = 1.01\,f_S$ or f_P is 101% of f_S

$\therefore$ f_P is greater than f_S by 1%.

Exercise Problems

8.1 In a transistor RC phase shift oscillator R = 3.9 kΩ and C = 0.01 μF. If R_C = 4.7 kΩ calculate the frequency of oscillation.

8.2 Find the values of R and C for a transistor RC-phase shift oscillator for a frequency of 3 kHz. R_C = 5 kΩ and for the transistor h_{fe} = 100.

8.3 Design the component values for a Weinbridge oscillator for a frequency of 1.5 kHz.

8.4 In a transistor Hartley oscillator $L_1 = L_2$ = 10 mH, M = 50 μH and C = 0.01 μF. Calculate the frequency of oscillations.

8.5 In a transistor Colpitt's oscillator $C_1 = C_2$ = 0.01 μF, L = 20 mH. Calculate the frequency of oscillation.

8.6 A Quartz crystal has the following data:

L = 0.5 H R = 1 kΩ C = 2 pF C_M = 20 pF.

Calculate the following:

(a) Series resonant frequency
(b) Parallel resonant frequency
(c) Quality factor

Chapter 9

FET Amplifiers

Junction field-effect transistor (JFET) is basically a voltage controlled device. The output current of the device is controlled by the input voltage. FET has an excellent voltage gain and high input impedance. Because of high input impedance, the ac equivalent model is simpler than that of BJT which makes the ac analysis of FET amplifiers less complex. In this chapter analysis of common-source, common gate and common drain JFET amplifiers have been carried out. The analysis of DMOSFET and EMOSFET amplifiers have also been considered. A few design examples are included at the end of this chapter.

9.1 BASICS OF JUNCTION FIELD EFFECT TRANSISTOR

A Junction field-effect transistor, abbreviated as JFET or simply FET, is a three terminal semiconductor device in which the current flow is due to only one type of carriers i.e., either electrons or holes. Hence it is a unipolar device.

The name field-effect transistor is derived from the fact that the current flow is controlled by an electric field setup in the device by an externally applied voltage. Unlike BJT which is a current controlled device, the FET is a voltage controlled device.

Figure 9.1 shows the circuit symbols of *n*-channel and *p*-channel FETs. The three terminals of the FET are Drain (*D*), Source (*S*) and Gate (*G*) which are analogous to the collector, emitter and base of the BJT respectively. In *n* channel FET, the current flow is due to only electrons whereas in *p*-channel FET it is due to only holes.

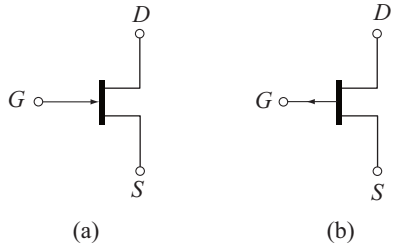


Fig. 9.1 (a) Circuit symbol of n-channel FET
(b) Circuit symbol of p-channel FET

9.2 FET CURRENT EQUATION

Figure 9.2 shows the biasing arrangement for an *n*-channel FET. Observe that the gate is made negative with respect to source and the drain positive with respect to source.

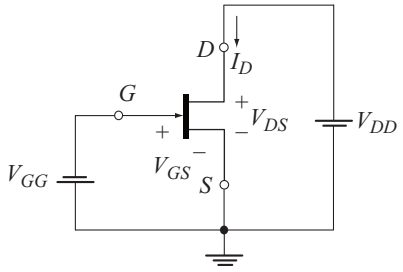


Fig. 9.2 Biasing arrangement for n-channel FET

In FET the drain current I_D is controlled by the gate-source voltage V_{GS}. The relationship between I_D and V_{GS} is defined by shockley's equation given by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \tag{9.1}$$

When $V_{GS} = 0$ and $V_{DS} > |V_p|$,

$$I_D = I_{DSS} \tag{9.2}$$

I_{DSS} is the maximum drain current in the FET which occurs when $V_{GS} = 0$ and $V_{DS} > |V_p|$.

When $V_{GS} = V_p$

$I_D = 0$

V_p is called the pinch-off voltage

V_p is negative for *n*-channel FETs and positive for *p* channel FETs.

9.3 TRANSFER CHARACTERISTICS

Transfer characteristic is the plot of I_D versus V_{GS}. Figure 9.3 shows the transfer characteristics of FET. Transfer characteristics is defined by the shockley's equation.

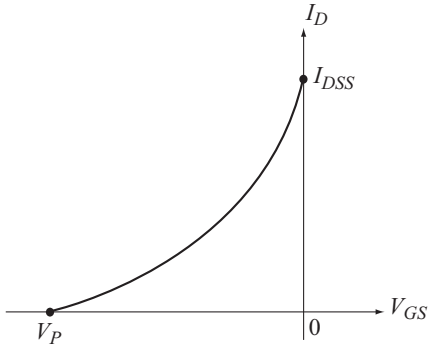


Fig. 9.3 Transfer characteristics of FET

Observe that I_D has the maximum value of I_{DSS} when $V_{GS} = 0$. It decreases for negatively increasing V_{GS} and becoming zero at $V_{GS} = V_p$. It should be noted that I_D is a non linear function of V_{GS}.

9.4 DRAIN CHARACTERISTICS

Figure 9.4 shows the drain characteristics of FET.

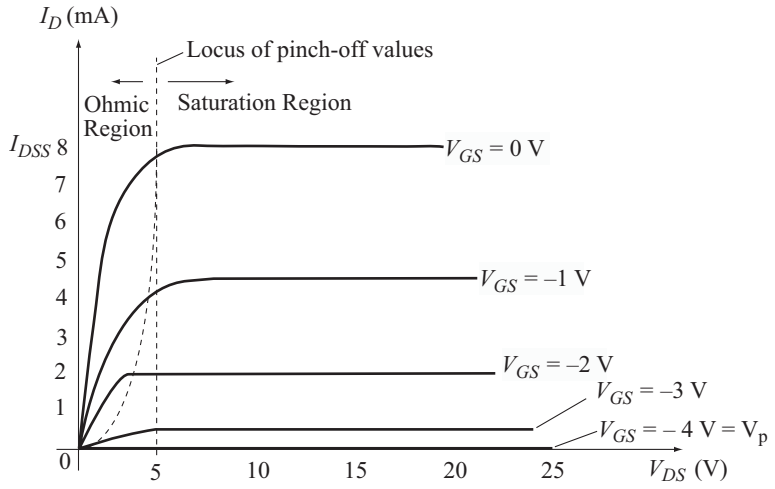


Fig. 9.4 Drain characteristics of FET

The region to the right of the pinch-off locus is called the saturation region. In this region I_D varies very little with V_{DS} but changes significantly with V_{GS}. This is the linear amplification region for the FET. When biased in this region, FET amplifies the applied signal with minimum distortion.

Therefore the biasing requirements for *n*-channel FET to work as a linear amplifying device are:

$$0 > V_{GS} > V_p \tag{9.3}$$

and

$$V_{DS} > |V_p| \tag{9.4}$$

9.5 FET SMALL-SIGNAL MODEL

The small-signal ac model of FET is required in the ac analysis of FET amplifiers. The small-signal ac model is developed using the following facts.

- The impedance between gate and source terminals of an FET is very high. Typically it is in the order of 1000 MΩ. Hence FET can be represented by an open circuit between gate and source terminals.
- The drain current is controlled by the gate-source voltage.

i.e., $I_d \propto V_{gs}$

or

$$I_d = g_m V_{gs} \tag{9.5}$$

g_m is called the transconductance of FET. g_m is alternatively represented by y_{fs}. y_{fs} stands for forward transfer admittance.

As per Equation (9.5), FET can be modelled as a voltage controlled current source, $I_d = g_m V_{gs}$, between drain and source terminals.

- In the saturation region, I_d changes slightly with V_{ds}

ie $$I_d \propto V_{ds}$$

or $$I_d = \left[\frac{1}{r_d}\right] V_{ds} \tag{9.6}$$

r_d is the output impedance of FET.

$$r_d = \frac{1}{y_{os}} \tag{9.7}$$

y_{os} is the output admittance.

As per Equation (9.6), FET can be modelled as a resistor r_d, connected between the drain and source terminals. Typically r_d lies in the range 20 kΩ – 100 kΩ.

The lower case suffixes are used to imply that I_d, V_{gs}, V_{ds}, g_m and r_d are all ac values.

Figure 9.5 shows the small-signal ac model of FET. This model applies for both *n*-channel *p*-channel and FETs.

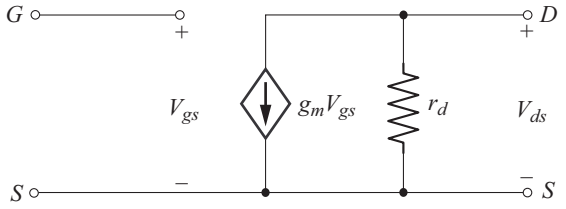


Fig. 9.5 Small signal ac model of FET

Example 9.1

An FET has y_{fs} = 4 mS and y_{os} = 33.33 μS

(a) Find g_m and r_d

(b) Sketch the small-signal ac model of FET

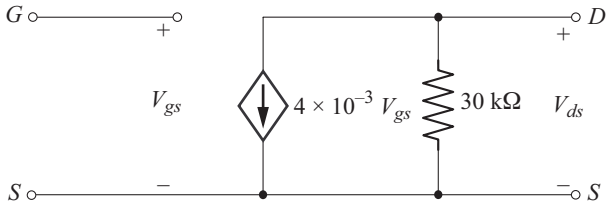
Solution

(a) $$g_m = y_{fs} = 4 \text{ mS}$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{33.33\,\mu\text{S}}$$

$$r_d = 30 \text{ k}\Omega$$

(b) The small-signal ac model is shown below.



9.6 GRAPHICAL DETERMINATION OF g_m

The transconductance g_m is given by the slope of the transfer characteristics at the Q point.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{Q\text{ point}} \tag{9.8}$$

Graphical determination of g_m is illustrated in Fig. 9.6.

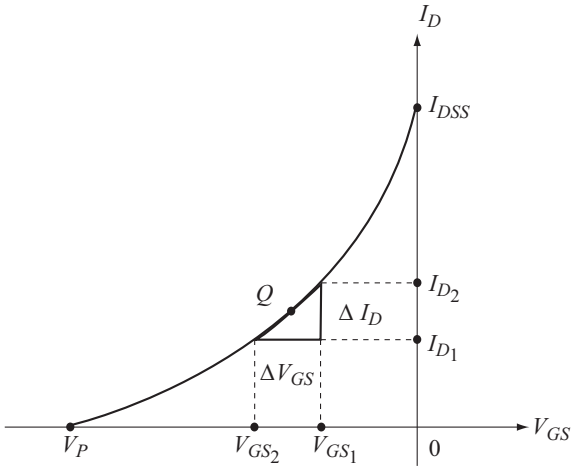


Fig. 9.6 Graphical determination of g_m

From Fig. 9.6 we have

$$\Delta I_D = I_{D_2} - I_{D_1}$$
$$\Delta V_{GS} = V_{GS_2} - V_{GS_1}$$

Now

$$g_m = \frac{I_{D_2} - I_{D_1}}{V_{GS_2} - V_{GS_1}} \tag{9.9}$$

9.7 MATHEMATICAL EXPRESSION FOR g_m

g_m is given by the slope of the transfer characteristics at the Q point. But slope of transfer characteristics is given by the derivative of I_D with respect to V_{GS} at the Q point.

$$\therefore \quad g_m = \left.\frac{d I_D}{d V_{GS}}\right|_{Q\text{–point}} \tag{9.10}$$

But $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

Now $$g_m = 2\, I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]\left[\frac{-1}{V_p}\right] \tag{9.11}$$

In Equation (9.11), $\frac{V_{GS}}{V_p}$ is positive, for both *n*-channel and *p*-channel FETs. To get positive value for g_m, let us omit negative sign and write $|V_p|$ instead of V_p.

Hence $$g_m = \frac{2 I_{DSS}}{|V_p|}\left[1 - \frac{V_{GS}}{V_p}\right] \tag{9.12}$$

When $V_{GS} = 0$,

$$g_m = \frac{2 I_{DSS}}{|V_p|}$$

Note that this is the highest possible value of g_m.

Let $$g_{m_o} = \frac{2 I_{DSS}}{|V_p|} \tag{9.13}$$

Using Equation (9.13) in Equation (9.12) we have

$$g_m = g_{m_o}\left[1 - \frac{V_{GS}}{V_p}\right] \tag{9.14}$$

Observe from Equation (9.14) that, g_m decreases from g_{m_o} to 0 when V_{GS} is increased negatively from 0 to V_p.

From Equation (9.14) we have

$$g_m = \left[-\frac{g_{m_o}}{V_p}\right] V_{GS} + g_{m_o} \tag{9.15}$$

Equation (9.15) represents a straight line in $V_{GS} - g_m$ plane with slope $-\frac{g_{m_o}}{V_p}$ and intercept g_{mo}. The plot of g_m versus V_{GS} is shown in Fig. 9.7.

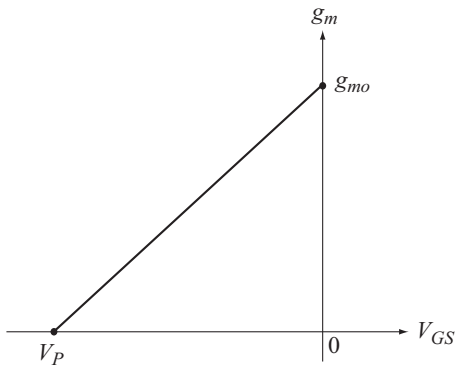


Fig. 9.7 Plot of g_m versus V_{GS}

Example 9.2

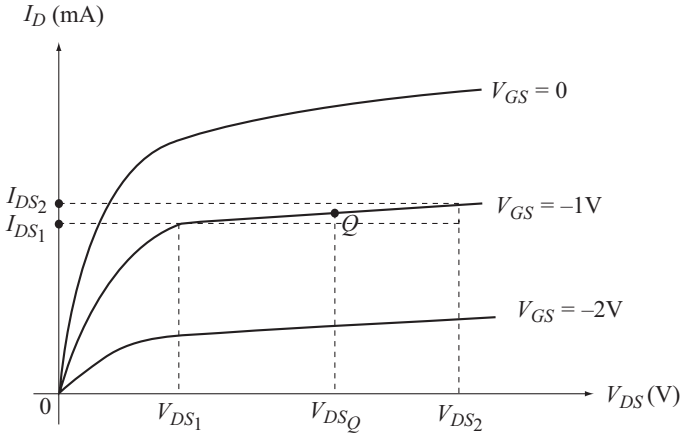
Explain the graphical determination of r_d.

Solution

The output impedance is defined as the slope of the horizontal portion *of* the drain characteristics at the *Q* point.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{const}}$$

The calculation of r_d is illustrated in the following figure.



$$r_d = \left.\frac{V_{DS_2} - V_{DS_1}}{I_{DS_2} - I_{DS_1}}\right|_{V_{GS}=-1\text{V}}$$

Typically r_d is in the range of 20 kΩ – 100 kΩ. Under the ideal situation, the curve is perfectly horizontal. As a result, $\Delta I_D = 0$ and hence $r_d = \infty$.

9.8 RELATION BETWEEN I_D AND g_m

From Shockley's equation we have

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$$

$$\therefore \quad \frac{I_D}{I_{DSS}} = \left[1-\frac{V_{GS}}{V_p}\right]^2$$

$$\Rightarrow \quad \left[1-\frac{V_{GS}}{V_p}\right] = \sqrt{\frac{I_D}{I_{DSS}}} \tag{9.16}$$

But $$g_m = g_{m_o}\left[1-\frac{V_{GS}}{V_p}\right]$$

$$\therefore \quad g_m = g_{m_o}\sqrt{\frac{I_D}{I_{DSS}}} \tag{9.17}$$

Observe from Equation (9.17) that, g_m varies as the square root of I_D.

9.9 JFET COMMON-SOURCE AMPLIFER USING FIXED BIAS CONFIGURATION

JFET common-source amplifier is analogous to BJT common-emitter amplifer. Figure 9.8 shows the circuit of common-source amplifier using fixed bias configuration.

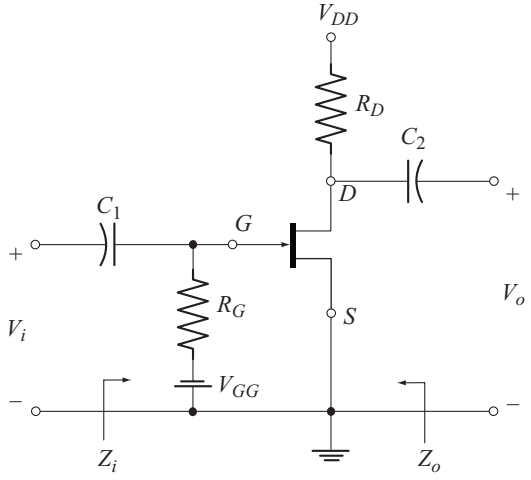


Fig. 9.8 JFET common-source amplifier using fixed bias configuration

Due to high input impedance of JFET, the dc current through R_G is almost zero. Thus a constant bias voltage $-V_{GG}$ is applied between the gate and source terminals. Hence the name fixed bias configuration.

The input coupling capacitor isolates the dc supply $-V_{GG}$ and the ac input signal V_i. The output coupling capacitor isolates the dc supply V_{DD} and the load. They are properly selected so as to represent short-circuits at the lowest frequency of operation.

AC Equivalent Circuit

The ac equivalent circuit is obtained by short circuiting the capacitors C_1 and C_2 and reducing the dc sources V_{DD} and $-V_{GG}$ to zero, as shown in Fig. 9.9.

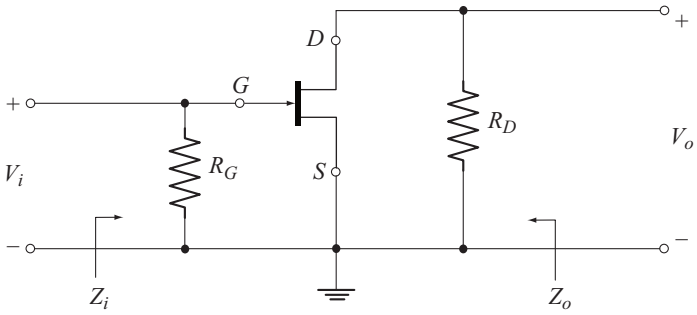


Fig. 9.9 Ac equivalent circuit of JFET common-source amplifier

Let us replace the JFET by its small-signal ac equivalent circuit. The resulting circuit is shown in Fig. 9.10.

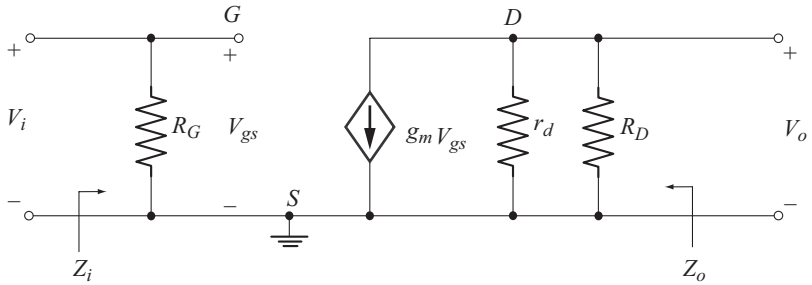


Fig. 9.10 Ac equivalent using small-signal ac model of JFET

Input Impedance (Z_i)

Observe in Fig. 9.10 that, there is an open circuit between the gate and source terminals. Hence the input impedance is nothing but R_G.

$$\text{ie} \qquad Z_i = R_G \tag{9.18}$$

Output Impedance (Z_o)

To find the output impedance we have to set V_i to zero. Note that $V_i = V_{gs}$. Hence, with $V_i = 0$, $g_m V_{gs} = 0$. Thus the current source $g_m V_{gs}$ is represented by an open circuit as shown in Fig. 9.11.

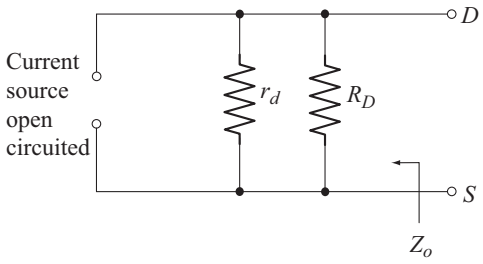


Fig. 9.11 Circuit to find Z_o

From the circuit of Fig. 9.11, the output impedance Z_o is given by

$$Z_o = r_d \,||\, R_D \tag{9.19}$$

Voltage Gain (A_V)

$$A_V = \frac{V_o}{V_i} \tag{9.20}$$

From Fig. 9.10,

$$V_i = V_{gs} \tag{9.21}$$

The output circuit of Fig. 9.10 is redrawn in Fig. 9.12 for convenience.

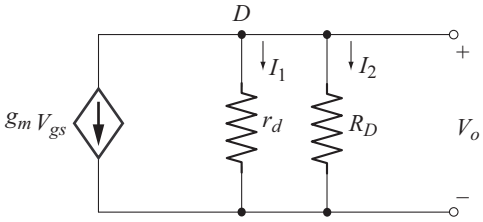


Fig. 9.12 Output ac equivalent Circuit

Appling KCL at the node *D* we have

$$g_m V_{gs} + I_1 + I_2 = 0$$

$$I_1 = \frac{V_o}{r_d} \quad \text{and} \quad I_2 = \frac{V_o}{R_D}$$

Using these relations in the above equation, we get

$$g_m V_{gs} + \frac{V_o}{r_d} + \frac{V_o}{R_D} = 0$$

$$g_m V_{gs} = -V_o \left[\frac{1}{r_d} + \frac{1}{R_D}\right]$$

$$g_m V_{gs} = -V_o \left[\frac{r_d + R_D}{r_d\ R_D}\right]$$

$$V_o = -g_m V_{gs} \left[\frac{r_d\ R_D}{r_d + R_D}\right]$$

or
$$V_o = -g_m V_{gs} [r_d \,||\, R_D] \tag{9.22}$$

Using Equations (9.21) and (9.22) in Equation (9.20), we have

$$A_V = \frac{-g_m V_{gs} \left[r_d \,||\, R_D\right]}{V_{gs}}$$

$$A_V = -g_m [r_d \,||\, R_D] \tag{9.23}$$

The negative sign in Equation (9.23) reveals that, V_i and V_o are 180° out of phase. Note that common-source configuration is an inverting amplifier.

For $r_d \geq 10\ R_D$

When $r_d = 10\ R_D$

$$r_d \,||\, R_D = 0.909\ R_D$$

Hence when $r_d \geq 10\ R_D$, we can take

$$r_d \,||\, R_D \approx R_D$$

From Equation (9.19)

$$Z_o \approx R_D \tag{9.24}$$

From eqution (9.23)

$$A_V \approx -g_m R_D \tag{9.25}$$

Important characteristics of common-source configuration

Based on the results derived, we can attribute the following characteristics to common-source configuration

- High input impedance [$Z_i \approx R_G$]
- Medium high output impedance [$Z_o \approx R_D$]
- Medium voltage gain [$A_V \approx -g_m R_D$]
- 180° phase difference between input and output voltages.

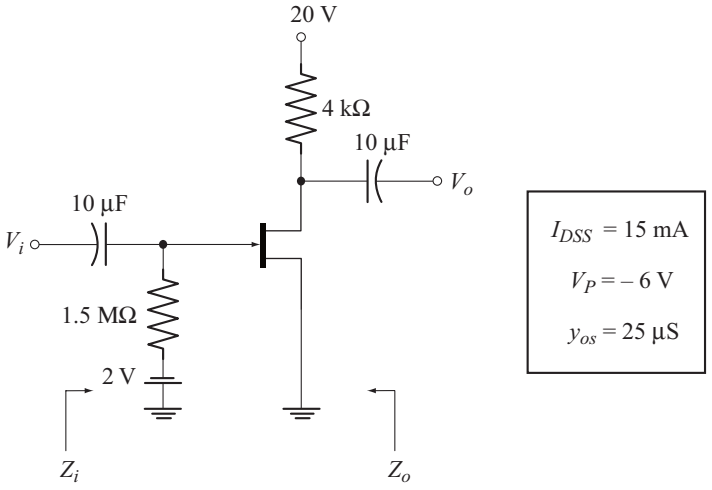
Example 9.3

For the FET amplifer shown below:

(a) Calculate Z_i and Z_o

(b) Calculate A_V

(c) Calculate Z_i, Z_o and A_V, neglecting the effect of r_d and compare the results.



Solution

First we have to find g_m and r_d

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|} = \frac{2(15\text{ mA})}{6\text{ V}} = 5\text{ mS}.$$

$$V_{GS_Q} = -V_{GG} = -2\text{ V}$$

$$g_m = 5\text{ mS}\left[1 - \frac{-2\text{ V}}{-6\text{ V}}\right] = 3.33\text{ mS}$$

$$r_d = \frac{1}{y_{o_s}} = \frac{1}{25\,\mu\text{S}} = 40\text{ k}\Omega.$$

(a) $Z_i = R_G = 1.5\text{ M}\Omega$

$Z_o = r_d \,||\, R_D = 40\text{ k}\Omega \,||\, 4\text{ k}\Omega = 3.63\text{ k}\Omega.$

(b) $A_V = -g_m[r_d \,||\, R_D] = -[3.33\text{ mS}][3.63\text{ k}\Omega] = -12.08$

(c) $r_d = 40\text{ k}\Omega$ and $10\,R_D = 40\text{ k}\Omega.$

Since $r_d = 10\,R_D$, we can ignore the effect of r_d. Neglecting r_d we have:

$$Z_i = R_G = 1.5\text{ M}\Omega$$

$$Z_o \approx R_D = 4\ \text{k}\Omega$$
$$A_V \approx -g_m R_D = -[3.33\ \text{mS}]\ [4\ \text{k}\Omega] = -13.32.$$

The results are compared in the following table

Parameter	*With r_d*	*With out r_d*
Z_i	1.5 MΩ	1.5 MΩ
A_V	– 12.08	– 13.32
Z_o	3.63 kΩ	4 kΩ

Observe that the results closely agree since $r_d = 10\ R_D$.

9.10 JFET COMMON SOURE AMPLIFIER USING SELF-BIAS CONFIGURATION

Figure 9.13(a) shows JFET common-source amplifier using self bias. Observe that, this circuit requires only one dc supply V_{DD} to establish the desired operating point. The dc voltage across R_S will serve as the biasing voltage between gate and source terminals.

$$\therefore \qquad V_{GS_Q} = -I_{DQ} R_S$$

The functions of C_1 and C_2 have already been explained in section 9.9. C_S is the source bypass capacitor. For ac operation it creates a short circuit across R_S, thus preventing ac negative feedback through R_S. Without C_S, the negative feedback through R_S reduces the voltage gain. Also C_S allows the dc bias current I_{DQ} through R_S, by acting as an open circuit.

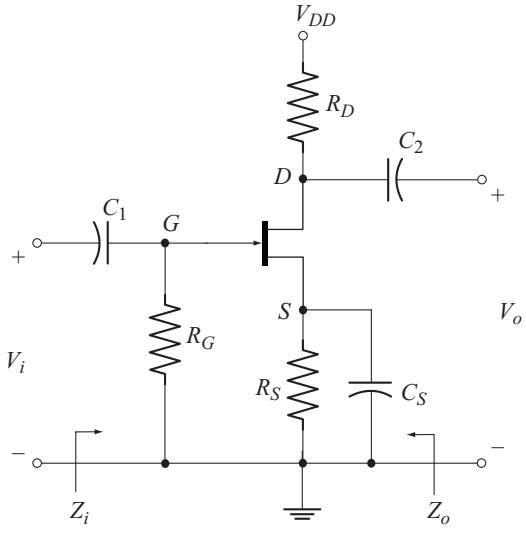


Fig. 9.13(a) JFET Common source amplifier using self bias configuration

The ac equivalent circuit is drawn in Fig 9.13(b) by short circuiting the capacitors C_1, C_2 and C_S and reducing V_{DD} to zero.

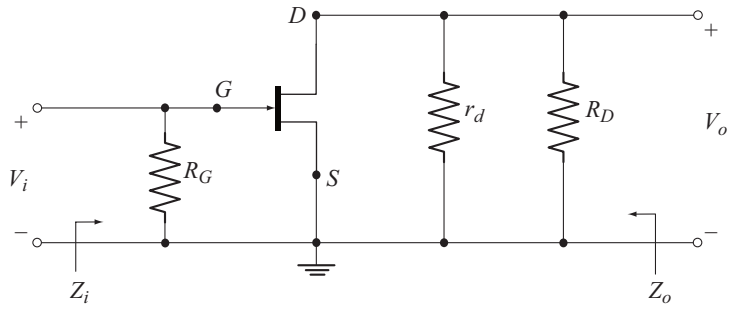


Fig. 9.13(b) AC equivalent circuit of the amplifier of Fig 9.13(a)

The ac equivalent circuit is redrawn in Fig. 9.14 by replacing the JFET with its small-signal ac model.

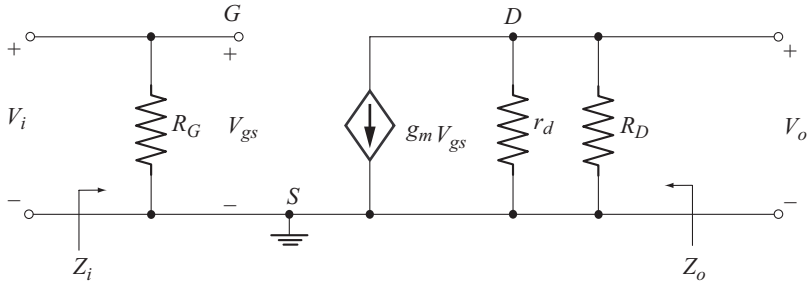


Fig. 9.14 AC equivalent circuit using small signal model

Observe that this circuit is same as that given in Fig. 9.10. Therefore all the results derived in section 9.9 can be readily applied to this circuit.

When the effect of r_d is considered.

$$Z_i = R_G \tag{9.26}$$

$$Z_o = r_d \,||\, R_D \tag{9.27}$$

$$A_V = -g_m [r_d \,||\, R_D] \tag{9.28}$$

For $r_d \geq 10\ R_D$

$$Z_o \approx R_D \tag{9.29}$$

$$A_V \approx -g_m R_D \tag{9.30}$$

The negative sign in the expression for A_V reveals that V_i and V_o are 180° out of phase.

Example 9.4

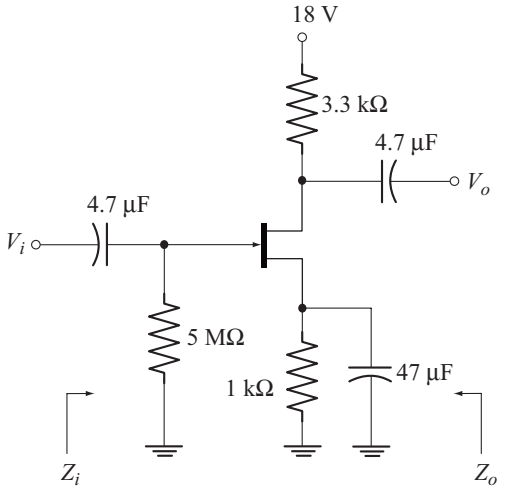
For the JFET amplifier shown below:

(a) Calculate Z_i and Z_o

(b) Calculage A_V

(c) Find V_o if V_i = 10 mV(p – p)

(d) Find Z_i, Z_o, A_V and V_o neglecting the effect of r_d.



I_{DSS} = 8 mA

I_{DQ} = 2.5 mA

V_P = – 5 V

y_{os} = 20 µS

Solution

Let us find g_m and r_d using the given data

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|} = \frac{2(8\text{ mA})}{5\text{V}} = 3.2\text{ mS}$$

$$V_{GS_Q} = -I_{DQ}R_S = -(2.5\text{ mA})(1\text{ k}\Omega) = -2.5\text{ V}$$

Now

$$g_m = 3.2\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-5\text{ V}}\right] = 1.6\text{ mS}$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{20\,\mu\text{S}} = 50\text{ k}\Omega$$

(a)

$$Z_i = R_G = 5\text{ M}\Omega$$

$$Z_o = r_d \,||\, R_D$$

$$= 50\text{ k}\Omega \,||\, 3.3\text{ k}\Omega = 3.09\text{ k}\Omega$$

(b)

$$A_V = -g_m[r_d \,||\, R_D] = -(1.6\text{ mS})(3.09\text{ k}\Omega) = -4.944$$

(c) $V_o = A_V V_i = (-4.944)\,(10\text{ mV}) = -49.44\text{ mV}_{(p-p)}$

(d) $r_d = 50\text{ k}\Omega$ and $10\,R_D = 33\text{ k}\Omega$

Since $r_d > 10\,R_D$ we can neglect r_d. With r_d neglected, we get the following results.

$$Z_i = R_G = 5\text{ M}\Omega$$

$$Z_o = R_D = 3.3\text{ k}\Omega$$

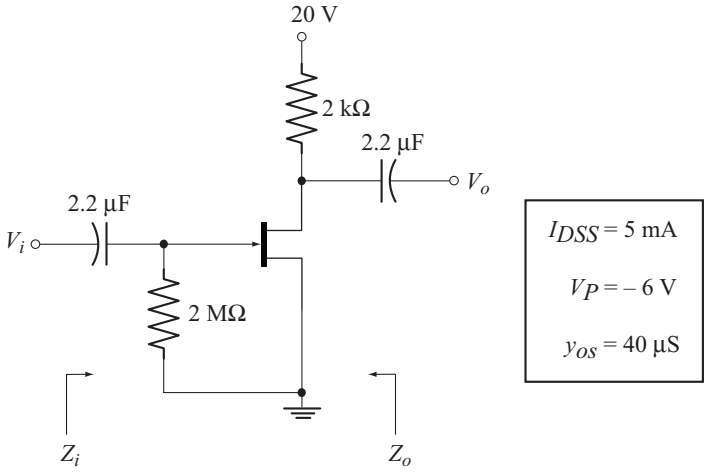
$$A_V = -g_m R_D = -(1.6\text{ mS})\,(3.3\text{ k}\Omega) = -5.28$$

$$V_o = (-5.28)\,(10\text{ mV}) = -52.8\text{ mV}_{(p-p)}$$

Example 9.5

For the JFET amplifier shown below:

(a) Calculate Z_i and Z_o
(b) Calculate A_V
(c) Calculate V_o if $V_i = 50$ mV (rms)
(d) Calculate Z_i, Z_o, A_V and V_o, neglecting r_d



$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$V_{GS_Q} = I_{D_Q} R_S$$

Since $R_S = 0$, $V_{GS_Q} = 0$

$\therefore$ $g_m = g_{m_o}$

$$= \frac{2\,I_{DSS}}{|V_p|} = \frac{(2)(5\text{ mA})}{6\text{ V}} = 1.67\text{ mS}$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{40\,\mu S} = 25\ k\Omega$$

(a) $Z_i = R_G = 2\ M\Omega$

$Z_o = r_d \,||\, R_D = 25\ k\Omega \,||\, 2\ k\Omega = 1.85\ k\Omega$

(b) $A_V = -g_m\,[r_d \,||\, R_D] = -\,[1.67\ mS]\,[1.85\ k\Omega] = -3.08$

(c) $V_o = A_V V_i = (-3.08)\,(50\ mV) = -154\ mV\ (rms)$

(d) $r_d = 25\ k\Omega$ and $10\,R_D = 20\ k\Omega$

Since $r_d > 10\,R_D$, we can neglect r_d.

Results with r_d neglected

$Z_i = R_G = 2\ M\Omega$

$Z_o = R_D = 2\ k\Omega$

$A_V = -g_m R_D = -\,[1.67\ mS]\,[2\ k\Omega] = -3.34$

$V_o = AV_i = (-3.34)\,(50\ mV) = -167\ mV\ (rms)$

9.11 JFET COMMON-SOURCE AMPLIFIER WITH UNBYPASSED R_S

Figure 9.15 shows the circuit of JFET common-source amplifier with unbypassed R_S. Since C_S is not present, ac feedback occurs through R_S. Note that the feedback voltage across R_S is in series with V_i and the feedback is negative.

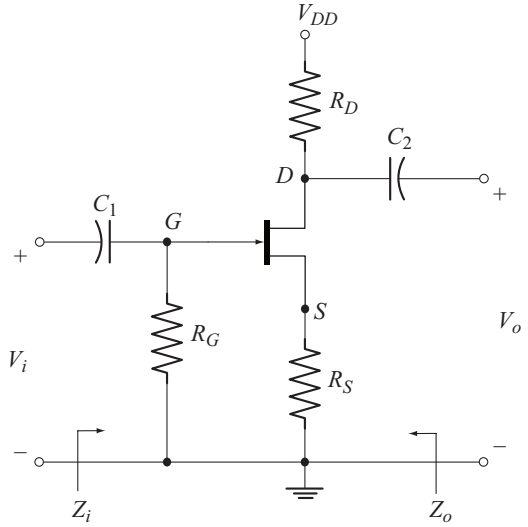


Fig. 9.15 JFET Common-source amplifier with unbypassed R_s

The ac equivalent circuit using the small signal ac model of JFET is drawn in Fig. 9.16

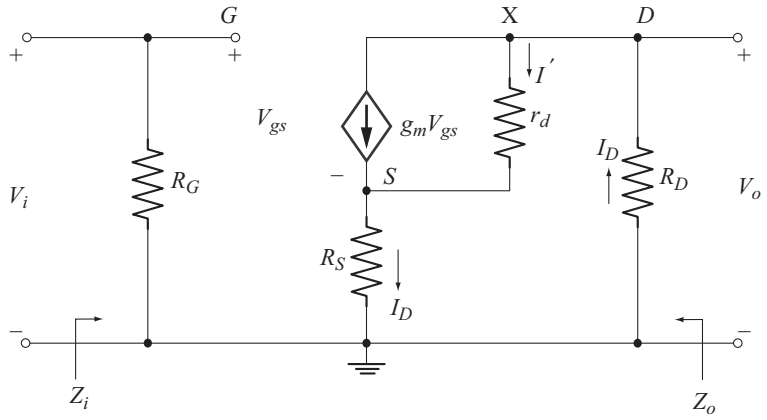


Fig. 9.16 Ac equivalent of the amplifier of Fig. 9.15

Input Impedance **(z_i)**

From the input circuit of Fig. 9.16, we have

$$Z_i = R_G \tag{9.31}$$

Voltage Gain **(A_V)**

$$A_V = \frac{V_o}{V_i} \tag{9.32}$$

$$V_o = -I_D R_D \tag{9.33}$$

To find I_D let us apply KCL at node *X*.

$$I_D = I' + g_m V_{gs} \tag{9.34}$$

Writing KVL to the path consisting of R_D, r_d and R_S we get

$$-I_D R_D - I' r_d - I_D R_S = 0$$

$$I' r_d = -I_D [R_D + R_S]$$

$$I' = -I_D \left[\frac{R_D + R_S}{r_d}\right] \tag{9.35}$$

Using Equation (9.35) in Equation (9.34) we get

$$I_D = -I_D \left[\frac{R_D + R_S}{r_d}\right] + g_m V_{gs} \tag{9.36}$$

To find V_{gs} let us apply kVL to the path consisting of V_i, V_{gs} and R_S we get

$$V_i - V_{gs} - I_D R_S = 0$$

$$V_{gs} = V_i - I_D R_S \tag{9.37}$$

Using this relation is Equation (9.36) we get

$$I_D = -I_D \left[\frac{R_D + R_S}{r_d}\right] + g_m [V_i - I_D R_S]$$

$$I_D \left[1 + \frac{R_D + R_S}{r_d} + g_m R_S\right] = g_m V_i$$

$$I_D = \frac{g_m V_i}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} \tag{9.38}$$

Substituting Equation (9.38) in Equation (9.33) we get

$$V_o = -\frac{g_m R_D V_i}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

Now $$A_V = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} \tag{9.39}$$

The negative sign in Equation (9.39) reveals that V_i and V_o differ in phase by 180°

Effect of Unbypassed R_S on Voltage Gain

If R_S is bypassed by C_S, it gets short circuited for ac operation. Therefore, substituting $R_S = 0$ in Equation (9.39),

we get $$A_V = -\frac{g_m R_D}{1 + \dfrac{R_D}{r_d}}$$

$$= -g_m \left[\frac{R_D r_d}{R_D + r_d}\right]$$

$$= -g_m [r_d \,||\, R_D]$$

This result is consistent with Equation (9.28) derived in section 9.10.

Comparing this result with Equation (9.39), we find that, unbypassing of R_S results in the drastic reduction of voltage gain.

Expression for A_V neglecting the Effect of r_d

Consider Equation (9.39)

If $$r_d \geq 10 (R_D + R_S)$$

or $$\left[\frac{R_D + R_S}{r_d}\right] \leq 0.1$$

$$1 + g_m R_S + \left[\frac{R_D + R_S}{r_d}\right] \approx 1 + g_m R_S$$

Now
$$A_V \approx -\frac{g_m R_D}{1 + g_m R_S} \tag{9.40}$$

Output Impedance (Z_o)

To develop the expression for Z_o we apply the following steps to the circuit of Fig. 9.16.

- The input voltage V_i is set to zero. As a result R_G gets short circuited.
- A voltage source V_o is connected between the output terminals.

The resulting circuit is shown in Fig. 9.17.

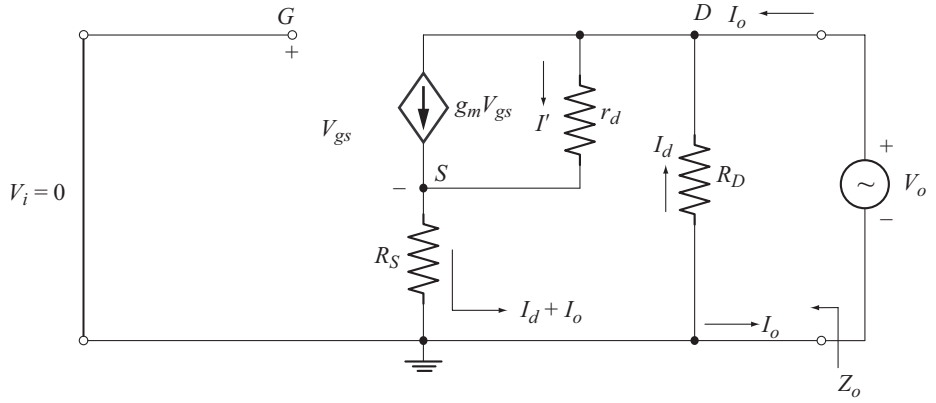


Fig. 9.17 Circuit to find Z_o

From Fig. 9.17, the output impedance is given by

$$Z_o = \frac{V_o}{I_o} \tag{9.41}$$

But
$$V_o = -I_d R_D$$

using this relation in Equation (9.41) we get

$$Z_o = -\frac{I_D R_d}{I_o} \tag{9.42}$$

To express I_D in terms of I_o, let us apply KCL at the node D. We get

$$I_o + I_d - I' - g_m V_{gs} = 0 \tag{9.43}$$

Let us find I' and V_{gs} in terms of I_d and I_o. Applying KVL to the path consisting of R_D, r_d and R_S we have

$$-I_d R_D - I' r_d - (I_d + I_o) R_S = 0$$

$$-I' r_d = I_d [R_D + R_S] + I_o R_S$$

$$I' = -I_d\left[\frac{R_D + R_S}{r_d}\right] - I_o\left[\frac{R_S}{r_d}\right] \tag{9.44}$$

Applying KVL to the path consisting of V_i, V_{gs} and R_S we get

$$-V_{gs} - R_S[I_d + I_o] = 0$$

$$V_{gs} = -I_d R_S - I_o R_S \tag{9.45}$$

Substituting Equations (9.44) and (9.45) in Equation (9.43) we get

$$I_o + I_d + I_d\left[\frac{R_D + R_S}{r_d}\right] + I_o\left[\frac{R_S}{r_d}\right] + g_m R_s I_d + g_m I_o R_S = 0$$

$$I_o\left[1 + \frac{R_S}{r_d} + g_m R_S\right] = -I_d\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right]$$

$$\frac{I_d}{I_o} = -\frac{1 + g_m R_S + \frac{R_S}{r_d}}{\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right]} \tag{9.46}$$

Substituting this relation in Equation (9.42) we get

$$Z_o = \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]} \tag{9.47}$$

Expression for Z_o Neglecting the Effect of r_d

Consider Equation (9.47)

If $r_d \geq 10\, R_D$

or $\frac{R_D}{r_d} \leq 0.1$

then $1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \approx 1 + g_m R_S + \frac{R_S}{r_d}$

Substituting this relation in Equation (9.47) we get

$$Z_o \approx R_D \tag{9.48}$$

Effect of Unbypassed R_S on Z_o

Observe from Equation (9.48) that, if $r_d \geq 10\ R_D$, unbypassing of R_S has no effect on Z_o. If $r_d < 10\ R_D$, Z_o is only slightly affected as given in Equation (9.47).

Important Characteristics of Common-source Configuration with Unbypassed R_S

Following are the important characteristics of common-source stage with unbypassed R_S.

- High input impedance
- Medium high output impedance
- Low voltage gain
- 180° phase shift betwen output and input voltages

Example 9.6

For the JFET amplifier shown below:

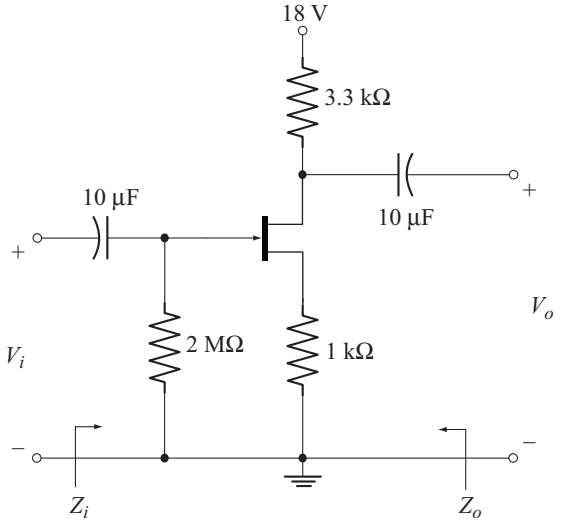
(a) Calculate Z_i and Z_o.

(b) Calculate A_V.

(c) Find V_o when $V_i = 50$ mV(p – p).

(d) Calculate Z_i, Z_o, A_V and V_o neglecting the effect of r_d.

(e) Compare the results.



$I_{DSS} = 8$ mA

$V_P = -6$ V

$I_{DSQ} = 2.5$ mA

$y_{os} = 25$ µS

Solution

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_P}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|}$$

$$= \frac{2(8\,\text{mA})}{6\,\text{V}} = 2.67\ \text{mS}$$

$$V_{GS_Q} = -I_{D_Q} R_S$$

$$= -(2.5\ \text{mA})\ (1\ \text{k}\Omega)$$

$$= -2.5\ \text{V}$$

Now $$g_m = 2.67\ \text{mS}\left[1 - \frac{-2.5\,\text{V}}{-6\,\text{V}}\right]$$

$$= 1.55\ \text{mS}$$

$$r_d = \frac{1}{y_{o_s}}$$

$$= \frac{1}{25\,\mu S} = 40\ \text{k}\Omega$$

(a) $$Z_i = R_G = 2\ \text{M}\Omega$$

$$Z_o = \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$$

$$1 + g_m R_S + \frac{R_S}{r_d} = 1 + (1.55\ \text{mS})\ (1\ \text{k}\Omega) + \frac{1\,\text{k}\Omega}{40\,\text{k}\Omega} = 2.575$$

$$1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} = 2.575 + \frac{3.3\,\text{k}\Omega}{40\,\text{k}\Omega} = 2.657$$

Now $$Z_o = \frac{(2.575)(3.3\,\text{k}\Omega)}{2.657} = 3.198\ \text{k}\Omega$$

(b) $$A_V = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

$$= -\frac{(1.55\,\text{mS})(3.3\,\text{k}\Omega)}{1 + (1.55\,\text{mS})(1\,\text{k}\Omega) + \left(\frac{3.3\,\text{k}\Omega + 1\,\text{k}\Omega}{40\,\text{k}\Omega}\right)}$$

$$= -1.924$$

(c) $$V_o = A_V V_i$$
$$= (-1.924)\ (50\ \text{mV})$$
$$= -96.2\ \text{mV}_{(p-p)}$$

(d) To find Z_i, Z_o, A_V and V_o neglecting the effect of r_d.

$$Z_i = R_G = 2\ \text{M}\Omega \quad \text{(Same as before)}$$
$$r_d = 40\ \text{k}\Omega \quad \text{and} \quad 10\ R_D = 33\ \text{k}\Omega$$

Since $r_d > 10\ R_D$, we can use Equation (9.48) to calculate Z_o.

$$Z_o = R_D = 3.3\ \text{k}\Omega$$

In order to use Equation (9.40) to find A_V, the required condition is

$$r_d \geq 10\ (R_D + R_S)$$
$$10\ (R_D + R_S) = 10\ (3.3\ \text{k}\Omega + 1\text{k}\Omega) = 43\ \text{k}\Omega$$
$$\text{But} \qquad r_d = 40\ \text{k}\Omega$$

Though the above condition is not satisfied, r_d is nearly equal to 10 $(R_D + R_S)$. Hence we can use Equation (9.40).

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$
$$= -\frac{(1.55\,\text{mS})(3.3\,\text{k}\Omega)}{1 + (1.55\,\text{mS})(1\,\text{k}\Omega)} = -2$$

The results are tabulated in the following table

Parameter	*Considering the effect of r_d*	*Neglecting the effect of r_d*
Z_i	2 MΩ	2 MΩ
Z_o	3.198 kΩ	3.3 kΩ
A_V	– 1.924	– 2

Observe that, the results are almost consistent since the approximating conditions are satisfied.

◆ 9.12 JFET COMMON-SOURCE AMPLIFIER USING VOLTAGE DIVIDER CONFIGURATION

Figure 9.18 shows the circuit of JFET common-source amplifier using voltage divider configuration.

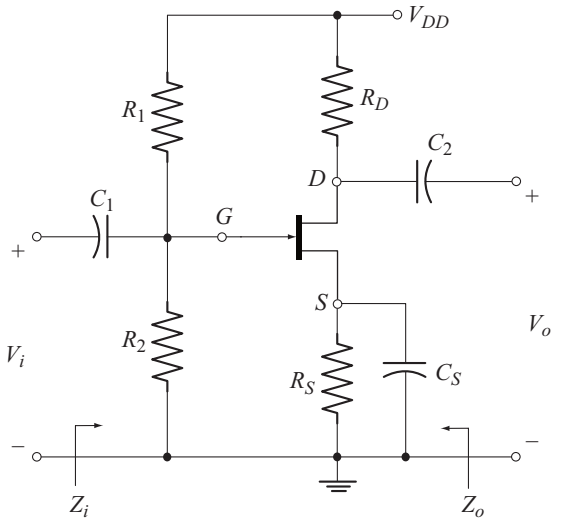


Fig. 9.18 JFET common-source amplifier using voltage divider configuration

The ac equivalent circuit is drawn in Fig. 9.19 by reducing V_{DD} to zero and short circuiting the capacitors C_1, C_2 and C_S. Observe that, the top end of R_1 goes to ground. As a result R_1 and R_2 will come in parallel between gate and the source.

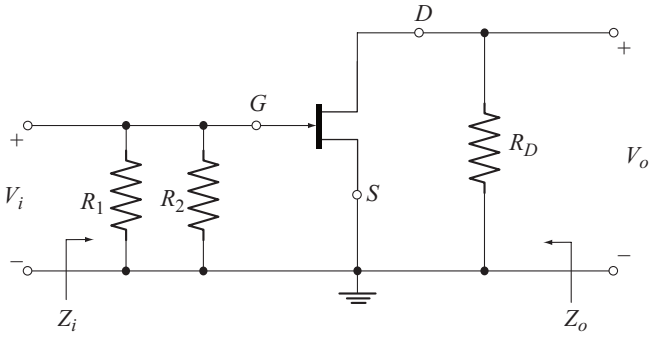


Fig. 9.19 Ac equivalent Circuit of the amplifier of Fig. 9.18

The ac equivalent circuit is redrawn in Fig. 9.20 by replacing JFET with its small signal ac model.

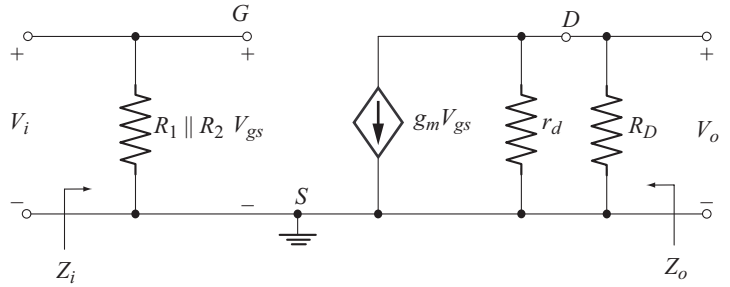


Fig. 9.20 Ac equivalent circuit redrawn using small-signal ac model of JFET

Note that the ac equivalent circuit of Fig. 9.20 is exactly the same as that of JFET amplifier using fixed bias configuration, shown in Fig. 9.10. Hence the results derived in section 9.9 can be readily applied to this circuit. The only exception is that, R_G should be replaced by $R_1 \parallel R_2$. Let us rewrite the results for reference.

When the effect of r_d is included

From Equations (9.18), (9.19) and (9.23) we have

$$Z_i = R_1 \parallel R_2 \tag{9.49}$$

$$Z_o = r_d \parallel R_D \tag{9.50}$$

$$A_V = -g_m [r_d \parallel R_D] \tag{9.51}$$

When the effect of r_d is neglected [For $r_d \geq 10\ R_D$]

From Equations (9.24) and (9.25) we have

$$Z_o \approx R_D \tag{9.52}$$

$$A_V \approx -g_m R_D \tag{9.53}$$

$$Z_i = R_1 \parallel R_2 \tag{9.54}$$

◆ 9.13 JFET COMMON-SOURCE AMPLIFIER USING VOLTAGE DIVIDER CONFIGURATION, WITH UNBYPASSED R_S

Figure 9.21 shows the circuit of JFET common-source amplifier using voltage divider configuration, with unbypassed R_S.

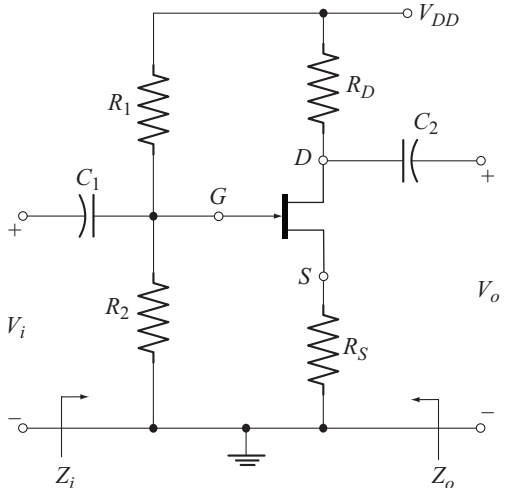


Fig. 9.21 JFET Voltage-divider configuration with unbypassed R_S

The ac equivalent circuit is drawn in Fig. 9.22 by reducing V_{DD} to zero, short circuiting capacitors C_1 and C_2 and replacing JFET with its small signal ac model.

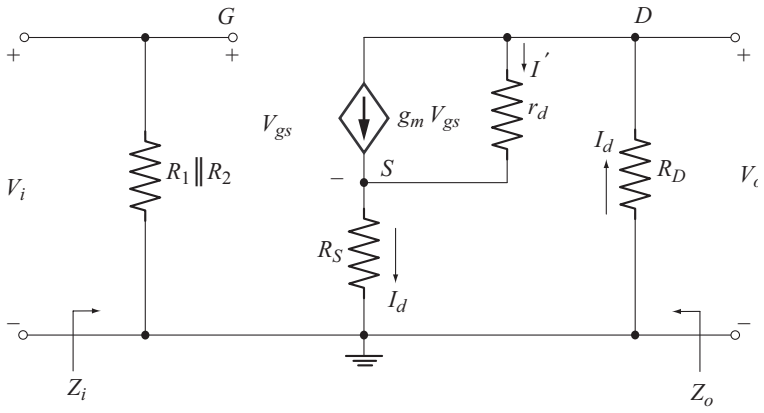


Fig. 9.22 Ac equivalent circuit of the JFET amplifier of Fig. 9.21

The ac equivalent circuit of Fig. 9.22 is exactly the same as that of JFET self bias configuration with unbypassed R_S, shown in Fig 9.16. Hence the results derived in section 9.11 can be readily applied to this circuit. The only exception is that, R_G should be replaced by $R_1 \| R_2$. Let us recall the results for reference.

When the effect of r_d is included

From Equations (9.31), (9.39) and (9.47) we have

$$Z_i = R_1 \| R_2 \tag{9.55}$$

$$A_V = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} \tag{9.56}$$

$$Z_o = \frac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]} \tag{9.57}$$

When the effect of r_d is neglected

Form Equations (9.40) and (9.48) we have

$$A_V = -\frac{g_m R_D}{1 + g_m R_S} \quad [\text{when } r_d \geq 10\,[R_D + R_S]] \tag{9.58}$$

$$Z_o = R_D \quad [\text{when } r_d \geq 10\, R_D] \tag{9.59}$$

$$Z_i = R_1 \| R_2 \tag{9.60}$$

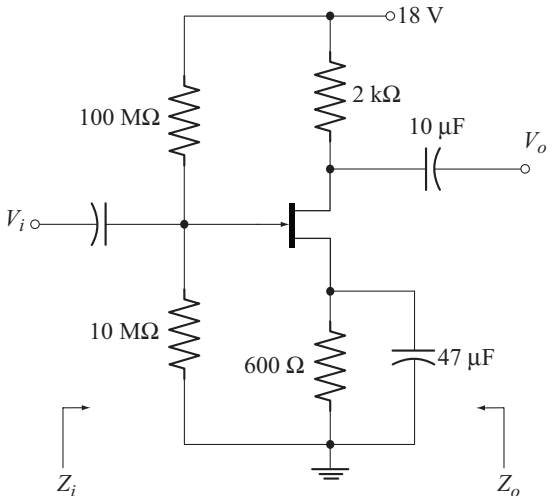
Example 9.7

For the JFET amplifier shown below:

(a) Calculate Z_i and Z_o

(b) Calculate A_V

(c) Find V_o if $V_i = 25$ mV (rms)



$I_{DSS} = 12$ mA

$V_P = -3$ V

$y_{os} = 10$ μS

$V_{GSQ} = -1$ V

Solution

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_P}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|}$$

$$= \frac{2(12\,\text{mA})}{3\,\text{V}} = 8\ \text{mS}$$

$$g_m = 8\ \text{mS}\left[1 - \frac{-1\,\text{V}}{-3\,\text{V}}\right] = 5.33\ \text{mS}$$

$$r_d = \frac{1}{y_{o_s}} = \frac{1}{10\,\mu\text{S}} = 100\ \text{k}\Omega$$

(a) $$Z_i = R_1 \| R_2 = 100\ \text{M}\Omega \| 10\ \text{M}\Omega = 9.09\ \text{M}\Omega$$

$$Z_o = r_d \| R_D = 100\ \text{k}\Omega \| 2\ \text{k}\Omega = 1.96\ \text{k}\Omega$$

(b) $$A_V = -g_m[r_d \| R_D]$$

$$= -[5.33\ \text{mS}]\,[1.96\ \text{k}\Omega] = -10.44$$

(c) $V_o = A_V V_i$

$= [-10.44]\,[25\text{ mV}] = -0.261\text{ V (rms)}$

Example 9.8

Repeat example 9.7 with source bypass capacitor C_S removed and compare the results.

Solution

$g_m = 5.33\text{ mS}$, $r_d = 100\text{ k}\Omega$ } As calculated in example 9.7

(a) $Z_i = R_1 \parallel R_2 = 9.09\text{ k}\Omega$

$10\,R_D = 10\,(2\text{ k}\Omega) = 20\text{ k}\Omega$

Note that $r_d > 10\,R_D$

$\therefore\quad Z_o = R_D$

$Z_o = 2\text{ k}\Omega$

(b) $10\,(R_S + R_D) = 10\,(600\ \Omega + 2\text{ k}\Omega) = 26\text{ k}\Omega$

Note that $r_d > 10\,(R_S + R_D)$

$\therefore\quad A_V = -\dfrac{g_m R_D}{1 + g_m R_S}$

$= -\dfrac{(5.33\text{ mS})(2\text{ kW})}{1 + (5.33\text{ mS})(600\text{ W})}$

$= -2.53$

(c) $V_o = A_V V_i$

$= (-2.53)\,(25\text{ mV}) = -63.25\text{ mV (rms)}$

The results of examples 9.7 and 9.8 are compared in the following table.

Parameter	*With bypassed R_S*	*With unbypassed R_S*	*Remarks*
Z_i	9.09 kΩ	9.09 kΩ	Not affected
Z_o	1.96 kΩ	2 kΩ	Slightly affected
A_V	– 10.44	– 2.53	Considerable reduction in voltage gain

Inference: Unbypassing of R_S in common-source configuration results in considerable reduction in voltage gain.

Example 9.9

Repeat example 9.8 taking $r_d = 20\ \text{k}\Omega$ keeping all other data remain unchanged.

Solution

$$g_m = 5.33\ \text{mS} \quad \text{[as given in example 9.9]}$$

$$r_d = 20\ \text{k}\Omega$$

(a) $$Z_i = R_1 \parallel R_2 = 9.09\ \text{k}\Omega$$

$$10\,R_D = (10)\,(2\ \text{k}\Omega) = 20\ \text{k}\Omega$$

The condition, $r_d \geq 10\,R_D$ is satisfied

$$\therefore \quad Z_o = R_D = 2\ \text{k}\Omega$$

(b) $$10\,(R_S + R_D) = 10\,(600\ \Omega + 2\ \text{k}\Omega) = 26\ \text{k}\Omega$$

Note that, $$r_d < 10\,(R_S + R_D)$$

$$\therefore \quad A_V = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

$$= -\frac{(5.33\ \text{mS})(2\text{k}\Omega)}{1 + (5.33\,\text{mS})(600\,\Omega) + \dfrac{2.6\,\text{k}\Omega}{20\,\text{k}\Omega}} = -2.46$$

◆ 9.14 JFET SOURCE-FOLLOWER [COMMON-DRAIN CONFIGURATION]

Figure 9.23 shows the circuit of JFET source-follower configuration. This circuit is analogous to BJT emitter-follower configuration.

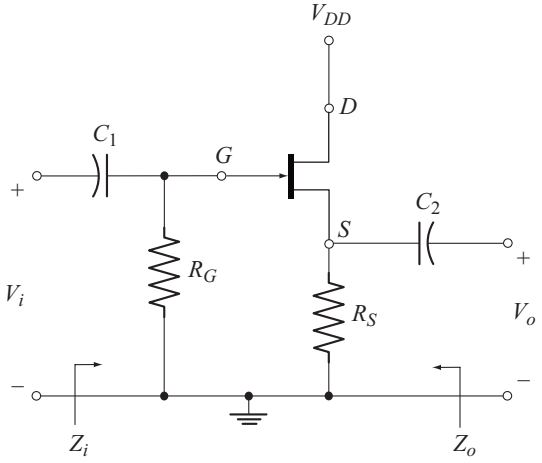


Fig. 9.23 JFET source-follower configuration

The ac equivalent circuit is drawn in Fig. 9.24, by reducing V_{DD} to zero and replacing C_1 and C_2 by their short circuit equivalents.

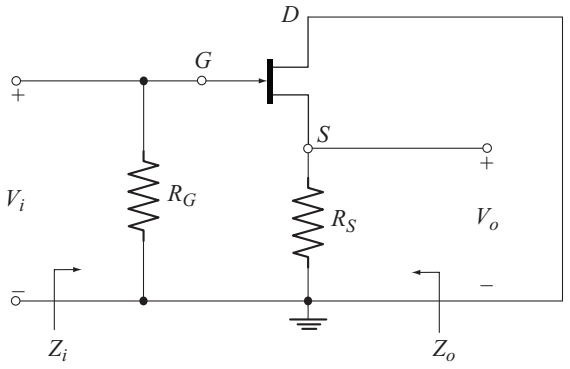


Fig. 9.24 *AC equivalent Circuit of JFET source-follower of Fig. 9.23*

Observe from Fig. 9.24 that, the ac input signal V_i, is applied between gate and ground (drain) and the ac output signal V_o, is taken between source and ground (drain). Since the drain terminal is common to input and output signals, the circuit is called common drain configuration.

The circuit has a voltage gain of approximately unity. Therefore $V_o \approx V_i$. Note that the output voltage (source voltage) follows the input voltage (gate voltage). Hence this circuit is also called the source-follower.

The ac equivalent circuit is redrawn in Fig. 9.25 using the JFET small-signal ac model.

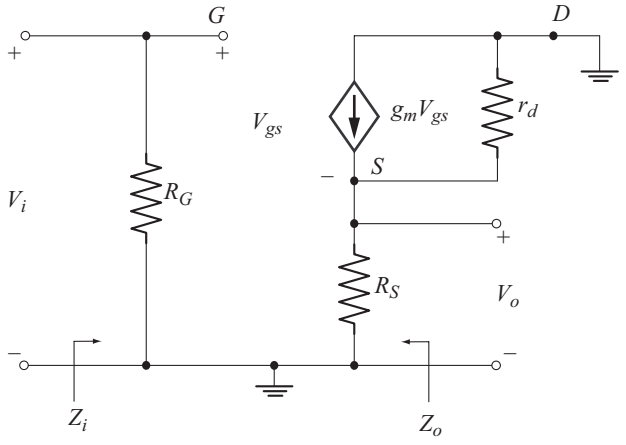


Fig. 9.25 *Ac equivalent circuit of source-follower using JFET small-signal ac model*

The ac equivalent circuit of Fig. 9.25 is redrawn in Fig. 9.26 for the convenience of analysis. This Circuit is written based on the following details available in the circuit of Fig. 9.25.

- The current $g_m V_{gs}$ flows from drain to source.
- Both r_d and R_S appear between source and drain terminals.

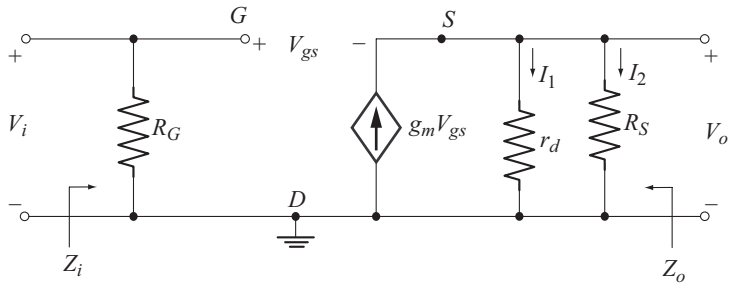


Fig. 9.26 Ac equivalent circuit of Fig. 9.25 redrawn

Input Impedance **[Z_i]**

From the input circuit of Fig. 9.26, we have

$$Z_i = R_G \tag{9.61}$$

Voltage Gain **[A_V]**

Applying KCL at the source node of Fig. 9.26 we have

$$g_m V_{gs} = \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

$$g_m V_{gs} = V_o \left[\frac{1}{r_d} + \frac{1}{R_S}\right]$$

$$g_m V_{gs} = V_o \left[\frac{R_S + r_d}{R_S\ r_d}\right]$$

$$V_o = g_m V_{gs} \left[\frac{R_S\ r_d}{R_S + r_d}\right]$$

or
$$V_o = g_m V_{gs} [r_d \,||\, R_S] \tag{9.62}$$

Applying KVL to the path consisting of V_i, V_{gs} and V_o we get

$$V_i - V_{gs} - V_o = 0 \tag{9.63}$$

or
$$V_{gs} = V_i - V_o \tag{9.64}$$

Using this relation in Equation (9.62) we get

$$V_o = g_m [V_i - V_o] [r_d \,||\, R_S]$$

$$V_o = g_m V_i [r_d \,||\, R_S] - g_m V_o [r_d \,||\, R_S]$$

$$V_o \left[1 + g_m [r_d \,||\, R_S]\right] = g_m V_i [r_d \,||\, R_S]$$

Now the voltage gain is

$$A_V = \frac{V_o}{V_i} = \frac{g_m [r_d \parallel R_S]}{1 + g_m [r_d \parallel R_S]} \tag{9.65}$$

Positive sign for A_V reveals that, V_o and V_i are in phase. Note that source-follower configuration is a non inverting amplifier.

Output Impedance [Z_o]

To find the output impedance, we apply the following steps to the circuit of Fig. 9.26:

- The input voltage V_i is set to zero. As a result R_G gets short Circuited
- A voltage source V_o is connected between the output terminals.

The resulting circuit is shown in Fig. 9.27.

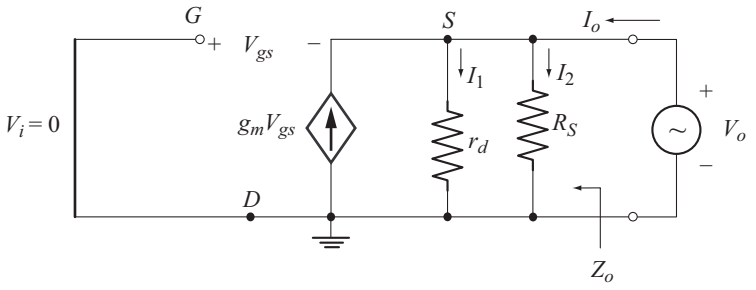


Fig. 9.27 Circuit to Find Z_o

From Fig. 9.27, the output impedance is given by

$$Z_o = \frac{V_o}{I_o} \tag{9.66}$$

Applying KCL at the node *S*, we have

$$I_o + g_m V_{gs} - I_1 - I_2 = 0 \tag{9.67}$$

$$I_1 = \frac{V_o}{r_d} \quad \text{and} \quad I_2 = \frac{V_o}{R_S}$$

Using these relations in Equation (9.67) we get

$$I_o + g_m V_{gs} - \frac{V_o}{r_d} - \frac{V_o}{R_S} = 0 \tag{9.68}$$

Let us eliminate V_{gs} by applying KVL to the path consisting of V_i, V_{gs} and V_o. We get

$$V_i - V_{gs} - V_o = 0$$

Since $V_i = 0$, we have

$$V_{gs} = -V_o \tag{9.69}$$

Using this relation in Equation (9.68) we get

$$I_o - g_m V_o - \frac{V_o}{r_d} - \frac{V_o}{R_S} = 0$$

$$I_o = V_o \left[g_m + \frac{1}{r_d} + \frac{1}{R_S} \right]$$

Now
$$Z_o = \frac{V_o}{I_o} = \frac{1}{g_m + \frac{1}{r_d} + \frac{1}{R_S}} \tag{9.70}$$

or
$$Z_o = \frac{1}{\frac{1}{\left[\frac{1}{g_m}\right]} + \frac{1}{r_d} + \frac{1}{R_S}} \tag{9.71}$$

In Equation (9.71), Z_o can be interpreted as the parallel combination of $\frac{1}{g_m}$, r_d and R_S.

$$\therefore \quad Z_o = \frac{1}{g_m} \| r_d \| R_S \tag{9.72}$$

Expression for A_v Neglecting the effect of r_d

For $r_d \geq 10\, R_S$

$$r_d \| R_S \approx R_S$$

From Equation (9.65) we get

$$A_V = \frac{V_o}{V_i} \approx \frac{g_m R_S}{1 + g_m R_S} \tag{9.73}$$

Further, if $g_m R_S \gg 1$, then from Equation (9.73) we get

$$A_V \approx \frac{g_m R_S}{g_m R_S} = 1$$

Note that the voltage gain under this condition is unity which justifies the name source-follower.

Expression for Z_o neglecting the effect of r_d

For $r_d \geq 10\, R_S$

$$r_d \| R_S \approx R_S$$

Using this condition in Equation (9.72) we get

$$Z_o \approx \frac{1}{g_m} \| R_S \tag{9.74}$$

Usually $g_m R_S \gg 1$ or $\dfrac{1}{g_m} \ll R_S$

As a result $Z_o \approx \dfrac{1}{g_m}$

Observe that source-follower has low output impedance relative to that of common-source and common-gate configurations.

Important characteristics of source-follower

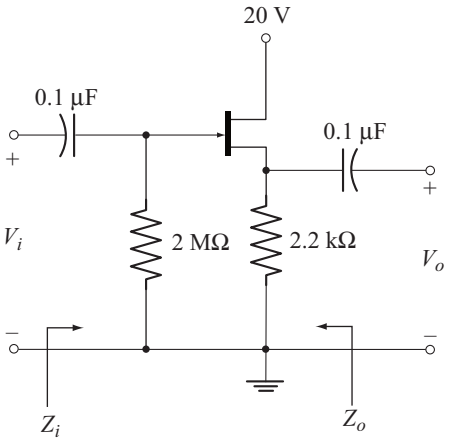
Following are the important characteristics of source-follower

- Approximately unity voltage gain
- High input impedance
- Relatively low output impedance
- Input and output voltages are in phase.

Example 9.10

For the JFET common drain configuration shown below:

(a) Calculate Z_i and Z_o
(b) Calculate A_V
(c) Find V_o if $V_i = 20$ mV(p – p)
(d) Find Z_i, Z_o, A_V and V_o neglecting the effect of r_d.



$I_{DSS} = 10$ mA
$V_P = -5$ V
$r_d = 40$ kΩ
$V_{GSQ} = -2.85$ V

Solution

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_P}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|} = \frac{2(10\text{ mA})}{5\text{ V}} = 4\text{ mS}$$

$$g_m = 4\text{ mS}\left[1 - \frac{-2.85\text{ V}}{-5\text{ V}}\right] = 1.72\text{ mS}$$

(a) $$Z_i = R_G = 2\ \text{M}\Omega$$

$$Z_o = \frac{1}{g_m} \parallel r_d \parallel R_S$$

$$\frac{1}{g_m} = \frac{1}{1.72\ \text{mS}} = 581.39\ \Omega$$

$$Z_o = 581.39\Omega \parallel 40\ \text{k}\Omega \parallel 2.2\ \text{k}\Omega = 454.63\Omega$$

(b) $$A_V = \frac{g_m \left[r_d \parallel R_S\right]}{1 + g_m \left[r_d \parallel R_S\right]}$$

$$= \frac{\left[1.72\,\text{mS}\right]\left[40\,\text{k}\Omega \parallel 2.2\,\text{k}\Omega\right]}{1 + \left[1.72\,\text{mS}\right]\left[40\,\text{k}\Omega \parallel 2.2\,\text{k}\Omega\right]} = 0.7818$$

(c) $$V_o = A_V V_i = [0.7818]\ [20\ \text{mV}] = 15.636\ \text{mV(p – p)}$$

(d) $$r_d = 40\ \text{k}\Omega \quad \text{and} \quad 10\ R_S = 22\ \text{k}\Omega$$

Since $r_d > 10\ R_S$, we can neglect the effect of r_d.

$$Z_i = 2\ \text{M}\Omega$$

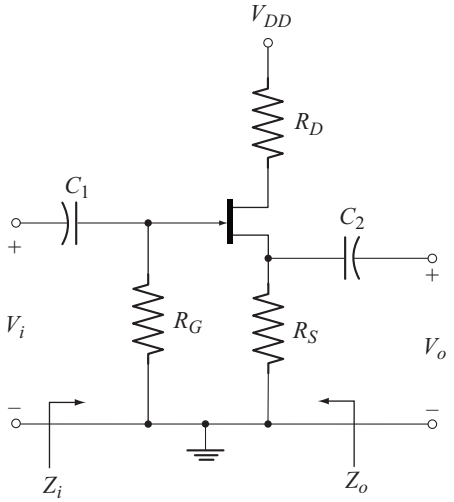
$$Z_o = \frac{1}{g_m} \parallel R_S = 581.39\ \Omega \parallel 2.2\ \text{k}\Omega = 459.86\ \Omega$$

$$A_V = \frac{g_m R_S}{1 + g_m R_S} = \frac{\left(1.72\,\text{mS}\right)\left(2.2\,\text{k}\Omega\right)}{1 + \left(1.72\,\text{mS}\right)\left(2.2\,\text{k}\Omega\right)} = 0.79$$

$$V_o = A_V V_i = (0.79)\ (20\ \text{mV}) = 15.8\ \text{mV(p – p)}$$

Example 9.11

For the source-follower with the drain circuit resistor R_D shown below, derive the expressions for Z_i, A_V and Z_o.



Solution

In the ac equivalent circuit, R_D comes between drain and ground. The ac equivalent circuit is drawn in Fig (A), using the circuit of Fig. 9.25.

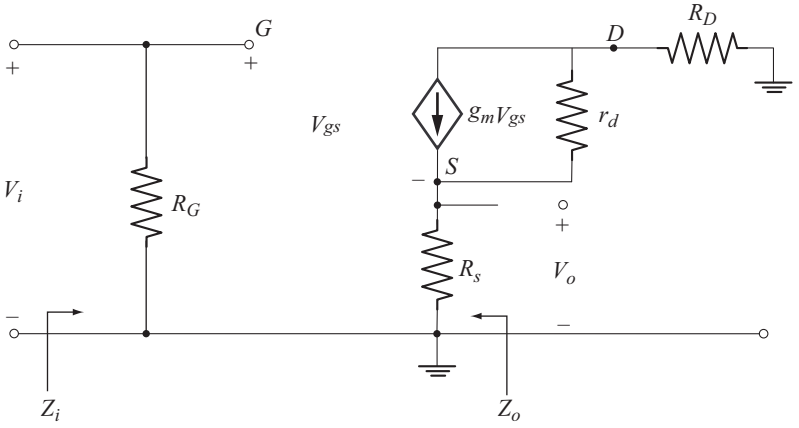
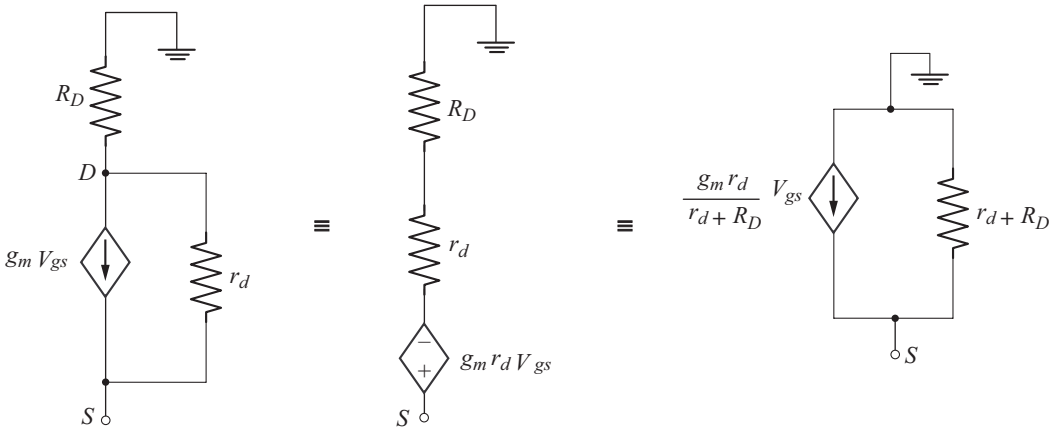


Fig. (A)

A part of the output circuit is shown in Fig. (B).



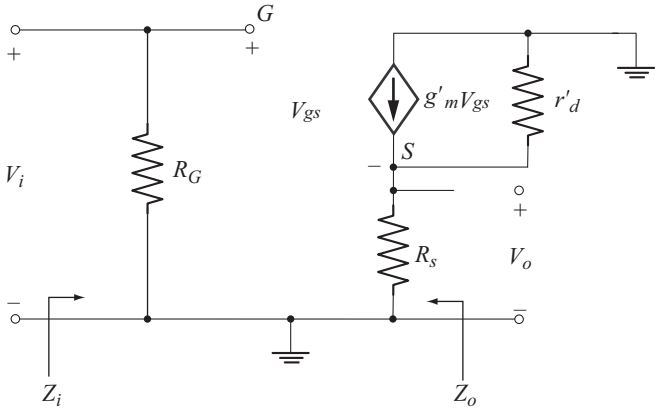
(B) (C) (D)

The current source $g_m V_{gs}$ in parallel with r_d in Fig. B is converted into its equivalent voltage source as shown Fig. (C). The voltage source is converted back into its equivalent current source in Fig. (D).

Let $$g'_m = \frac{g_m r_d}{r_d + R_D} \quad \text{(A)}$$

and $$r'_d = r_d + R_D \quad \text{(B)}$$

The ac equivalent circuit is redrawn in Fig. (E) after substituting the circuit of Fig (D) in Fig. (A).



(E)

Fig. (E)

The circuit of Fig. (E) has the same format as that of Fig. 9.25. Proceeding on the same lines given in section 9.14 we can arrive at the following results.

$$Z_i = R_G \tag{C}$$

$$A_V = \frac{V_o}{V_i} = \frac{g'_m \left[r'_d \parallel R_S\right]}{1 + g'_m \left[r'_d \parallel R_S\right]} \tag{D}$$

$$Z_o = \frac{1}{g'_m} \parallel r'_d \parallel R_S \tag{E}$$

Example 9.12

The following data are available for the circuit of example 9.11:

$V_{DD} = 20$ V $\quad R_D = 3.3$ kΩ $\quad R_G = 12$ MΩ
$R_S = 3.3$ kΩ $\quad I_{DSS} = 6$ mA $\quad V_p = -6$ V
$r_d = 30$ kΩ $\quad V_{GS_Q} = -3.8$ V

Calculate the values of Z_i, A_V and Z_o.

Solution

$$Z_i = R_G = 12 \text{ MΩ}$$

$$r'_d = r_d + R_D = 30 \text{ kΩ} + 3.3 \text{ kΩ} = 33.3 \text{ kΩ}$$

$$g'_m = \frac{g_m \, r_d}{r_d + R_D}$$

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$g_m = \frac{2\,I_{DSS}}{|V_P|} = \frac{2\ (6\ \text{mA})}{6\ \text{V}} = 2\ \text{mS}$$

$$g_{m_o} = 2\ \text{mS}\left[1 - \frac{-3.8\,\text{V}}{-6\,\text{V}}\right] = 0.733\ \text{mS}$$

Now
$$g'_m = \frac{[0.733\,\text{mS}][30\,\text{k}\Omega]}{[30\,\text{k}\Omega + 3.3\,\text{k}\Omega]} = 0.66\ \text{mS}$$

$$A_V = \frac{g'_m\,[r'_d \parallel R_S]}{1 + g'_m\,[r'_d \parallel R_S]}$$

$$= \frac{0.66\,\text{mS}\,[33.3\,\text{k}\Omega \parallel 3.3\,\text{k}\Omega]}{1 + 0.66\,\text{mS}\,[33.3\,\text{k}\Omega \parallel 3.3\,\text{k}\Omega]}$$

$$= 0.66$$

$$Z_o = \frac{1}{g'_m} \parallel r'_d \parallel R_S$$

$$\frac{1}{g'_m} = \frac{1}{0.66\,\text{mS}} = 1.515\ \text{k}\Omega$$

$\therefore$
$$Z_o = 1.515\ \text{k}\Omega \parallel 33.3\ \text{k}\Omega \parallel 3.3\ \text{k}\Omega$$

$$= 1\ \text{k}\Omega$$

◆ 9.15 JFET COMMON-GATE CONFIGURATION

JFET common-gate configuration is analogous to the BJT common-base configuration. Figure 9.28 shows the circuit of JFET common-gate configuration. An alternate representation of this circuit is also shown in Fig. 9.29.

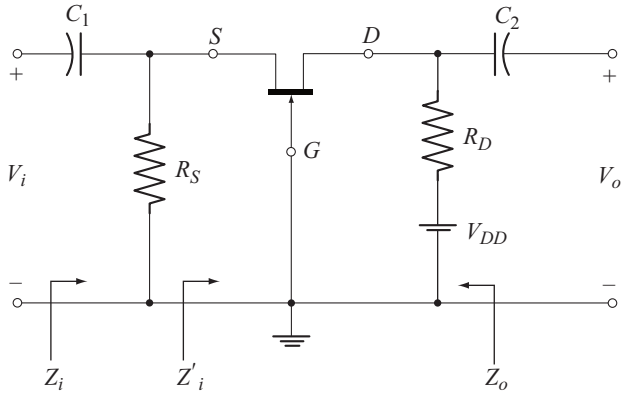


Fig. 9.28 JFET common-gate configuration

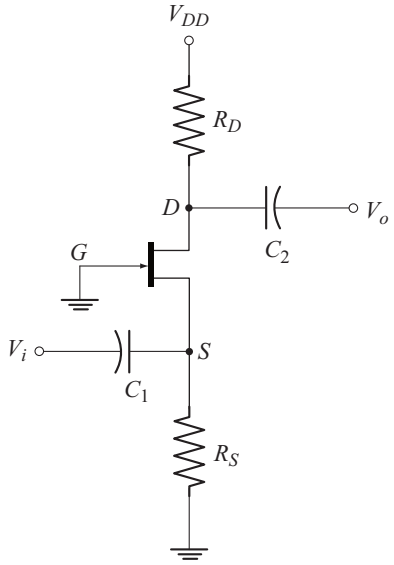


Fig. 9.29 Alternate representation of the circuit of Fig. 9.28

The ac equivalent circuit of Fig. 9.28 is drawn in Fig. 9.30 by replacing C_1 and C_2 with their short circuit equivalents and reducing V_{DD} to zero.

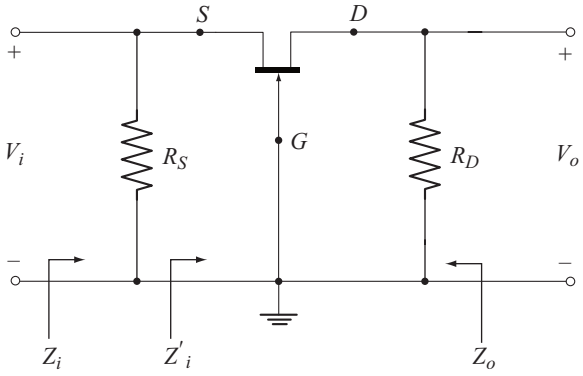


Fig. 9.30 Ac equivalent circuit of common-gate configuration

Observe form Fig. 9.30 that, the gate terminal is common for measuring both V_o and V_i. Hence the name common-gate configuration.

The ac equivalent is redrawn in Fig. 9.31 by replacing JFET with its small-signal ac model. Let us make the following important observations from the circuit of Fig. 9.31.

- R_S appears between source and gate. As a result, the open circuit condition between gate and source has been obviously lost.
- R_D appears between drain and gate.
- The current source $g_m V_{gs}$ and the FET output resistance r_d, will both appear between the drain and source terminals. The direction of $g_m V_{gs}$ is from drain to source, as usual.

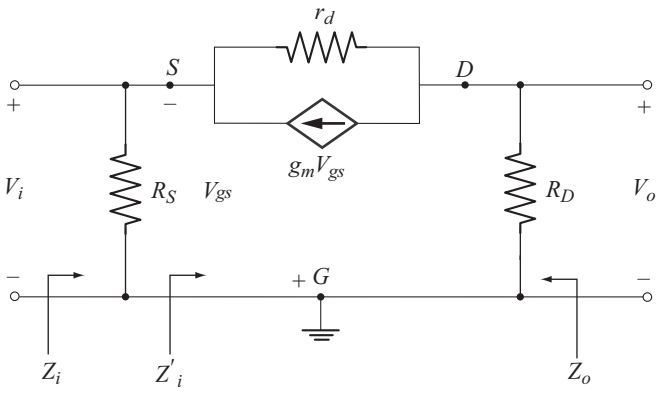


Fig. 9.31 AC equivalent circuit using JFET small signal model

Input Impedance [Z_i]

Form Fig. 9.31, the input impedance, Z_i is given by the parallel combination of R_S and Z'_i.

$$\text{i.e.,} \qquad Z_i = R_S \parallel Z'_i \tag{9.75}$$

where Z'_i is the impedance seen looking into source and gate terminals, excluding R_S.

To find Z'_i

The circuit between source and gate of Fig. 9.31 omitting R_S is redrawn in the convenient form in Fig. 9.32, to find Z'_i.

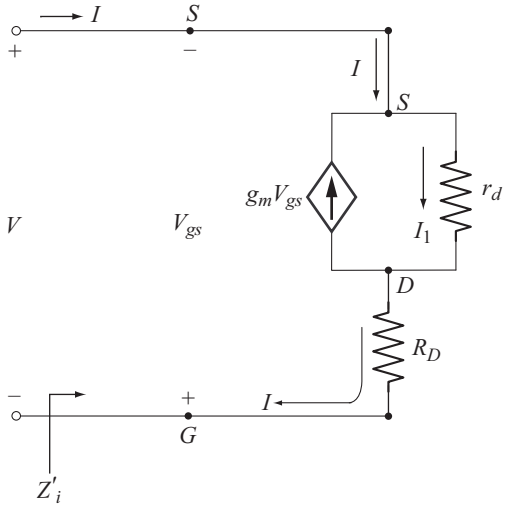


Fig. 9.32 Circuit to find Z_i'

Form Fig. 9.32, we find that

$$Z'_i = \frac{V}{I} \tag{9.76}$$

$$\text{Also} \qquad V = -V_{gs} \tag{9.77}$$

Applying KCL at the node S, we have

$$I + g_m V_{gs} = I_1 \tag{9.78}$$

Substituting Equation (9.77) in (9.78), we get

$$I - g_m V = I_1 \tag{9.79}$$

To express I_1 interms of V and I, let us apply KVL to the path consisting of V, r_d and R_D. We get

$$V - I_1 r_d - I R_D = 0$$

$$I_1 = \frac{V}{r_d} - \frac{R_D}{r_d} I \tag{9.80}$$

Using Equation (9.80) in Equation (9.79), we get

$$I - g_m V = \frac{V}{r_d} - \frac{R_D}{r_d} I$$

$$I\left[1 + \frac{R_D}{r_d}\right] = V\left[g_m + \frac{1}{r_d}\right]$$

$$Z_i' = \frac{V}{I} = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]} \tag{9.81}$$

$$\text{or} \qquad Z_i' = \frac{V}{I} = \frac{r_d + R_D}{1 + g_m r_d} \tag{9.82}$$

Using this relation in Equation (9.75), we get

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] \tag{9.83}$$

Expression for Voltage Gain [A_v]

$$A_V = \frac{V_o}{V_i} \tag{9.84}$$

From Fig. 9.31 we have

$$V_i = -V_{gs} \tag{9.85}$$

Combining Equations (9.77) and (9.85) we get

$$V_i = V \tag{9.86}$$

Observe from Fig. 9.31 that, V_o is measured across R_D connected between drain and ground i.e., V_o is the voltage across R_D.

From Fig. 9.32,

$$V_o = I R_D \tag{9.87}$$

From Equation (9.81), we get

$$I = \frac{V\left[g_m + \frac{1}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} \tag{9.88}$$

Using this relation in Equation (9.87), we get

$$V_o = \frac{V\left[g_m + \frac{1}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} . R_D$$

Substuting for V from Equation (9.86), we get

$$V_o = \frac{V_i\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]}$$

Now

$$A_V = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} \tag{9.89}$$

The positive sign for A_V reveals that V_o and V_i are inphase. Observe that, common gate configuration is a noninverting amplifier.

Expression for Output Impedance [Z_o]

To find Z_o, first we set V_i to zero. This results in the following changes in the circuit of Fig. 9.31.

- R_S gets short circuited
- $V_{gs} = - V_i = 0$

$\Rightarrow \quad g_m V_{gs} = 0$

Current source gets open circuited.
The resulting circuit is shown in Fig. 9.33.

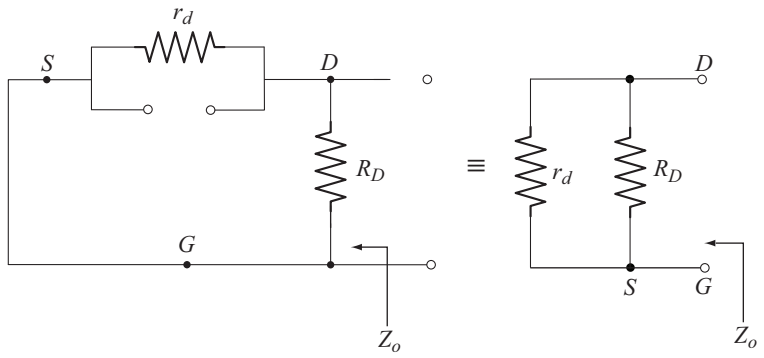


Fig. 9.33 Circuit to Find Z_o

From Fig. 9.33 we find that

$$Z_o = r_d \parallel R_D \tag{9.90}$$

Expressions for Z_i, A_V and Z_o neglecting the effect of r_d

For $r_d \geq 10\ R_D$

Consider Equation (9.81).

$$\text{Since} \quad \frac{R_D}{r_d} \leq 0.1$$

$$\therefore \quad 1 + \frac{R_D}{r_d} \approx 1$$

$$\text{Also} \quad \frac{1}{r_d} \ll g_m \quad [\text{Since } r_d \text{ is large}]$$

$$\text{As a result,} \quad g_m + \frac{1}{r_d} \approx g_m$$

Using these approximations in Equation (9.81), we get

$$Z_i' \approx \frac{1}{g_m} \tag{9.91}$$

Now

$$Z_i = R_S \parallel Z_i'$$

$$Z_i = R_S \parallel \frac{1}{g_m} \tag{9.92}$$

Now Consider Equation (9.89)

$$g_m R_D + \frac{R_D}{r_d} \approx g_m R_D$$

and

$$1 + \frac{R_D}{r_d} \approx 1$$

$$\therefore \quad A_V \approx g_m R_D \tag{9.93}$$

From Equation (9.90)

$$Z_o = r_d \,||\, R_D \approx R_D \tag{9.94}$$

Important characteristics of common gate configuration

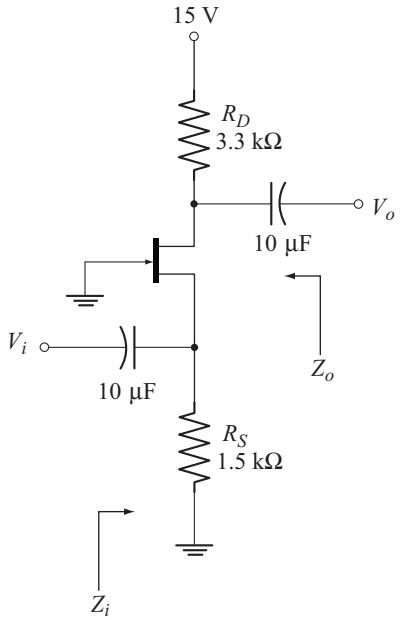
Based on the results derived, we can attribute the following characteristics to the common gate configuration.

- Relatively low input impedance $\left[Z_i \approx R_S \,||\, \frac{1}{g_m}\right]$
- Medium voltage gain $[A_V \approx g_m R_D]$
- Medium high output impedance $[Z_o \approx R_D]$
- Zero phase difference between input and output voltages [non inverting amplifier]

Example 9.13

For the JFET common-gate configuration shown below:

(a) Calculate Z_i and Z_o
(b) Find A_V
(c) Calculate V_o if $V_i = 1$ mV(p – p)
(d) Calculate Z_i, Z_o, A_V and V_o, neglecting the effect of r_d.



$I_{DSS} = 8$ mA
$V_P = -2.8$ V
$r_d = 40$ kΩ
$V_{GSQ} = -1.75$ V

Solution

$$g_m = g_{mo}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|} = \frac{(2)(8\text{ mA})}{2.8\text{ V}} = 5.71\text{ mS}$$

$$g_m = 5.71\text{ mS}\left[1 - \frac{-1.75\text{ V}}{-2.8\text{ V}}\right] = 2.14\text{ mS}.$$

(a)
$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$$
$$= 1.5\text{ k}\Omega \| \left[\frac{40\text{k}\Omega + 3.3\text{k}\Omega}{1 + (2.14\text{mS})(40\text{k}\Omega)}\right]$$
$$= 1.5\text{ k}\Omega \| 0.5\text{ k}\Omega = 375\Omega$$
$$Z_o = r_d \| R_D = 40\text{ k}\Omega \| 3.3\text{ k}\Omega = 3.04\text{ k}\Omega$$

(b)
$$A_V = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]}$$
$$= \frac{\left[(2.14\text{mS})(3.3\text{k}\Omega) + \frac{3.3\text{k}\Omega}{40\text{k}\Omega}\right]}{\left[1 + \frac{3.3\text{k}\Omega}{40\text{k}\Omega}\right]} = \frac{7.1445}{1.0825} = 6.6$$

(c)
$$V_o = A_V V_i = [6.6]\,[1\text{mV}] = 6.6\text{ mV(p – p)}$$

(d)
$$r_d = 40\text{ k}\Omega \quad \text{and} \quad 10\,R_D = 3.3\text{ k}\Omega$$

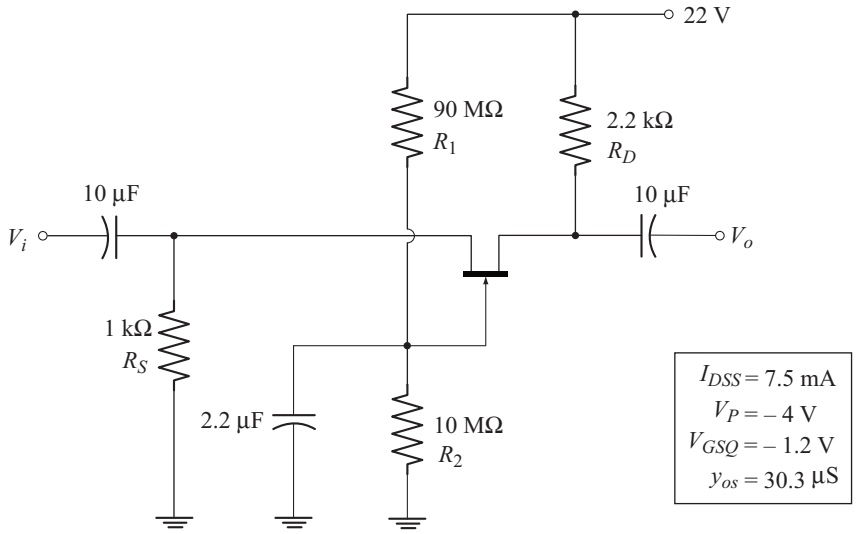
Since $r_d > 10\,R_D$, the effect of r_d can be neglected.

$$Z_i = R_S \| \frac{1}{g_m} = 1.5\text{ k}\Omega \| \frac{1}{2.14\text{mS}} = 356.12\Omega$$
$$Z_o = R_D = 3.3\text{ k}\Omega$$
$$A_V = g_m R_D = [2.14\text{ mS}]\,[3.3\text{ k}\Omega] = 7.06$$
$$V_o = A_V V_i = [7.06]\,[1\text{ mV}] = 7.06\text{ mV(p – p)}$$

Example 9.14

For the circuit shown below:

(a) Calculate Z_i and Z_o.
(b) Find A_V.
(c) Calculate V_o, if $V_i = 5$ mV (rms).
(d) Calculate Z_i, Z_o, A_V and V_o, neglecting the effect of r_d.



Solution

The given circuit is JFET common-gate configuration using voltage divider bias. The 22 µF capactior is used to create ground at the gate terminal for ac operation. As a result, the voltage divider resistors R_1 and R_2 will get shorted to ground.

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|} = \frac{(2)(7.5\,\text{mA})}{4\,\text{V}} = 3.75\ \text{mS}$$

$$g_m = 3.75\ \text{mS}\left[1 - \frac{-1.2\,\text{V}}{-4\,\text{V}}\right] = 2.625\ \text{mS}$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{30.3\,\mu\text{S}} = 33\ \text{k}\Omega$$

(a)
$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$$

$$= 1\ \text{k}\Omega \| \left[\frac{33\,\text{k}\Omega + 2.2\,\text{k}\Omega}{1 + (2.625\,\text{mS})(33\,\text{k}\Omega)}\right] = 286.58\ \Omega$$

$$Z_o = r_d \| R_D = 33\ \text{k}\Omega \| 2.2\ \text{k}\Omega = 2.06\ \text{k}\Omega$$

(b)
$$A_V = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]}$$

$$= \frac{\left[(2.625\,\text{mS})\ (2.2\,\text{k}\Omega) + \dfrac{2.2\,\text{k}\Omega}{33\,\text{k}\Omega}\right]}{\left[1 + \dfrac{2.2\,\text{k}\Omega}{33\,\text{k}\Omega}\right]} = 5.47$$

(c) $V_o = A_V V_i = [5.47]\ [5\ \text{mV}] = 27.35\ \text{mV (rms)}.$

(d) $r_d = 33\ \text{k}\Omega$ and $10\ R_D = (10)\ (2.2\ \text{k}\Omega) = 22\ \text{k}\Omega$

Since $r_d > 10\ R_D$, the effect of r_d can be neglected

$$Z_i = R_S \| \frac{1}{g_m} = 1\text{k}\Omega \| \frac{1}{2.625\,\text{mS}} = 275.86\Omega$$

$$Z_o = R_D = 2.2\ \text{k}\Omega$$

$$A_V = g_m R_D = (2.625\ \text{mS})\ (2.2\ \text{k}\Omega) = 5.775$$

$$V_o = A_V V_i = [5.775]\ [5\ \text{mV}] = 28.875\ \text{mV (rms)}$$

9.16 DEPLETION-TYPE MOSFETS [D-MOSFET]

MOSFET stands for metal oxide semiconductor field effect transistor. The name metal oxide is due to the fact that, the gate is made up of metal and a thin insulating silicon dioxide (SiO_2) layer separates the gate from the channel. Since the gate is electrically insulated from the channel, MOSFET has very high input impedance which is of the same order as that of JFET. As a result the gate current I_G is essentially zero for the dc-biased configurations.

The drain current and transconductance equations derived for JFET can be readily applied to D-MOSFET. These equations are reproduced below for reference.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS_Q}}{V_p}\right]^2 \tag{9.95}$$

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right] \tag{9.96}$$

where $$g_{m_o} = \frac{2I_{DSS}}{|V_p|} \tag{9.97}$$

In JFET, V_{GS_Q} can only be negative for *n* channel devices and positive for *p* channel devices. Hence g_m is always less than g_{m_o}. But for *D*-MOSFET, V_{GS_Q} can be of either polarily.

For instance, if V_{GS_Q} is negative for an *n* channel device, the device operates in the depletion mode. In depletion mode, $g_m < g_{m_o}$ and $I_D < I_{DSS}$ as seen from equations (9.95) and (9.96).

On the other hand, if V_{GS_Q} is positive, the device operates in the enhancement mode. In enhancement mode $g_m > g_{m_o}$ and $I_D > I_{DSS}$.

Small Signal Model of D-MOSFET

The small signal ac model of D-MOSFET is exactly the same as that of JFET. The range of r_d is same as that of JFET. The only difference is in the value of g_m. Figure 9.34 shows the circuit symbol and small signal ac model of D-MOSFET.

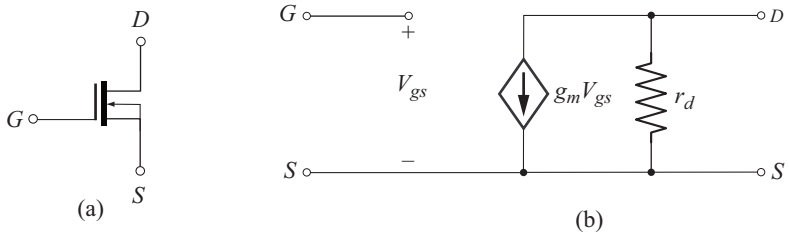


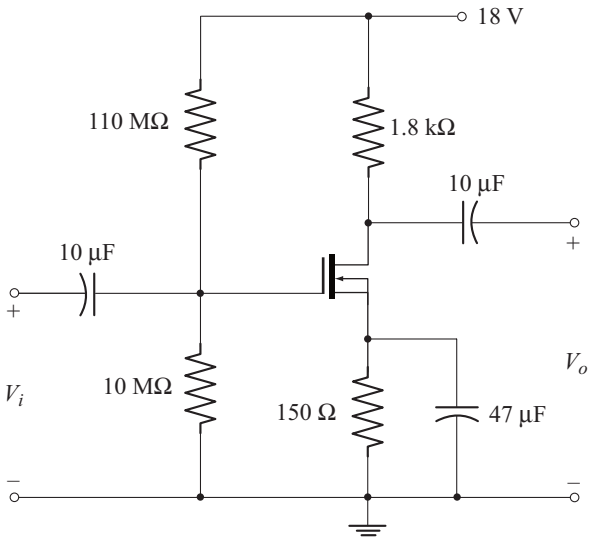
Fig. 9.34 (a) Circuit symbol of n channel D-MOSFET
(b) Small-signal ac model of D-MOSFET

It should be noted that the small signal ac model is same for both *n*-channel and p-channel D-MOSFETS. Also all the results derived for JFET configurations can be readily applied to the corresponding D-MOSFET configurations.

Example 9.15

For the D-MOSFET amplifier shown

(a) Calculate g_m and compare with g_{mo}
(b) Calculate r_d
(c) Draw the ac equivalent circuit
(d) Find Z_i and Z_o
(e) Calculate A_V
(f) Find V_o if $V_i = 2$ mV(p – p)



$I_{DSS} = 6$ mA
$V_P = -3$V
$V_{GSQ} = 0.35$ V
$y_{os} = 20$ µS

Solution

The given circuit is D-MOSFET common-source configuration using voltage divider bias. The results derived in section 9.12 for JFET configuration can be directly used for this circuit.

(a)
$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

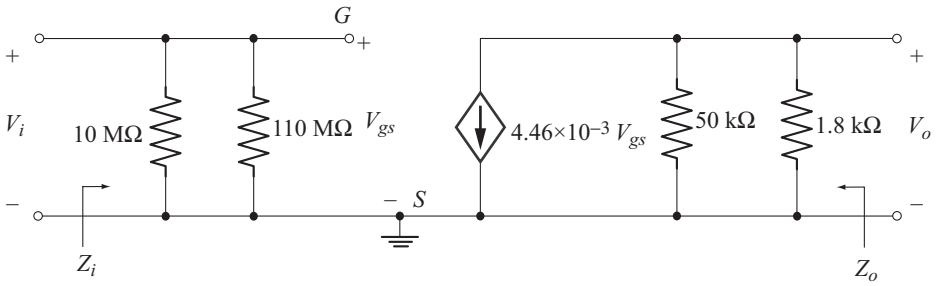
$$g_{m_o} = \frac{2I_{DSS}}{|V_p|} = \frac{(2)(6\,\text{mA})}{3\,\text{V}} = 4\ \text{mS}$$

$$g_m = 4\ \text{mS}\left[1 - \frac{0.35\,\text{V}}{-3\,\text{V}}\right] = 4.46\ \text{mS}$$

Note that, $g_m > g_{m_o}$ since V_{GS_Q} is positive.

(b)
$$r_d = \frac{1}{y_{os}} = \frac{1}{20\,\mu\text{S}} = 50\ \text{k}\Omega$$

(c) The ac equivalent circuit is shown below.



(d) From Equation (9.49),

$$Z_i = R_1 \parallel R_2$$
$$= 110\ \text{M}\Omega \parallel 10\ \text{M}\Omega = 9.16\ \text{M}\Omega$$

From Equation (9.50),

$$Z_o = r_d \parallel R_D = 50\ \text{k}\Omega \parallel 1.8\ \text{k}\Omega = 1.73\ \text{k}\Omega$$

(e) From Equation (9.51),

$$A_V = -g_m\,[r_d \parallel R_D]$$
$$= -[4.46\ \text{mS}]\,[50\ \text{k}\Omega \parallel 1.8\ \text{k}\Omega] = -7.71$$

(f)
$$V_o = A_V V_i = [-7.71]\,[2\ \text{mV}] = -15.42\ \text{mV(p-p)}$$

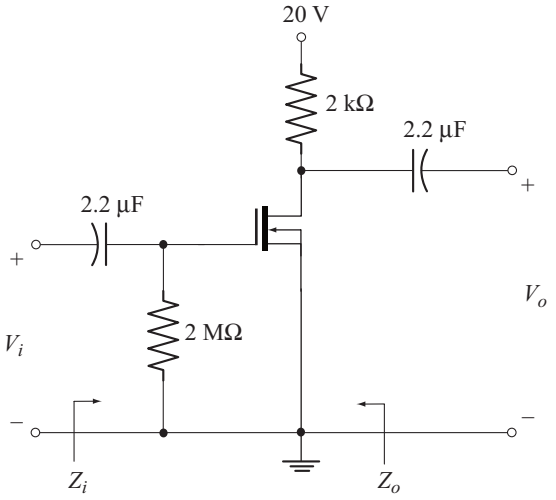
Example 9.16

For the D-MOSFET amplifier shown below

(a) Calculate Z_i and Z_o
(b) Find A_V
(c) Calculate V_o if $V_i = 50$ mV (rms)
(d) Find Z_i, Z_o, A_V and V_o neglecting the effect of r_d.

Solution

The given circuit is a D-MOSFET common source configuration with $V_{GS_Q} = 0$ V. For the solution, please refer Example 9.5.



$I_{DSS} = 5$ mA

$V_P = -6$ V

$y_{os} = 40$ µS

Example 9.17

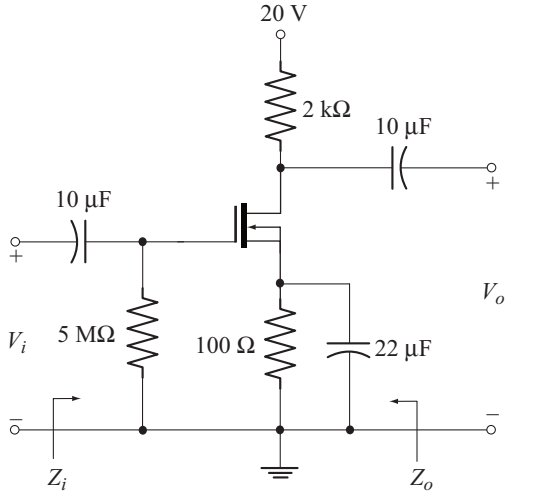
For the circuit shown below

(a) Calculate Z_i and Z_o

(b) Calculate A_V

(c) Find V_o if $V_i = 1$ mV (rms)

(d) Determine Z_i, Z_o, A_V and V_o neglecting the effect of r_d.



$I_{DSS} = 12$ mA

$V_P = -3.5$ V

$V_{GSQ} = -0.75$ V

$r_d = 50$ kΩ

Solution

The given circuit is D-MOSFET common-source configuration using self bias. The results derived in section 9.10 for JFET configuration can be readily applied to this circuit.

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|}$$

$$= \frac{2\,(12\,\text{mA})}{3.5\,\text{V}} = 6.85\ \text{mS}$$

$$g_m = 6.85\ \text{mS}\left[1 - \frac{-0.75\,\text{V}}{-3.5\,\text{V}}\right] = 5.38\ \text{mS}$$

(a) $Z_i = R_G = 5\ \text{M}\Omega$ [From Equation (9.26)]

$Z_o = r_d \,||\, R_D$ [From Equation (9.27)]

$= 50\ \text{k}\Omega \,||\, 2\ \text{k}\Omega = 1.92\ \text{k}\Omega$

(b) $A_V = -g_m\,[r_d \,||\, R_D]$ [From Equation (9.28)]

$= -[5.38\ \text{mS}]\,[1.92\ \text{k}\Omega]$

$= -10.33.$

(c) $V_o = A_V V_i$

$= [-10.33]\,[1\ \text{mV}]$

$= -10.33\ \text{mV(rms)}$

(d) $r_d = 50\ \text{k}\Omega$ and $10\,R_D = 20\ \text{k}\Omega$

Since $r_d > 10\,R_D$, the effect of r_d can be neglected.

$$Z_i = R_G = 5\ \text{M}\Omega$$

$$Z_o = R_D = 2\ \text{k}\Omega$$

$$A_V = -g_m R_D$$

$$= -[5.38\ \text{mS}]\,[2\ \text{k}\Omega] = -10.76$$

$$V_o = [-10.76]\,[1\ \text{mV}]$$

$$= -10.76\ \text{mV (rms)}$$

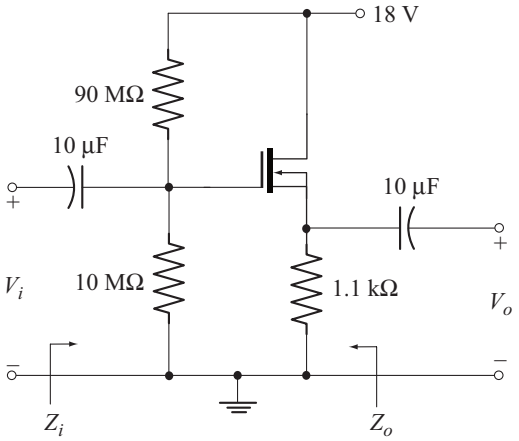
Example 9.18

For the amplifier shown below:

(a) Calculate Z_i and Z_o

(b) Calculate A_V

(c) Determine V_o if $V_i = 2$ mV (rms)



$I_{DSS} = 12$ mA

$V_P = -3$ V

$V_{GSQ} = -1.45$V

$r_d = 40$ kΩ

Solution

The given circuit is D-MOSFET source-follower configuration without R_D. The results derived in section 9.14 for JFET source-follower can be readily applied to this circuit.

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|}$$

$$= \frac{2(12\,\text{mA})}{3\,\text{V}} = 8\ \text{mS}$$

$$g_m = 8\ \text{mS}\left[1 - \frac{-1.45\,\text{V}}{-3\,\text{V}}\right] = 4.13\ \text{mS}$$

(a) $$Z_i = 90\ \text{M}\Omega \parallel 10\ \text{M}\Omega = 9\ \text{M}\Omega$$

$$Z_o = \frac{1}{g_m} \parallel r_d \parallel R_S \qquad \text{[From Equation (9.72)]}$$

$$= \frac{1}{4.13\,\text{mS}} \parallel 40\ \text{k}\Omega \parallel 1.1\ \text{k}\Omega = 197.46\Omega$$

(b) $$A_V = \frac{g_m[r_d \parallel R_S]}{1 + g_m[r_d \parallel R_S]} \qquad \text{[From Equation (9.65)]}$$

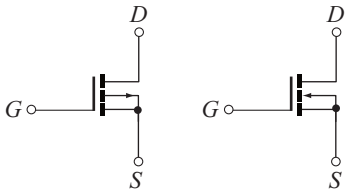
$$= \frac{[4.13\,\text{mS}][40\,\text{k}\Omega \parallel 1.1\,\text{k}\Omega]}{1 + [4.13\,\text{mS}][40\,\text{k}\Omega \parallel 1.1\,\text{k}\Omega]} = 0.815$$

(c) $$V_o = A_V V_i$$

$$= [0.815]\ [2\ \text{mV}] = 1.63\ \text{mV (rms)}$$

9.17 ENHANCEMENT-TYPE MOSFETS [E-MOSFET]

Figure 9.35 shows the circuit symbols of *n*-channel (*n* MOS) and *p*-channel (*p* MOS) E-MOSFETS. The E-MOSFET is fabricated to operate only in enhancement mode. Hence V_{GS_Q} can only be positive for *n*-channel device and negative for *p*-channel device.



(a) (b)

Fig. 9.35 (a) Circuit symbol of p MOS device
(b) Circuit symbol n MOS device

The drain current for E-MOSFET is given by the relation

$$I_D = k\,[V_{GS} - V_{GS\,(Th)}]^2 \tag{9.98}$$

$V_{GS(Th)}$ is the threshold voltage. It is important to note that, the drain current is zero for $V_{GS} < V_{GS(Th)}$ and it significantly increases for $V_{GS} \geq V_{GS(Th)}$. k is a constant which is specified on the data sheet for typical operating point.

9.18 EXPRESSION FOR TRANSCONDUCTANCE g_m

The transconductance is defined by

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\,\text{Point}} \tag{9.99}$$

Differentiating Equation (9.98) with respect to V_{GS}, we get

$$\frac{dI_D}{dV_{GS}} = 2\,k\,[V_{GS} - V_{GS(Th)}]$$

But

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\ \text{Point}}$$

$$\therefore \quad g_m = 2\,k\,[V_{GSQ} - V_{GS(Th)}] \tag{9.100}$$

9.19 SMALL SIGNAL AC MODEL OF E-MOSFET

The small signal ac model of E-MOSFET is shown in Fig. 9.36. Observe that, the format of the model is exactly identical to that of JFET.

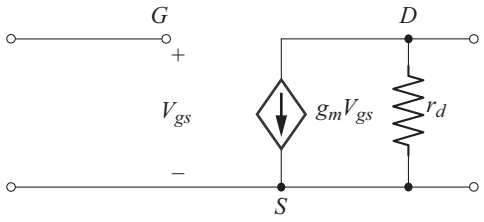


Fig. 9.36 Small Signal ac model of E-MOSFET

9.20 E-MOSFET DRAIN-FEEDBACK CONFIGURATION

Figure 9.37 shows the circuit of E-MOSFET common-source amplifer employing drain feedback. The resistor R_F provides ac negative feedback.

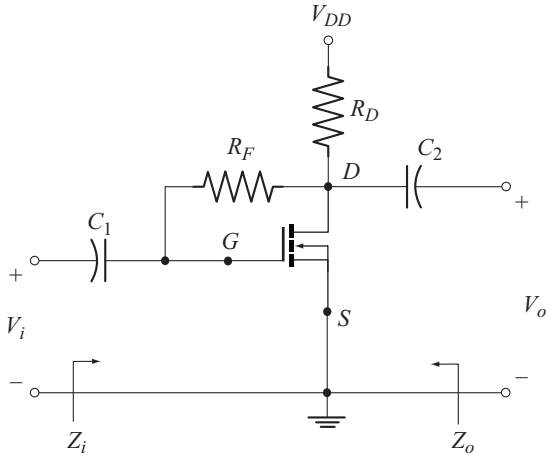


Fig 9.37 E – MOSFET drain-feedback configuration

The ac equivalent circuit is drawn in Fig. 9.38 by reducing V_{DD} to zero and replacing C_1 and C_2 with their short circuit equivalents.

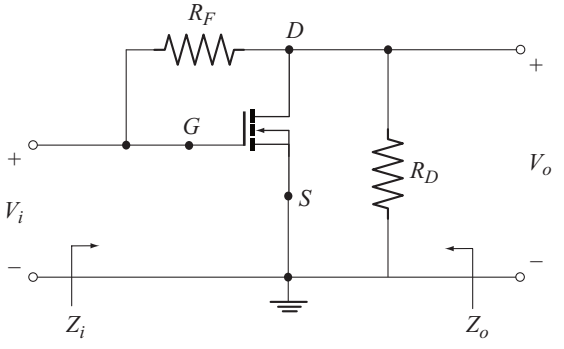


Fig 9.38 AC equivalent circuit of E–MOSFET drain–feedback configuration

The ac equivalent circuit is redrawn in Fig. 9.39 by replacing E–MOSFET with its small–signal ac model.

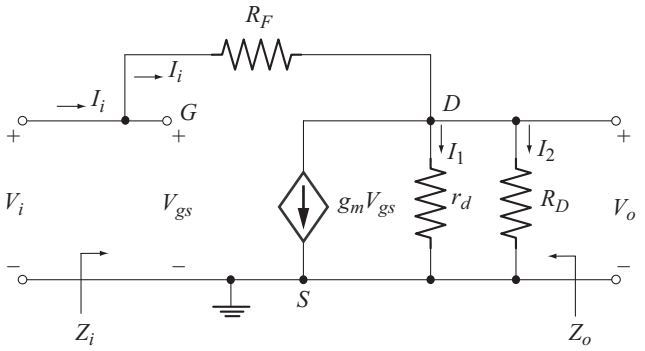


Fig 9.39 Ac equivalent circuit using small signal ac model of E-MOSFET

Due to open circuit between the gate and source terminals, the current into the gate terminal is zero. Hence I_i flows into R_F.

Expression for input impedance [Z_i]

Due to the connection between input and output nodes, the calculation Z_i is not straight forward. The input impedance is given by

$$Z_i = \frac{V_i}{I_i} \tag{9.101}$$

Applying KCL at the node D, we have

$$I_i = g_m V_{gs} + I_1 + I_2 \tag{9.102}$$

From the input circuit

$$V_{gs} = V_i \tag{9.103}$$

From the output circuit,

$$I_1 = \frac{V_o}{r_d} \quad \text{and} \quad I_2 = \frac{V_o}{R_D}$$

Now
$$I_1 + I_2 = \frac{V_o}{r_d} + \frac{V_o}{R_D}$$

$$= V_o \left[\frac{1}{r_d} + \frac{1}{R_D}\right]$$

$$= V_o \left[\frac{1}{R'_D}\right] \tag{9.104}$$

where
$$\frac{1}{R'_D} = \frac{1}{r_d} + \frac{1}{R_D}$$

$$\Rightarrow \qquad R'_D = \frac{r_d R_D}{r_d + R_D} = r_d \parallel R_D \tag{9.105}$$

Using Equations (9.103) and (9.104) in Equation (9.102), we get

$$I_i = g_m V_i + \frac{V_o}{R'_D} \tag{9.106}$$

But $$I_i = \frac{V_i - V_o}{R_F} \qquad [\text{current through } R_F]$$

$$\Rightarrow \qquad V_o = V_i - I_i R_F \tag{9.107}$$

Using Equation (9.107) in Equation (9.106), we have

$$I_i = g_m V_i + \frac{V_i - I_i R_F}{R'_D}$$

$$I_i \left[1 + \frac{R_F}{R'_D}\right] = V_i \left[g_m + \frac{1}{R'_D}\right]$$

Now $$Z_i = \frac{V_i}{I_i} = \frac{\left[1 + \dfrac{R_F}{R'_D}\right]}{\left[g_m + \dfrac{1}{R'_D}\right]}$$

or $$Z_i = \frac{R_F + R'_D}{1 + g_m R'_D} \tag{9.108}$$

or $$Z_i = \frac{R_F + [r_d \parallel R_D]}{1 + g_m [r_d \parallel R_D]} \tag{9.109}$$

Approximate expression for Z_i

Usually, $R_F >> r_d \parallel R_D$

$$\therefore \quad R_F + [r_d \parallel R_D] \approx R_F$$

Using this approximation in Equation (9.109) we get

$$Z_i \approx \frac{R_F}{1 + g_m [r_d \parallel R_D]}$$

Further, if $$r_d \geq 10\, R_D,$$

$$r_d \parallel R_D \approx R_D$$

Now we get

$$Z_i \approx \frac{R_F}{1+g_m R_D} \tag{9.110}$$

Expression for Voltage Gain [A_V]

From Equation (9.106) we have

$$I_i = g_m V_i + \frac{V_o}{R'_D} \tag{9.111}$$

Using $I_i = \frac{V_i - V_o}{R_F}$, we get

$$\frac{V_i - V_o}{R_F} = g_m V_i + \frac{V_o}{R'_D}$$

$$V_o \left[\frac{1}{R_F} + \frac{1}{R'_D}\right] = V_i \left[\frac{1}{R_F} - g_m\right]$$

$$A_V = \frac{V_o}{V_i} = \frac{\left[\frac{1}{R_F} - g_m\right]}{\left[\frac{1}{R_F} + \frac{1}{R'_D}\right]} \tag{9.112}$$

$$\frac{1}{R'_D} = \frac{1}{r_d} + \frac{1}{R_D}$$

$$\therefore \quad \frac{1}{R_F} + \frac{1}{R'_D} = \frac{1}{R_F} + \frac{1}{r_d} + \frac{1}{R_D}$$

$$\Rightarrow \quad \frac{1}{\frac{1}{R_F} + \frac{1}{R'_D}} = R_F \,||\, r_d \,||\, R_D \tag{9.113}$$

Using Equation (9.113) in Equation (9.112) we get

$$A_V = \left[\frac{1}{R_F} - g_m\right][R_F \,||\, r_d \,||\, R_D] \tag{9.114}$$

Usually $\frac{1}{R_F}$ is smaller than g_m. Hence A_V is negative. The negative sign reveals that, V_o and V_i are out of phase by 180°.

Approximate Expression for A_V

Typically $\frac{1}{R_F} \ll g_m$. As a result

$$\frac{1}{R_F} - g_m \approx -g_m$$

Also $R_F \gg r_d \,||\, R_D$

Hence $R_F \,||\, r_d \,||\, R_D \approx r_d \,||\, R_D$

Using these approximations in Equation (9.114) we get

$$A_V \approx -g_m [r_d \,||\, R_D]$$

If $r_d \geq 10\, R_D$, then $r_d \,||\, R_D \approx R_D$

Now we get $$A_V \approx -g_m R_D \tag{9.115}$$

Expression for Output Impedance [Z_o]

To find the output impedance, we reduce V_i to zero in the circuit of Fig 9.39. With $V_i = 0$

- Gate get shorted to source
- $g_m V_{gs} = 0$. Therefore the current $g_m V_{gs}$ represents an open circuit.

The resulting circuit is shown in Fig 9.40.

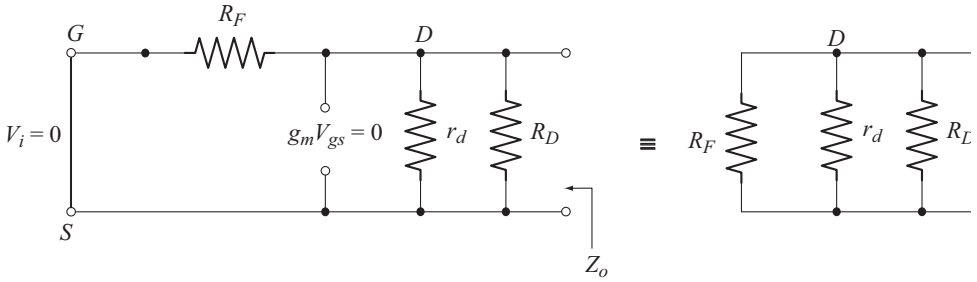


Fig 9.40 Circuit to find Z_o

From Fig. 9.40 we find that

$$Z_o = R_F \,||\, r_d \,||\, R_D \tag{9.116}$$

Approximate Expression for Z_o

Using the conditions

$R_F \gg r_d \,||\, R_D$ and $r_d \geq 10\, R_D$ in Equation (9.116) we get

$$Z_o \approx R_D \tag{9.117}$$

Example 9.19

A MOSFET has $V_{GS\,(Th)} = 3.5$ V and it is biased at $V_{GS_Q} = 7$ V. Assuming $k = 0.5 \times 10^{-3}$ A/V^2 calculate the value of g_m.

Solution

$$g_m = 2\,k\,[V_{GS_Q} - V_{GS\,(Th)}]$$
$$= (2)\,(0.5 \times 10^{-3}\ \text{A/V}^2)\,[7\text{V} - 3.5\text{V}] = 3.5\ \text{mS}.$$

Example 9.20

An E-MOSFET amplifier circuit has the following data.

$$V_T = 4\text{ V} \qquad I_{D\,(on)} = 4\text{ mA}$$
$$V_{GS}(\text{on}) = 7\text{V} \qquad y_{os} = 25\ \mu\text{S}.$$

Calculate the values of k, g_m and r_d.

Solution

$$I_D = k\,[V_{GS} - V_{GS\,(\text{Th})}]^2$$
$$\Rightarrow \quad I_{D\,(\text{on})} = k\,[V_{GS\,(\text{on})} - V_{GS\,(\text{Th})}]^2$$
$$k = \frac{I_{D(\text{on})}}{\left[V_{GS(\text{on})} - V_{GS(\text{Th})}\right]^2}$$

Note that $V_T = V_{GS\,(\text{Th})}$

$$k = \frac{4\,\text{mA}}{[7\,\text{V} - 4\,\text{V}]^2}$$
$$= 0.44 \times 10^{-3}\ \text{A/V}^2$$

$$g_m = 2\,k\,[V_{GS_Q} - V_{GS\,(\text{Th})}]$$
$$V_{GS_Q} = V_{GS\,(\text{on})}$$
$$g_m = 2\,[0.44 \times 10^{-3}\text{A/V}^2]\,[7\text{ V} - 4\text{ V}]$$
$$= 2.64\text{ mS}.$$

$$r_d = \frac{1}{y_{os}}$$
$$= \frac{1}{25\ \mu\text{S}} = 40\ \text{k}\Omega$$

Example 9.21

For the E-MOSFET drain feed back amplifier shown below:

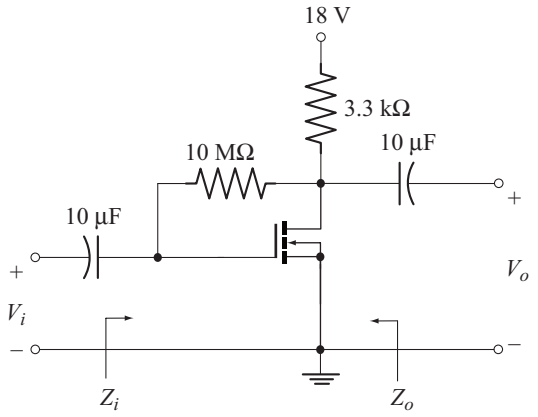
(a) Calculate g_m and r_d.

(b) Determine Z_i and Z_o.

(c) Calculate A_V.

(d) Find V_o if $V_i = 5$ mV.

(f) Calculate Z_i, Z_o, A_V and V_o, neglecting the effect of r_d and compare the results.



$V_{GS(Th)} = 3$ V
$k = 0.4 \times 10^{-3}$ A/V^2
$y_{os} = 10$ µS
$V_{GSQ} = 6$ V

Solution

(a) $$g_m = 2\text{ k}\left[V_{GS_Q} - V_{GS(\text{Th})}\right]$$
$$= (2)\,(0.4 \times 10^{-3}\text{ A/V}^2)\,[6\text{ V} - 3\text{ V}] = 2.4\text{ mS}.$$
$$r_d = \frac{1}{y_{os}} = \frac{1}{10\,\mu\text{S}} = 100\text{ k}\Omega$$

(b) $$Z_i = \frac{R_F + [r_d \,\|\, R_D]}{1 + g_m [r_d \,\|\, R_D]}$$
$$= \frac{10\,\text{M}\Omega + [100\,\text{k}\Omega \,\|\, 3.3\,\text{k}\Omega]}{1 + [2.4\,\text{mS}][100\,\text{k}\Omega \,\|\, 3.3\,\text{k}\Omega]} = 1.15\text{ M}\Omega$$
$$Z_o = R_F \,\|\, r_d \,\|\, R_D$$
$$= 10\text{ M}\Omega \,\|\, 100\text{ k}\Omega \,\|\, 3.3\text{ k}\Omega = 3.29\text{ k}\Omega$$

(c) $$A_V = \left[\frac{1}{R_F} - g_m\right][R_F \,\|\, r_d \,\|\, R_D]$$
$$= \left[\frac{1}{10\,\text{M}\Omega} - 2.4\,\text{mS}\right][10\text{ M}\Omega \,\|\, 100\text{ k}\Omega \,\|\, 3.3\text{ k}\Omega]$$
$$= -7.89$$

(d) $$V_o = A_V V_i$$
$$= [-7.89]\,[5\text{ mV}] = -39.45\text{ mV}$$

(e) ***When the effect of r_d is neglected***

$$R_F = 10\text{ M}\Omega \quad \text{and} \quad r_d \,\|\, R_D = 3.19\text{ k}\Omega$$

Note that, $$R_F >> r_d \,\|\, R_D$$
$$r_d = 100\text{ k}\Omega \quad \text{and} \quad 10\,R_D = 33\text{ k}\Omega$$

Also note that $r_d > 10\ R_D$.

Hence we can use approximate results by neglecting r_d.

$$Z_i \approx \frac{R_F}{1 + g_m R_D}$$

$$= \frac{10\,\text{MW}}{1 + [2.4\,\text{mS}]\,[3.3\,\text{kW}]} = 1.12\ \text{M}\Omega$$

$$Z_o \approx R_D = 3.3\ \text{k}\Omega$$

$$A_V \approx -g_m R_D = -[2.4\ \text{mS}]\,[3.3\ \text{k}\Omega] = -7.92$$

$$V_o = A_V V_i = [-7.92]\,[5\text{mV}] = -39.6\ \text{mV}.$$

The results are compared in the following table.

Parameter	*With* r_d	*With out* r_d
Z_i	1.15 MΩ	1.12 MΩ
Z_o	3.29 MΩ	3.3 MΩ
A_V	–7.89	–7.92

Note that the results are very close since the conditions $R_F >> r_d \parallel R_D$ and $r_d > 10\ R_D$ are satisfied.

9.21 E-MOSFET COMMON-SOURCE AMPLIFIER USING VOLTAGE DIVIDER CONFIGURATION

Figure 9.41 shows the circuit of E-MOSFET common-source amplifier using voltage divider bias.

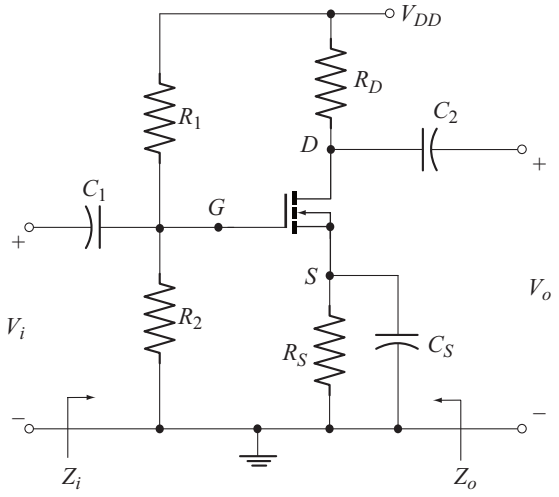


Fig. 9.41 E-MOSFET voltage divider configuration

The ac equivalent circuit is drawn in Fig. 9.42 by

- reducing V_{DD} to zero
- replacing the capacitors C_1, C_2 and C_S with their short circuit equivalents and
- replacing E-MOSFET with its small-signal ac model

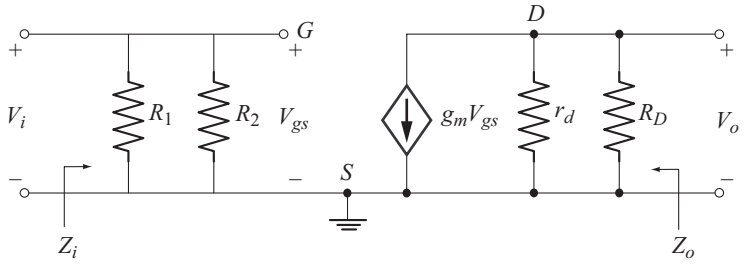


Fig. 9.42 AC equivalent circuit of E-MOSFET voltage divider configuration

This circuit is exactly identical that of Fig. 9.20 analysed in section 9.12, for JFET voltage divider bias configuration. The results are reproduced below for reference.

When the effect of r_d is included

$$Z_i = R_1 \| R_2 \tag{9.118}$$

$$Z_o = r_d \| R_D \tag{9.119}$$

$$A_V = -g_m [r_d \| R_D] \tag{9.120}$$

The negative sign in A_V reveals that V_o and V_i are 180° out of phase.

***When the effect of r_d is neglected* [*For $r_d \geq 10\ R_D$*]**

$$Z_i = R_1 \| R_2 \tag{9.121}$$

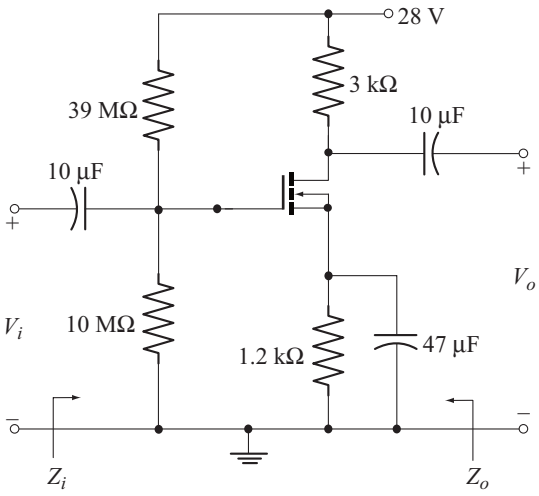
$$Z_o \approx R_D \tag{9.122}$$

$$A_V \approx -g_m R_D \tag{9.123}$$

Example 9.22

For the E–MOSFET voltage divider configuration shown

(a) Calculate Z_i and Z_o.
(b) Calculate A_V.
(c) Find V_o if $V_i = 1$ mV.
(d) Calculate Z_i, Z_o, A_V and V_o, neglecting the effect of r_d.



$V_{GS\,(Th)} = 3$ V

$k = 0.4 \times 10^{-3}$ A/V^2

$V_{GSQ} = 4.8$ V

$y_{os} = 25$ µS

Solution

$$g_m = 2k\left[V_{GS_Q} - V_{GS(Th)}\right]$$

$$= 2\,[0.4 \times 10^{-3}\ \text{A/V}^2]\,[4.8\text{V} - 3\text{V}] = 1.44\ \text{mS}$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{25\ \mu\text{S}} = 40\ \text{k}\Omega$$

(a) $Z_i = R_1 \parallel R_2 = 39\ \text{M}\Omega \parallel 10\ \text{M}\Omega = 7.95\ \text{M}\Omega$

$Z_o = r_d \parallel R_D = 40\ \text{k}\Omega \parallel 3\ \text{k}\Omega = 2.79\ \text{k}\Omega$

(b) $A_V = -g_m\,[r_d \parallel R_D] = -\,[1.44\ \text{mS}]\,[2.79\ \text{k}\Omega] = -4.01$

(c) $V_o = A_V V_i = [-4.01]\,[1\ \text{mV}] = -4.01\ \text{mV}$

(d) $r_d = 40\ \text{k}\Omega$ and $10\,R_D = 30\ \text{k}\Omega$

Since $r_d > 10\,R_D$, the effect of r_d can be neglected.

$Z_i = R_1 \parallel R_2 = 7.95\ \text{M}\Omega$

$Z_o \approx R_D = 3\ \text{k}\Omega$

$A_V \approx -g_m R_D = -\,[1.44\ \text{mS}]\,[3\ \text{k}\Omega] = -4.32$

$V_o = A_V V_i = [-4.32]\,[1\ \text{mV}] = -4.32\ \text{mV}.$

9.22 DESIGN OF FET AMPLIFIERS

Design of FET amplifiers involve the calculation of circuit elements R_D, R_G, R_S, C_1, C_2 and C_S to meet the required ac and dc specifications.

In most of the cases, drain supply voltage V_{DD} is known. The values of R_D and R_S are calculated from the gain and biasing requirements. In majority of the circuits, R_G decides the input impedance.

The capacitors C_1, C_2 and C_S are calculated to meet the required frequency response specifications. The following examples illustrate the design of some of the FET amplifier networks.

Example 9.23

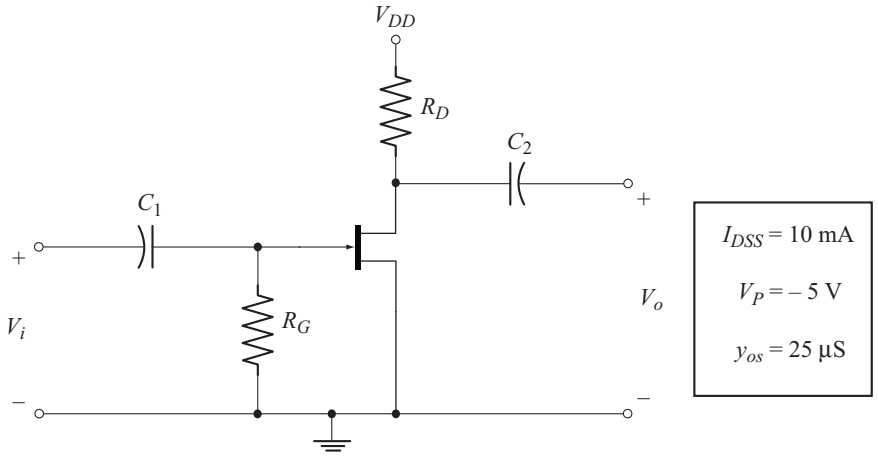
Design the fixed bias FET common–source amplifier shown below to meet the following requirements.

Magnitude of voltage gain, $|A_V|$: 12

Input impedance, Z_i : 10 MΩ

Available drain supply voltage, V_{DD} : 40 V

For the circuit designed, calculate the values of V_{DS_Q} and Z_o.



Solution

Selection of R_G

For the given circuit

$$Z_i = R_G$$

Since $Z_i = 10\ \text{M}\Omega$

Select $R_G = 10\ \text{M}\Omega$

Selection of R_D

$$A_V = -g_m [R_D \parallel r_d] \qquad \text{(A)}$$

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

For the given circuit, $V_{GS_Q} = 0$ [since $R_S = 0$].

$$\therefore \quad g_m = g_{m_o} = \frac{2I_{DSS}}{|V_p|} = \frac{(2)(10\ \text{mA})}{5\ \text{V}}$$

$$\therefore \quad g_m = 4\ \text{mS}.$$

Given, $A_V = 12$

Since common source configuration is an inverting amplifier, A_V is negative

$$\therefore \quad A_V = -12$$

$$r_d = \frac{1}{y_{os}} = 40\ \text{k}\Omega.$$

From Equation (A)

$$-12 = -4\ \text{mS}\ [R_D \parallel r_d]$$

$$R_D \parallel r_d = 3\ \text{k}\Omega$$

$$\left[\frac{R_D\, r_d}{R_D + r_d}\right] = 3\ \text{k}\Omega$$

Solving we get

$$R_D = 3.24\ \text{k}\Omega$$

Output impedance, $\boldsymbol{Z_o}$

$$Z_o = R_D \parallel r_d = 3.24\ \text{k}\Omega \parallel 40\ \text{k}\Omega = 3\ \text{k}\Omega$$

Calculation of V_{DSQ}

Applying KVL to the drain circuit, we have

$$V_{DD} = I_{D_Q} R_D + V_{DS_Q} \qquad \text{(B)}$$

$$I_{D_Q} = I_{DSS}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$= I_{DSS} = 10\ \text{mA} \qquad [\text{Since } V_{GSQ} = 0]$$

Now from Equation (B), we get

$$V_{DD} = I_{D_Q} R_D + V_{DS_Q} \qquad \text{(B)}$$

$$40\ \text{V} = (10\ \text{mA})\,(3.24\ \text{k}\Omega) + V_{DS_Q}$$

$$V_{DS_Q} = 7.6\ \text{V}$$

Example 9.24

Design the self bias FET common-source amplifier shown below to meet the following requirements:

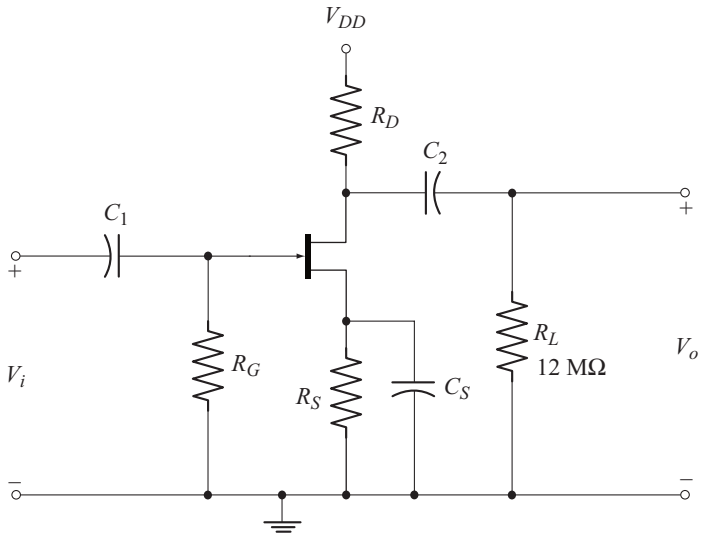
Magnitude of voltage gain, $|A_V|$: 10

Input impedance, Z_i : 5 MΩ

Quiescent gate to source voltage, $V_{GSQ} : \frac{V_P}{3}$

Available drain supply voltage, V_{DD} : 20 V

For the circuit designed calculate the values of V_{DSQ} and Z_o.



I_{DSS} = 12 mA

V_P = – 3 V

r_d = 40 kΩ

Solution

Selection of R_G

For the given circuit, $Z_i = R_G$

But $Z_i = 5\ \text{M}\Omega$

$\therefore$ We select $R_G = 5\ \text{M}\Omega$

Selection of R_D

$$A_V = -g_m [R_D \| r_d \| R_L]$$

Since R_L = 12 MΩ which is very high relative to r_d, we can treat it as an open circuit.

$$\therefore \quad A_V \approx -g_m [R_D \| r_d] \qquad \text{(A)}$$

$$g_m = g_{m_o}\left[1 - \frac{V_{GS_Q}}{V_p}\right]$$

$$V_{GS_Q} = \frac{V_P}{3} \Rightarrow \frac{V_{GS_Q}}{V_P} = \frac{1}{3}$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|} = \frac{(2)\,(12\,\text{mA})}{3\,\text{V}} = 8\ \text{mS}.$$

$$g_m = 8\ \text{mS}\left[1 - \frac{1}{3}\right] = 5.33\ \text{mS}$$

Now from Equation (A), we have

$$-10 = [-5.33\ \text{mS}]\,[R_D \| r_d]$$

$$R_D \| r_d = 1.876\ \text{k}\Omega$$

$$\frac{R_D . r_d}{R_D + r_d} = 1.876\ \text{k}\Omega$$

$$\frac{R_D\ (40\,\text{kW})}{R_D + 40\,\text{kW}} = 1.876\ \text{k}\Omega$$

Solving we get, $R_D = 1.968\ \text{k}\Omega$

Calculation of R_S

$$V_{GS_Q} = -I_{D_Q} R_S \qquad \text{(B)}$$

$$V_{GS_Q} = \frac{V_P}{3} = \frac{-3\text{V}}{3} = -1\ \text{V}$$

$$I_{D_Q} = I_{DSS}\left[1 - \frac{V_{GS_Q}}{V_p}\right]^2$$

$$= 12\ \text{mA}\left[1 - \frac{1}{3}\right]^2 = 6.66\ \text{mA}$$

From Equation (B),

$$R_S = -\frac{V_{GS_Q}}{I_{D_Q}}$$

$$R_S = -\frac{-1\text{V}}{6.66\ \text{mA}} = 150\ \Omega$$

Output impedance, Z_o

$$Z_o = R_D \,||\, r_d \,||\, R_L$$

$$= 1.968\ \text{k}\Omega \,||\, 40\ \text{k}\Omega \,||\, 12\ \text{M}\Omega$$

$$\approx 1.968\ \text{k}\Omega \,||\, 40\ \text{k}\Omega = 1.875\ \text{k}\Omega.$$

Drain-source voltage, V_{DSQ}

Applying KVL to the drain circuit, we have

$$V_{DD} = I_{D_Q} R_D + V_{DS_Q} + I_{D_Q} R_S$$

$$20\ \text{V} = (6.66\ \text{mA})\ (1.968\ \text{k}\Omega) + V_{DS_Q} + 1\ \text{V}$$

$$V_{DS_Q} = 5.89\text{V}$$

Example 9.25

Design the self biased FET common-source amplifier with unbypassed R_S, shown below to meet the following requirements:

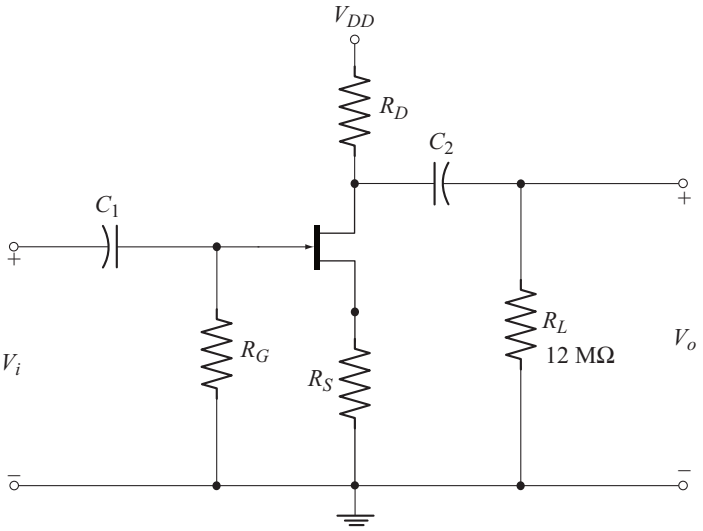
Magnitude of voltage gain, $|A_V|$: 8

Input impedance Z_i : 2 MΩ

Quiescent gate to source voltage V_{GS_Q} : $\frac{V_P}{4}$

Available drain supply voltage V_{DD} : 30 V

For the circuit designed, calculate the values of Z_o and V_{DSQ}



I_{DSS} = 10 mA

V_P = – 5 V

r_d = 50 kΩ

Solution

Selection of R_G

For the given circuit, $Z_i = R_G$

But $Z_i = 2\ \text{M}\Omega$

∴ We select $R_G = 2\ \text{M}\Omega$

Selection of R_S

$$V_{GS_Q} = -I_{D_Q} R_S \qquad \text{(A)}$$

$$V_{GS_Q} = \frac{V_P}{4} = \frac{-5\text{V}}{4} = -1.25\ \text{V}$$

$$I_{D_Q} = I_{DSS}\left[1 - \frac{V_{GS_Q}}{V_p}\right]^2$$

$$= 10\ \text{mA}\left[1 - \frac{-1.25\ \text{V}}{-5\ \text{V}}\right]^2 = 5.625\ \text{mA}$$

From Equation (A)

$$R_S = -\frac{V_{GS_Q}}{I_{D_Q}} = -\frac{-1.25\text{V}}{5.625\text{ mA}} = 222.2\ \Omega$$

Selection of R_D

To simplify the calculation, for the moment, let us assume that $r_d \geq 10\ [R_D + R_S]$. we will justify our assumption after the calculation of R_D.

$$\text{Now} \qquad A_V \approx -\frac{g_m R_D}{1+g_m R_S} \tag{B}$$

R_L is not considered since it is relatively larger.

$$g_m = g_{m_o}\left[1-\frac{V_{GS_Q}}{V_p}\right]$$

$$g_{m_o} = \frac{2I_{DSS}}{|V_p|} = \frac{2\,[10\text{ mA}]}{5\text{V}} = 4\text{ mS}$$

$$g_m = 4\text{ mS}\left[1-\frac{-1.25\text{V}}{-5\text{V}}\right] = 3\text{ mS}.$$

Now from Equation (B), we have

$$R_D = -\frac{A_V[1+g_m R_S]}{g_m}$$

$$= -\frac{[-8]\,[1+(3\text{mS})(222.2\Omega)]}{3\text{mS}} = 4.44\ \text{k}\Omega$$

Justification of Assumption

$$r_d = 50\ \text{k}\Omega$$

$$10\,[R_D + R_S] = 10\,[4.44\ \text{k}\Omega + 222.2\ \Omega] = 46.62\ \text{k}\Omega$$

Observe that $r_d > 10\ [R_D + R_S]$, which justifies our assumption.

Output Impedance

Since $r_d > 10\ R_D$

$$Z_o \approx R_D$$

$$\therefore \qquad Z_o = 4.44\ \text{k}\Omega$$

Drain to Source Voltage

Applying KVL to the drain circuit we have

$$V_{DD} = I_{DQ} R_D + V_{DSQ} + I_{DQ} R_S$$

$$30\text{ V} = (5.625\text{ mA})\,(4.44\ \text{k}\Omega) + V_{DS_Q} + (5.625\text{ mA})\,(222.2\ \Omega)$$

$$V_{DS_Q} = 3.775\text{ V}.$$

Exercise Problems

9.1 A common-source JFET amplifier using self-bias with bypassed R_S has R_G = 1 MΩ, R_S = 2.7 kΩ, R_D = 3.9 kΩ, g_m = 2800 μS and r_d = 40 kΩ. Calculate Z_i, Z_o, A_V and A_I.

9.2 Repeat the previous problem with R_S unbypassed.

9.3 A JFET source-follower has R_G = 5 MΩ, R_D = 2 kΩ, R_S = 2.7 kΩ, g_m = 0.8 mS and r_d = 40 kΩ. Calculate Z_i, Z_o, A_V and A_I.

9.4 A JFET common-gate amplifier has R_G = 1.2 MΩ, R_D = 3 kΩ, g_m = 2 mS and r_d = 50 kΩ. Calculate Z_i, Z_o and A_V.

9.5 Design a self-biased common-source JFET amplifier with bypassed R_S which has $|A_V| = 8$ and Z_i = 10 MΩ. For the FET, g_m = 5 mS, r_d = 50 kΩ and V_{DD} = 22 V.

Bibliography

1. Chirlian P.M., *Analysis and Design of Integrated Electronic Circuits*, 2e, Prentice Hall of India, 2004.
2. Comer D.J. and Comer D.T., *Advanced Electronic Circuit Design*, John Wiley, 2002.
3. Gray P.R. and Meyer R.G., *Analysis and Design of Analog Integrated Circuits*, 3e John Wiley, 1994.
4. Hayt W.H. and *Neudeck G.W., Electronic Circuit analysis and Design*, 2e John Wiley, 1994.
5. Horenstein M.N., *Microelectronic Circuit and Devices*, 2e, Prentice Hall, 1996.
6. Johns D and Martin K, *Analog Integrated Circuit Design*, John Wiley, 1996.
7. Lunn, *Essence Analog Electronics*, Prentice Hall, 1997.
8. Malvino A.P., *Electronics Principles*, 6e, Tata McGraw-Hill, 1999.
9. Millman J. and Grabel A., *Microelectronics*, 2e McGraw-Hill, 1987.
10. Millman J. and Halkias C.C., *Integrated Electronics-Analog & Digital Circuits and Systems*, Tata McGraw-Hill, 2001.
11. Neamen D.A., *Electronic Circuit Analysis and Design*, 2e, Tata McGraw-Hill, 2002.
12. Rashid M.H., *Microelectronic Circuits: Analysis & Design,* PWS, Boston, 1999.
13. Robbins A.H. and Miller W., *Circuit Analysis with Devices: Theory and Practice*, Thomson Learning, 2004.
14. Robert L. Boylestad and Louis Nashelsky, *Electronic devices and Circuit Theory*, 8e, Pearson Education, 2002.
15. Sedra A.S and Smith K.C., *Microelectronic Circuits*, 5e, Oxford University Press, 2004.
16. Shilling D.L. and Belove C., *Electronic Circuits*, 2e, McGraw-Hill, 1979.
17. Smith R.J., *Electronics: Circuits and Devices*, 3e John Wiley, 1987.
18. Spencer R. and Ghausi M., *Introduction to Electronic Circuit design*, Prentice Hall, 2003.
19. Suresh Babu V., *Solid State Devices and Technology: A Simplified Approach*, Sanguine Technical Publishers, 2004.
20. White C., *Hands-On Electronics: A Practical Introduction to Analog and Digital Circuits*, Cambridge University Press, 2003.

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